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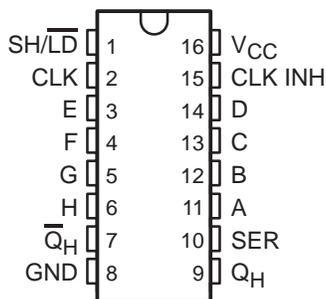
Jameco Part Number 380381

SN54HC165, SN74HC165 8-BIT PARALLEL-LOAD SHIFT REGISTERS

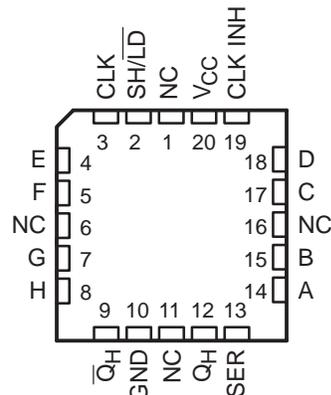
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- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 13$ ns
- ± 4 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- Complementary Outputs
- Direct Overriding Load (Data) Inputs
- Gated Clock Inputs
- Parallel-to-Serial Data Conversion

SN54HC165 . . . J OR W PACKAGE
SN74HC165 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC165 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The 'HC165 devices are 8-bit parallel-load shift registers that, when clocked, shift the data toward a serial (Q_H) output. Parallel-in access to each stage is provided by eight individual direct data (A–H) inputs that are enabled by a low level at the shift/load (SH/LD) input. The 'HC165 devices also feature a clock-inhibit (CLK INH) function and a complementary serial (\bar{Q}_H) output.

ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------|--------------|-----------------------|------------------|
| –40°C to 85°C | PDIP – N | Tube of 25 | SN74HC165N | SN74HC165N |
| | SOIC – D | Tube of 40 | SN74HC165D | HC165 |
| | | Reel of 2500 | SN74HC165DR | |
| | | Reel of 250 | SN74HC165DT | |
| | SOP – NS | Reel of 2000 | SN74HC165NSR | HC165 |
| | SSOP – DB | Reel of 2000 | SN74HC165DBR | HC165 |
| –55°C to 125°C | TSSOP – PW | Tube of 90 | SN74HC165PW | HC165 |
| | | Reel of 2000 | SN74HC165PWR | |
| | | Reel of 250 | SN74HC165PWT | |
| –55°C to 125°C | CDIP – J | Tube of 25 | SNJ54HC165J | SNJ54HC165J |
| | CFP – W | Tube of 150 | SNJ54HC165W | SNJ54HC165W |
| | LCCC – FK | Tube of 55 | SNJ54HC165FK | SNJ54HC165FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54HC165, SN74HC165 8-BIT PARALLEL-LOAD SHIFT REGISTERS

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description/ordering information (continued)

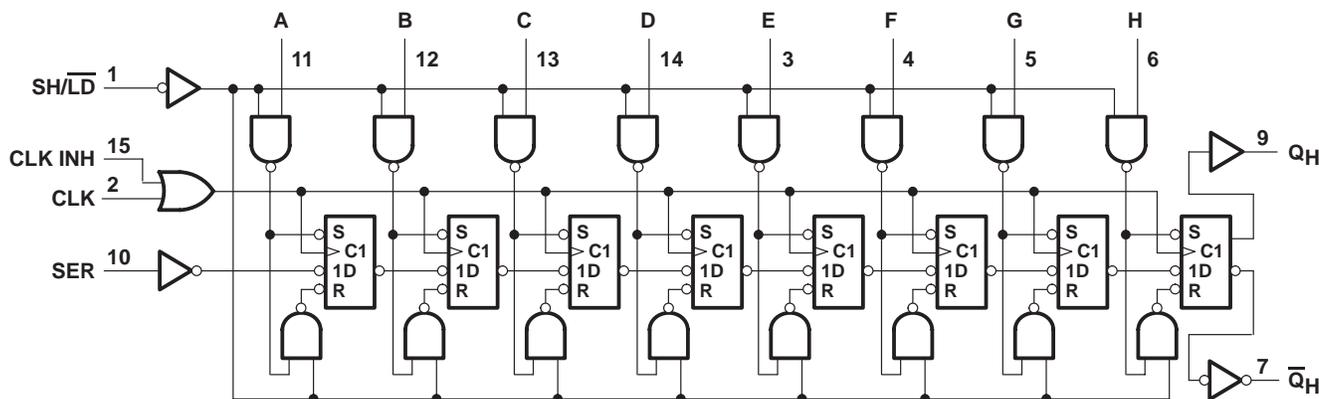
Clocking is accomplished by a low-to-high transition of the clock (CLK) input while SH/ $\overline{\text{LD}}$ is held high and CLK INH is held low. The functions of CLK and CLK INH are interchangeable. Since a low CLK and a low-to-high transition of CLK INH also accomplish clocking, CLK INH should be changed to the high level only while CLK is high. Parallel loading is inhibited when SH/ $\overline{\text{LD}}$ is held high. While SH/ $\overline{\text{LD}}$ is low, the parallel inputs to the register are enabled independently of the levels of the CLK, CLK INH, or serial (SER) inputs.

FUNCTION TABLE

| INPUTS | | | FUNCTION |
|----------------------------|------------|------------|-----------------|
| SH/ $\overline{\text{LD}}$ | CLK | CLK INH | |
| L | X | X | Parallel load |
| H | H | X | No change |
| H | X | H | No change |
| H | L | \uparrow | Shift \dagger |
| H | \uparrow | L | Shift \dagger |

\dagger Shift = content of each internal register shifts toward serial output Q_H . Data at SER is shifted into the first register.

logic diagram (positive logic)

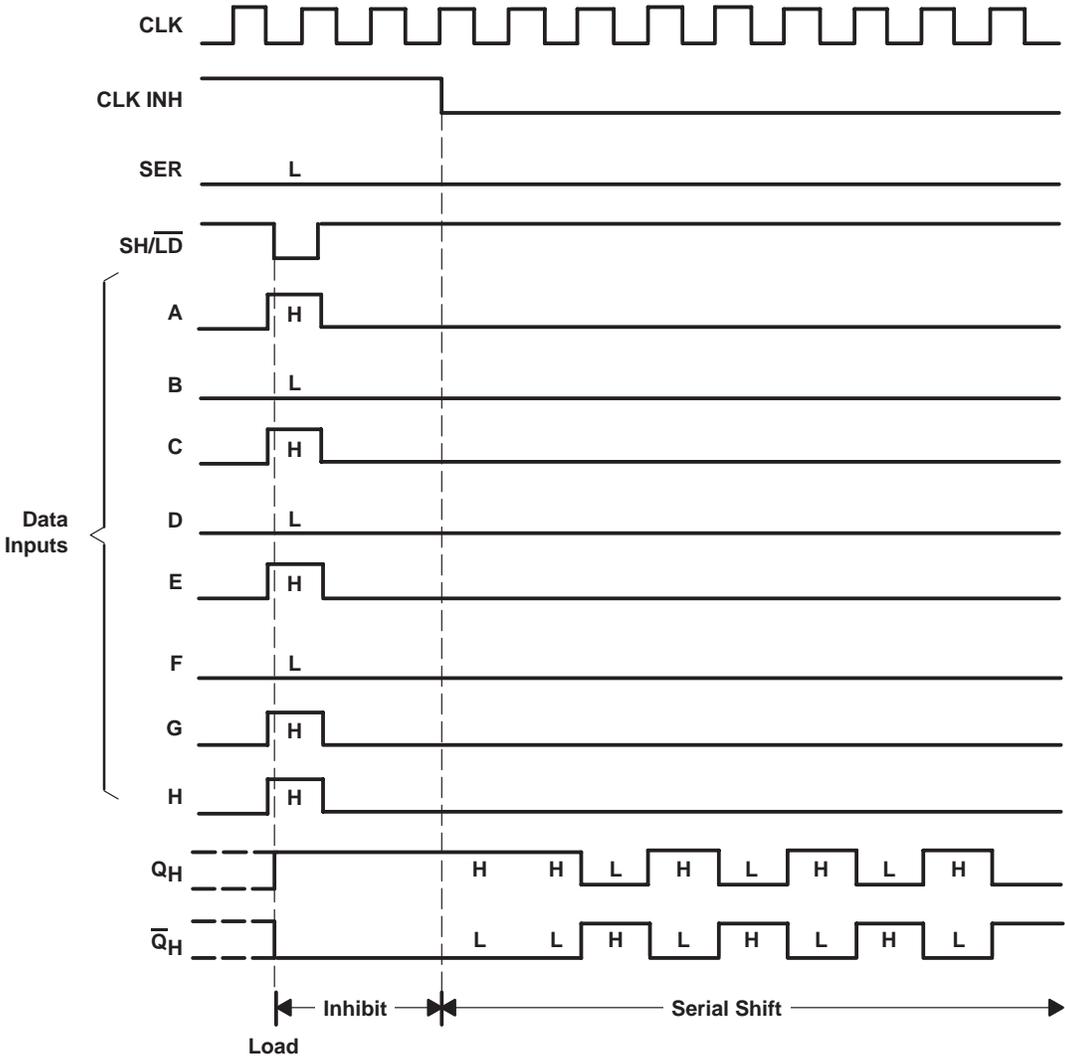


Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

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typical shift, load, and inhibit sequence



SN54HC165, SN74HC165

8-BIT PARALLEL-LOAD SHIFT REGISTERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|----------------|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) | ± 20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) | ± 20 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ± 25 mA |
| Continuous current through V_{CC} or GND | ± 50 mA |
| Package thermal impedance, θ_{JA} (see Note 2): D package | 73°C/W |
| DB package | 82°C/W |
| N package | 67°C/W |
| NS package | 64°C/W |
| PW package | 108°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

| | | SN54HC165 | | | SN74HC165 | | | UNIT |
|-----------------------|---------------------------------|------------------|-----|----------|-----------|-----|----------|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 2 | 5 | 6 | 2 | 5 | 6 | V |
| V_{IH} | High-level input voltage | $V_{CC} = 2$ V | | 1.5 | 1.5 | | V | |
| | | $V_{CC} = 4.5$ V | | 3.15 | 3.15 | | | |
| | | $V_{CC} = 6$ V | | 4.2 | 4.2 | | | |
| V_{IL} | Low-level input voltage | $V_{CC} = 2$ V | | | 0.5 | | V | |
| | | $V_{CC} = 4.5$ V | | | 1.35 | | | |
| | | $V_{CC} = 6$ V | | | 1.8 | | | |
| V_I | Input voltage | 0 | | V_{CC} | 0 | | V_{CC} | V |
| V_O | Output voltage | 0 | | V_{CC} | 0 | | V_{CC} | V |
| $\Delta t/\Delta v$ ‡ | Input transition rise/fall time | $V_{CC} = 2$ V | | | 1000 | | ns | |
| | | $V_{CC} = 4.5$ V | | | 500 | | | |
| | | $V_{CC} = 6$ V | | | 400 | | | |
| T_A | Operating free-air temperature | -55 | | 125 | -40 | | 85 | °C |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

‡ If this device is used in the threshold region (from $V_{ILmax} = 0.5$ V to $V_{IHmin} = 1.5$ V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at $t_t = 1000$ ns and $V_{CC} = 2$ V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.



SN54HC165, SN74HC165 8-BIT PARALLEL-LOAD SHIFT REGISTERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | V _{CC} | T _A = 25°C | | | SN54HC165 | | SN74HC165 | | UNIT |
|-----------------|---|---------------------------|-----------------|-----------------------|-------|------|-----------|-------|-----------|-------|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | V _I = V _{IH} or V _{IL} | I _{OH} = -20 μA | 2 V | 1.9 | 1.998 | | 1.9 | | 1.9 | V | |
| | | | 4.5 V | 4.4 | 4.499 | | 4.4 | | 4.4 | | |
| | | | 6 V | 5.9 | 5.999 | | 5.9 | | 5.9 | | |
| | | I _{OH} = -4 mA | 4.5 V | 3.98 | 4.3 | | 3.7 | | 3.84 | | |
| | | I _{OH} = -5.2 mA | 6 V | 5.48 | 5.8 | | 5.2 | | 5.34 | | |
| V _{OL} | V _I = V _{IH} or V _{IL} | I _{OL} = 20 μA | 2 V | | 0.002 | 0.1 | | 0.1 | | 0.1 | V |
| | | | 4.5 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | | 6 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | I _{OL} = 4 mA | 4.5 V | | 0.17 | 0.26 | | 0.4 | | 0.33 | |
| | | I _{OL} = 5.2 mA | 6 V | | 0.15 | 0.26 | | 0.4 | | 0.33 | |
| I _I | V _I = V _{CC} or 0 | | 6 V | | ±0.1 | ±100 | | ±1000 | | ±1000 | nA |
| I _{CC} | V _I = V _{CC} or 0, I _O = 0 | | 6 V | | | 8 | | 160 | | 80 | μA |
| C _i | | | 2 V to 6 V | | 3 | 10 | | 10 | | 10 | pF |

SN54HC165, SN74HC165 8-BIT PARALLEL-LOAD SHIFT REGISTERS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

| | | V _{CC} | T _A = 25°C | | SN54HC165 | | SN74HC165 | | UNIT |
|--------------------|--|-----------------|-----------------------|-----|-----------|-----|-----------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| f _{clock} | Clock frequency | 2 V | 6 | | 4.2 | | 5 | | MHz |
| | | 4.5 V | 31 | | 21 | | 25 | | |
| | | 6 V | 36 | | 25 | | 29 | | |
| t _w | SH/ $\overline{\text{LD}}$ low | 2 V | 80 | | 120 | | 100 | | ns |
| | | 4.5 V | 16 | | 24 | | 20 | | |
| | | 6 V | 14 | | 20 | | 17 | | |
| | CLK high or low | 2 V | 80 | | 120 | | 100 | | |
| | | 4.5 V | 16 | | 24 | | 20 | | |
| | | 6 V | 14 | | 20 | | 17 | | |
| t _{su} | SH/ $\overline{\text{LD}}$ high before CLK \uparrow | 2 V | 80 | | 120 | | 100 | | ns |
| | | 4.5 V | 16 | | 24 | | 20 | | |
| | | 6 V | 14 | | 20 | | 17 | | |
| | SER before CLK \uparrow | 2 V | 40 | | 60 | | 50 | | |
| | | 4.5 V | 8 | | 12 | | 10 | | |
| | | 6 V | 7 | | 10 | | 9 | | |
| | CLK INH low before CLK \uparrow | 2 V | 100 | | 150 | | 125 | | |
| | | 4.5 V | 20 | | 30 | | 25 | | |
| | | 6 V | 17 | | 25 | | 21 | | |
| | CLK INH high before CLK \uparrow | 2 V | 40 | | 60 | | 50 | | |
| | | 4.5 V | 8 | | 12 | | 10 | | |
| | | 6 V | 7 | | 10 | | 9 | | |
| | Data before SH/ $\overline{\text{LD}}$ \downarrow | 2 V | 100 | | 150 | | 125 | | |
| | | 4.5 V | 20 | | 30 | | 25 | | |
| | | 6 V | 17 | | 26 | | 21 | | |
| t _h | SER data after CLK \uparrow | 2 V | 5 | | 5 | | 5 | | ns |
| | | 4.5 V | 5 | | 5 | | 5 | | |
| | | 6 V | 5 | | 5 | | 5 | | |
| | PAR data after SH/ $\overline{\text{LD}}$ \downarrow | 2 V | 5 | | 5 | | 5 | | |
| | | 4.5 V | 5 | | 5 | | 5 | | |
| | | 6 V | 5 | | 5 | | 5 | | |



SN54HC165, SN74HC165 8-BIT PARALLEL-LOAD SHIFT REGISTERS

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switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V_{CC} | $T_A = 25^\circ\text{C}$ | | | SN54HC165 | | SN74HC165 | | UNIT |
|------------|----------------------------|---------------------------|----------|--------------------------|-----|-----|-----------|-----|-----------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f_{\max} | | | 2 V | 6 | 13 | | 4.2 | | 5 | MHz | |
| | | | 4.5 V | 31 | 50 | | 21 | | 25 | | |
| | | | 6 V | 36 | 62 | | 25 | | 29 | | |
| t_{pd} | SH/ $\overline{\text{LD}}$ | Q_H or \overline{Q}_H | 2 V | | 80 | 150 | | 225 | | 190 | ns |
| | | | 4.5 V | | 20 | 30 | | 45 | | 38 | |
| | | | 6 V | | 16 | 26 | | 38 | | 32 | |
| | CLK | Q_H or \overline{Q}_H | 2 V | | 75 | 150 | | 225 | | 190 | |
| | | | 4.5 V | | 15 | 30 | | 45 | | 38 | |
| | | | 6 V | | 13 | 26 | | 38 | | 32 | |
| | H | Q_H or \overline{Q}_H | 2 V | | 75 | 150 | | 225 | | 190 | |
| | | | 4.5 V | | 15 | 30 | | 45 | | 38 | |
| | | | 6 V | | 13 | 26 | | 38 | | 32 | |
| t_t | | Any | 2 V | | 38 | 75 | | 110 | | 95 | ns |
| | | | 4.5 V | | 8 | 15 | | 22 | | 19 | |
| | | | 6 V | | 6 | 13 | | 19 | | 16 | |

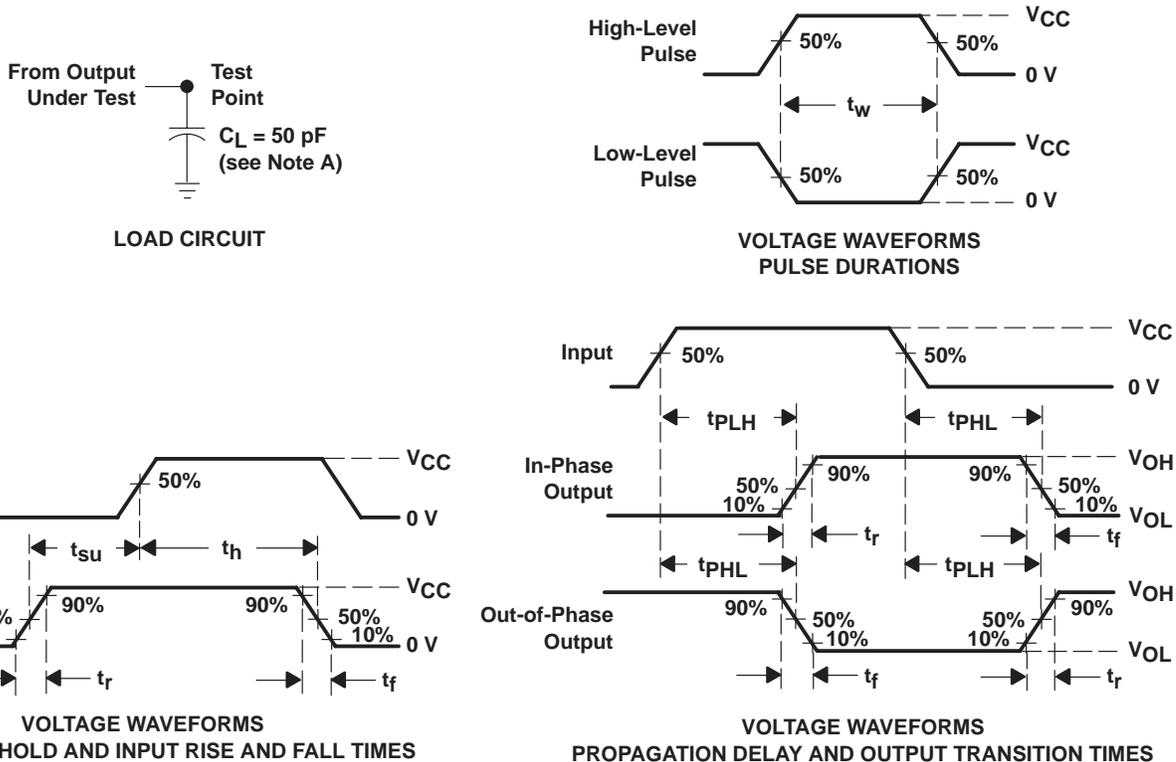
operating characteristics, $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|--|-----------------|-----|------|
| C_{pd} Power dissipation capacitance | No load | 75 | pF |

SN54HC165, SN74HC165 8-BIT PARALLEL-LOAD SHIFT REGISTERS

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PARAMETER MEASUREMENT INFORMATION



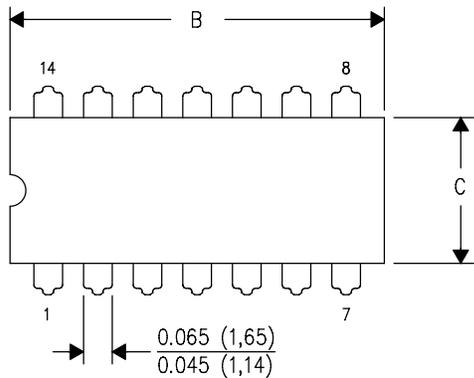
- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
 - C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

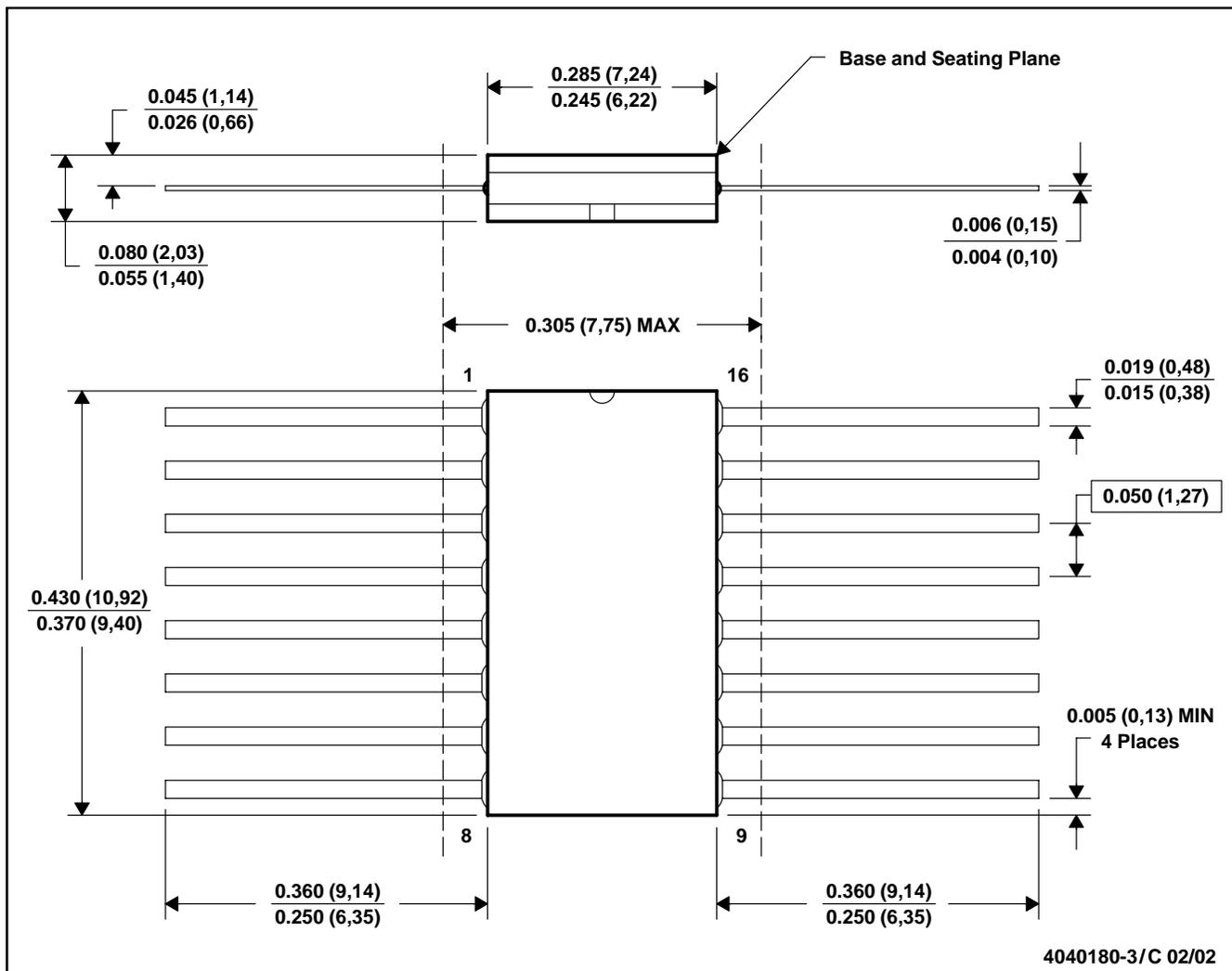


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- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK

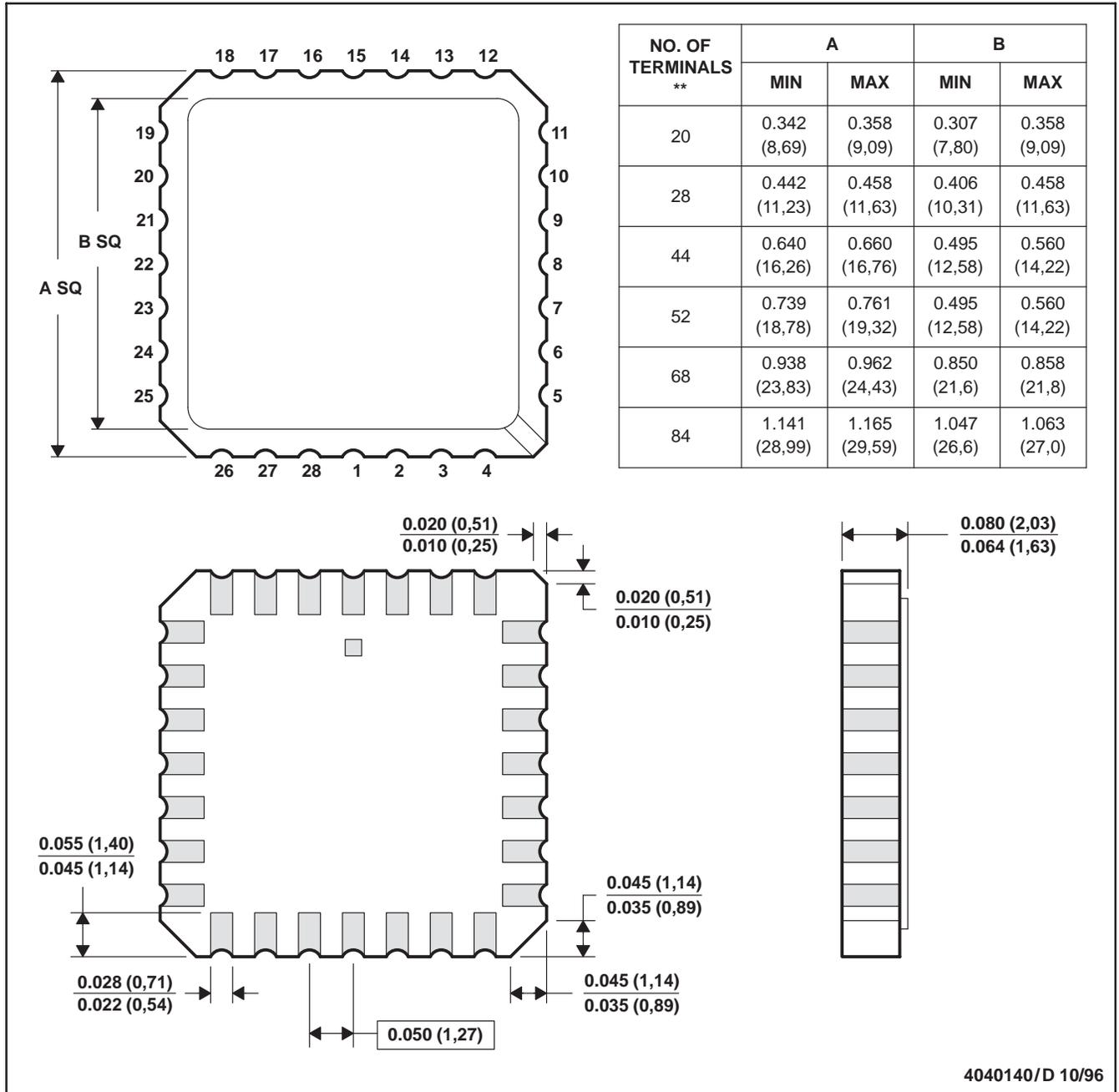


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only.
 E. Falls within MIL STD 1835 GDFP-1F16 and JEDEC MO-092AC

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

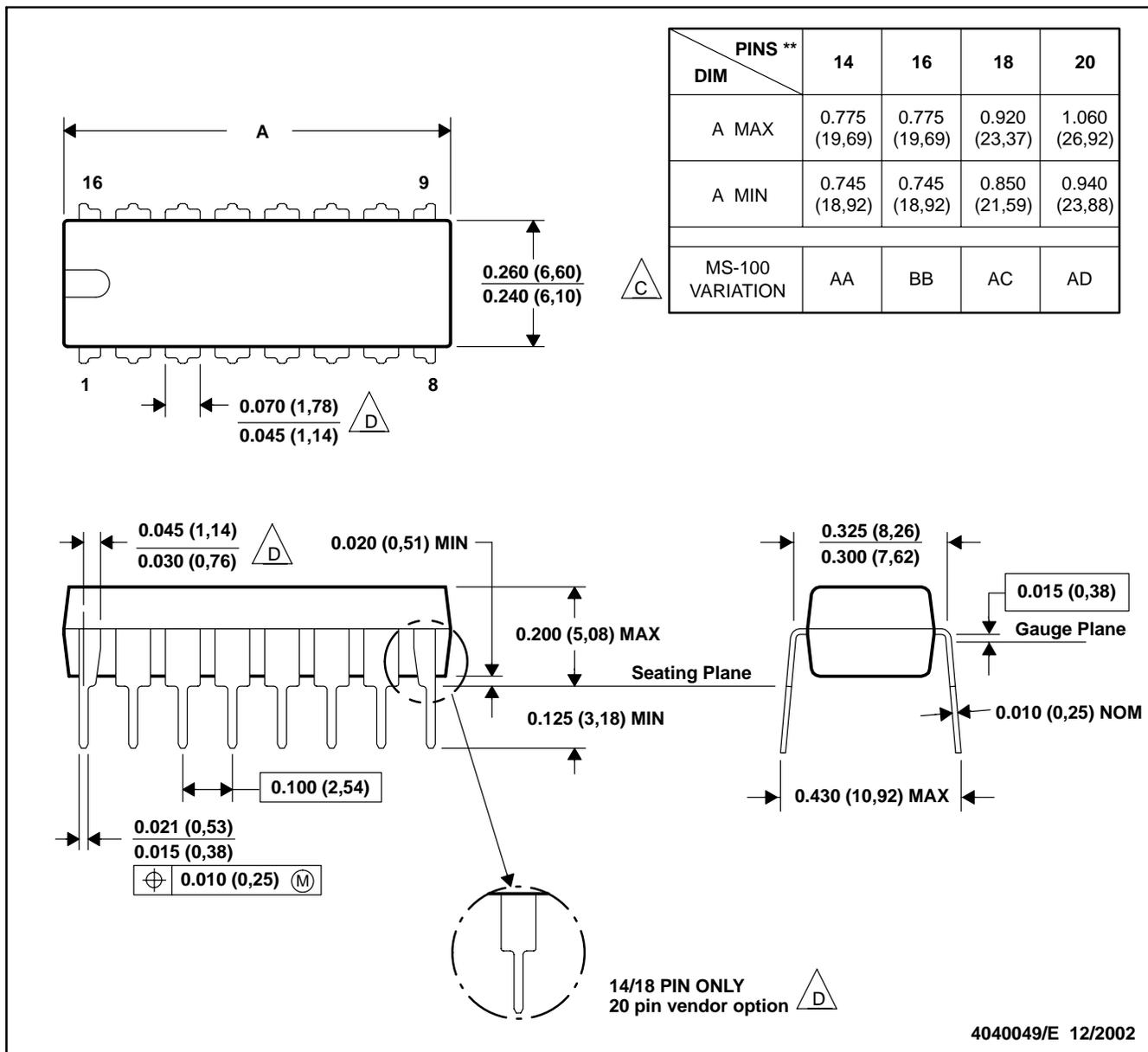


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

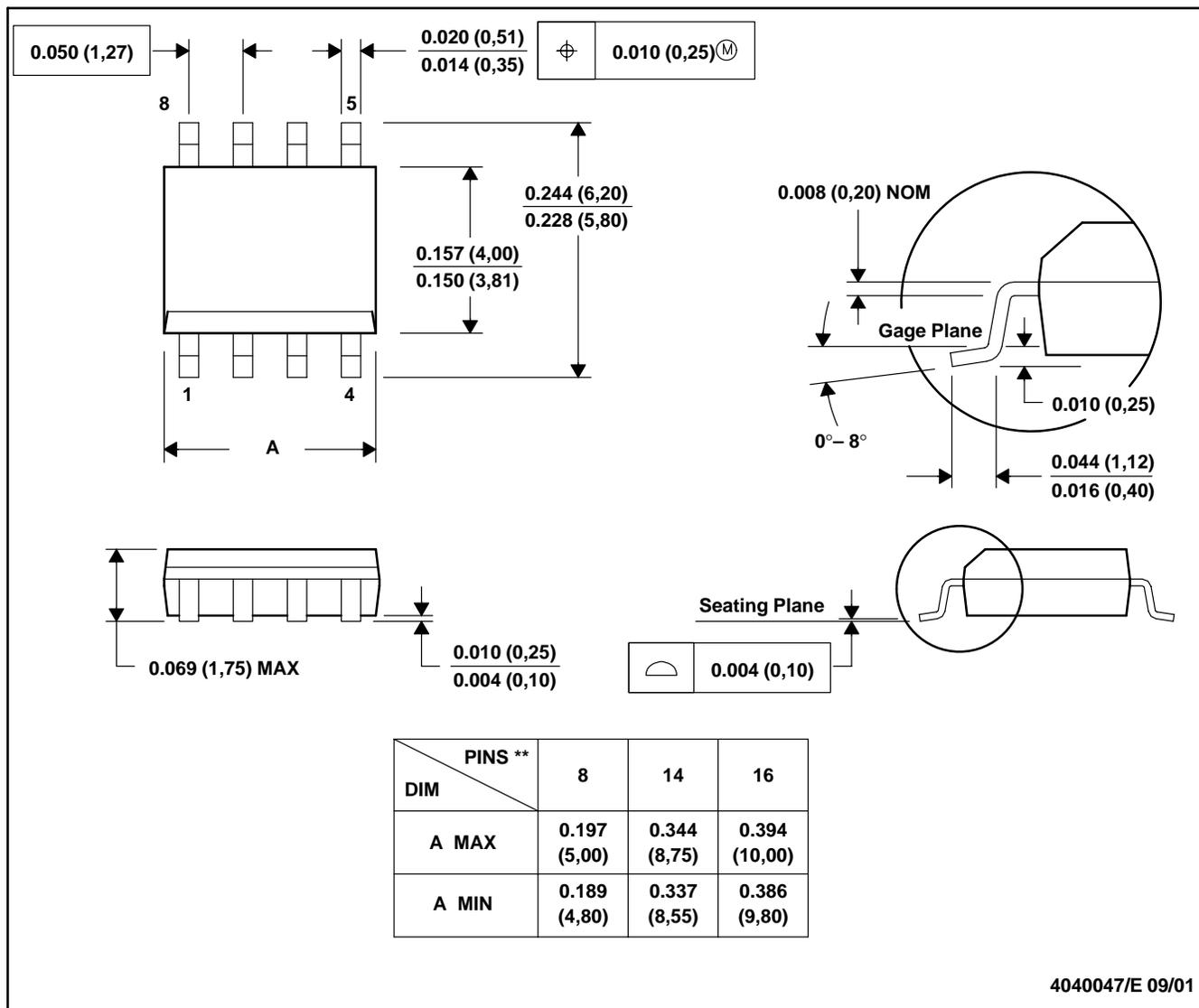


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 D The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



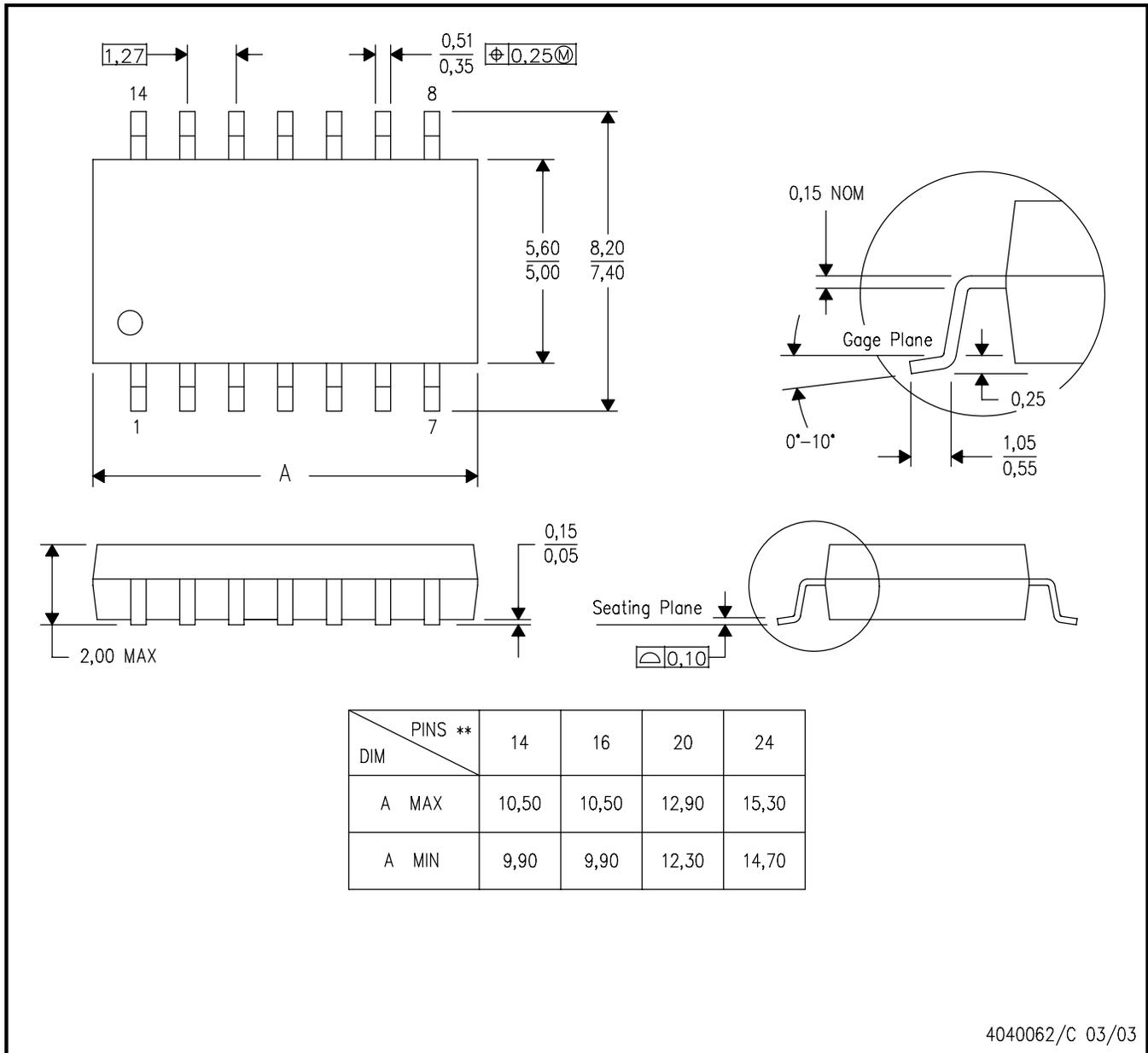
- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

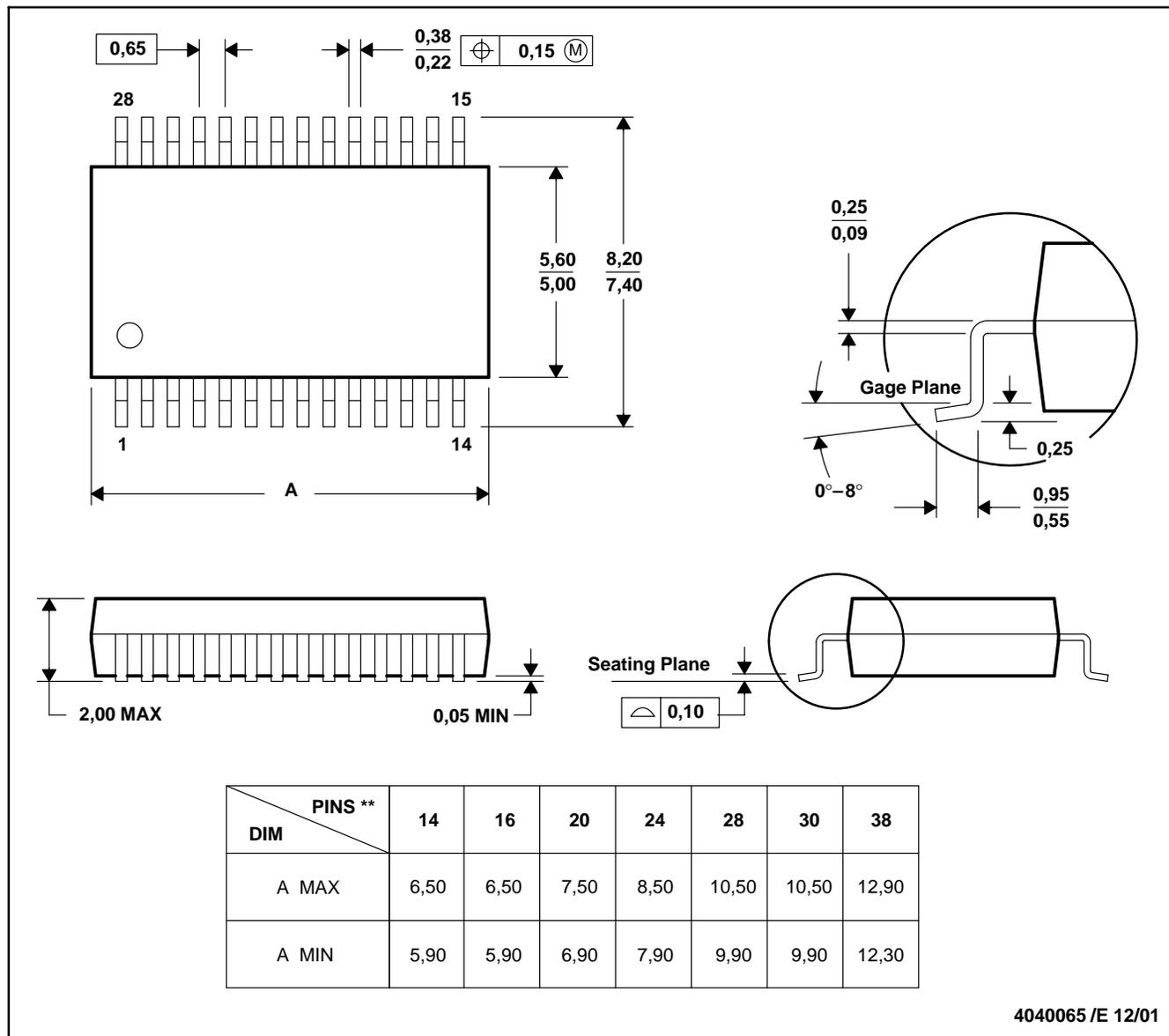


- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN

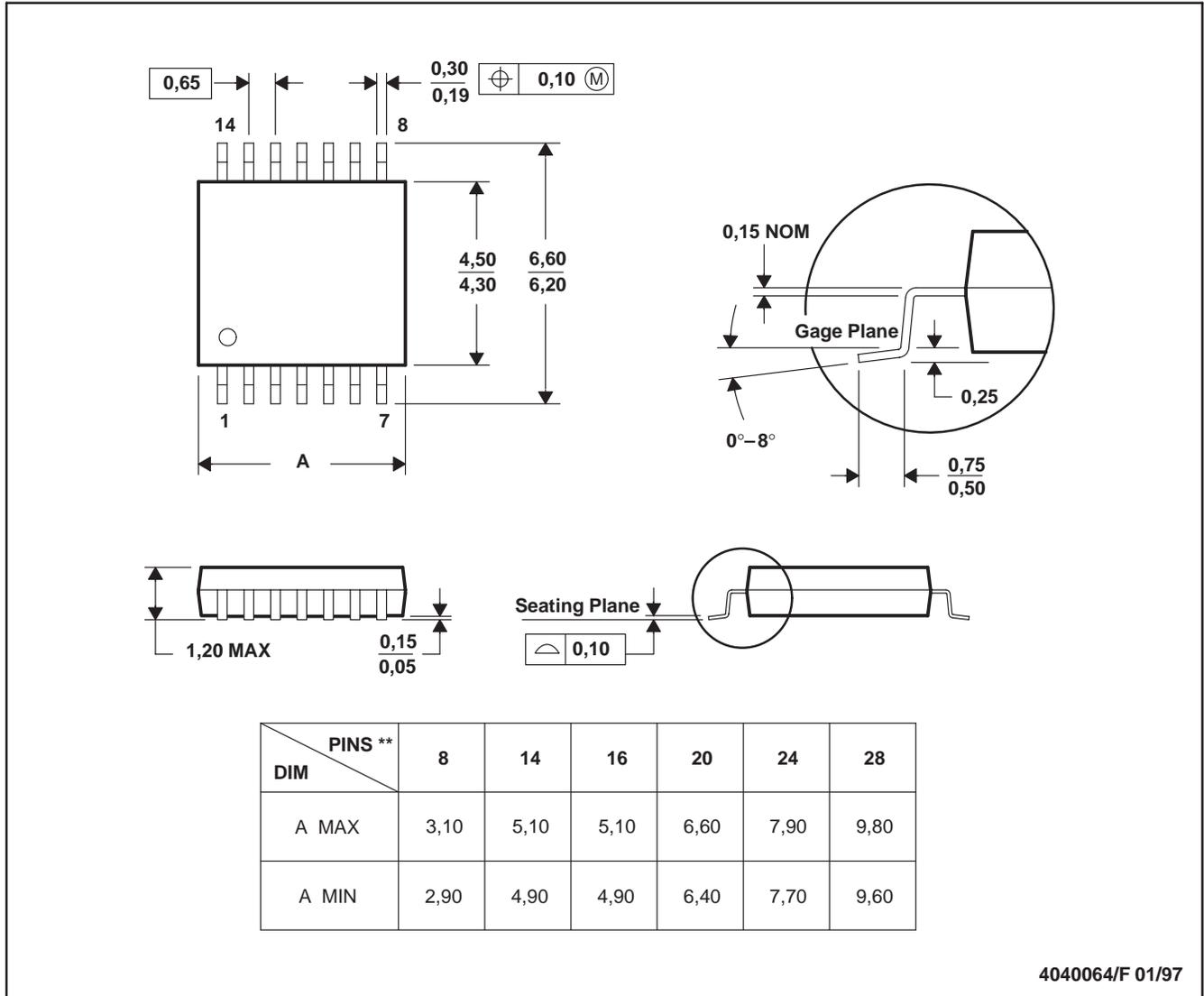


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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