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Jameco Part Number 915817

# SN54HC259, SN74HC259 8-BIT ADDRESSABLE LATCHES

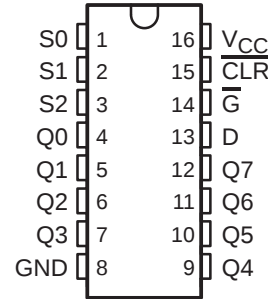
SCLS134E – DECEMBER 1982 – REVISED SEPTEMBER 2003

- Wide Operating Voltage Range of 2 V to 6 V
- High-Current Inverting Outputs Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd} = 14$  ns
- $\pm 4$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Max
- 8-Bit Parallel-Out Storage Register Performs Serial-to-Parallel Conversion With Storage
- Asynchronous Parallel Clear
- Active-High Decoder
- Enable Input Simplifies Expansion
- Expandable for n-Bit Applications
- Four Distinct Functional Modes

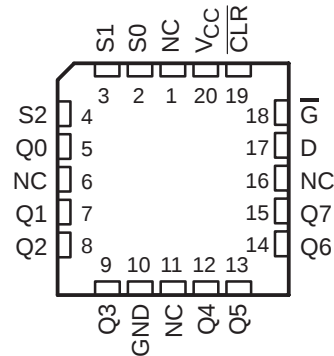
## description/ordering information

These 8-bit addressable latches are designed for general-purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches and being a 1-of-8 decoder or demultiplexer with active-high outputs.

SN54HC259 . . . J OR W PACKAGE  
SN74HC259 . . . D, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54HC259 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## ORDERING INFORMATION

| T <sub>A</sub> | PACKAGE <sup>†</sup> |              | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|----------------------|--------------|-----------------------|------------------|
| –40°C to 85°C  | PDIP – N             | Tube of 25   | SN74HC259N            | SN74HC259N       |
|                | SOIC – D             | Tube of 40   | SN74HC259D            | HC259            |
|                |                      | Reel of 2500 | SN74HC259DR           |                  |
|                |                      | Reel of 250  | SN74HC259DT           |                  |
|                | SOP – NS             | Reel of 2000 | SN74HC259NSR          | HC259            |
|                | TSSOP – PW           | Reel of 2000 | SN74HC259PWR          | HC259            |
|                |                      | Reel of 250  | SN74HC259PWT          |                  |
| –55°C to 125°C | CDIP – J             | Tube of 25   | SNJ54HC259J           | SNJ54HC259J      |
|                | CFP – W              | Tube of 150  | SNJ54HC259W           | SNJ54HC259W      |
|                | LCCC – FK            | Tube of 55   | SNJ54HC259FK          | SNJ54HC259FK     |

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# SN54HC259, SN74HC259

## 8-BIT ADDRESSABLE LATCHES

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### description/ordering information (continued)

Four distinct modes of operation are selectable by controlling the clear ( $\overline{\text{CLR}}$ ) and enable ( $\overline{\text{G}}$ ) inputs. In the addressable-latch mode, data at the data-in terminal is written into the addressed latch. The addressed latch follows the data input, with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches,  $\overline{\text{G}}$  should be held high (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output follows the level of the D input with all other outputs low. In the clear mode, all outputs are low and unaffected by the address and data inputs.

### Function Tables

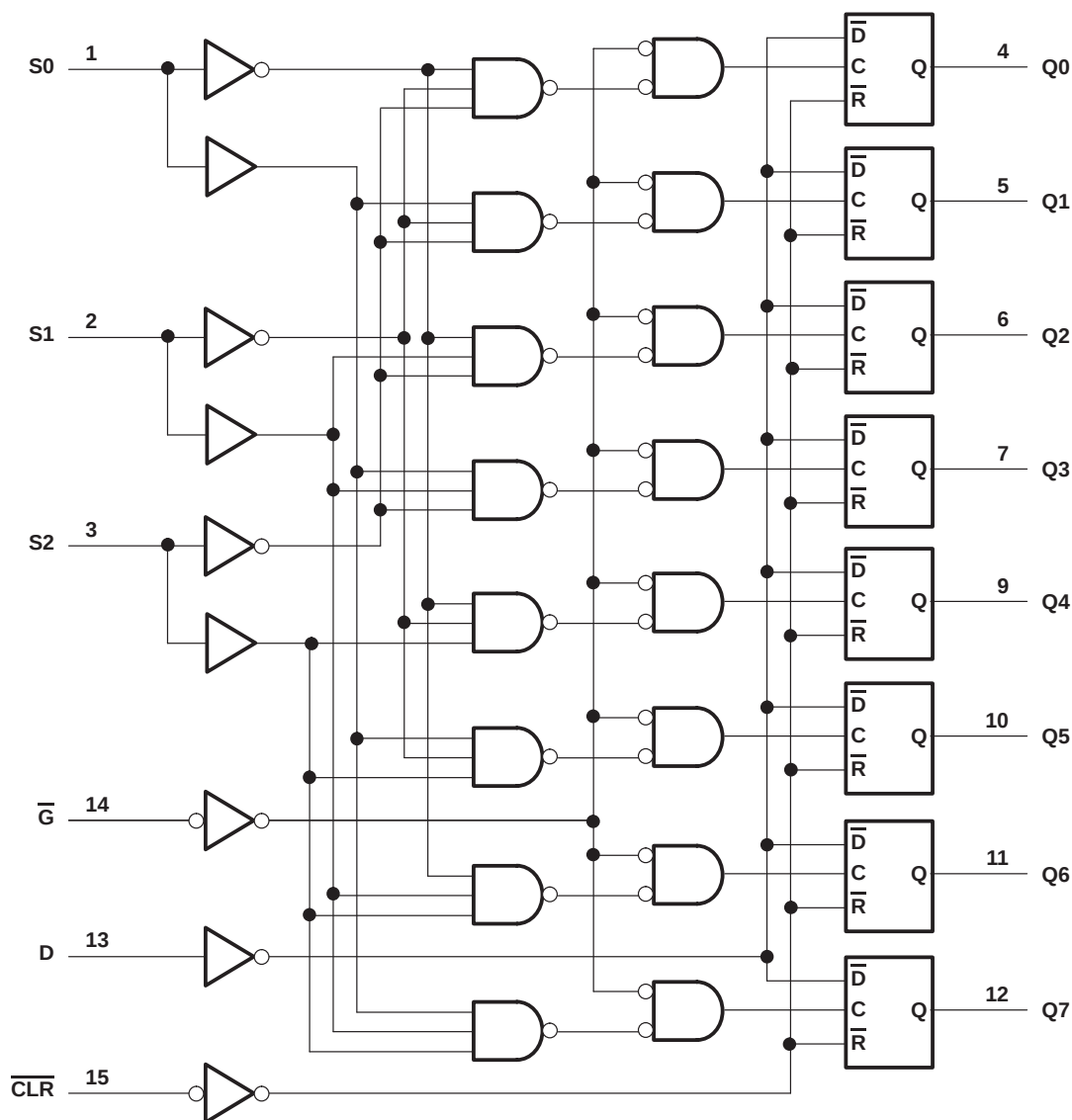
FUNCTION

| INPUTS                  |                       | OUTPUT OF<br>ADDRESSED<br>LATCH | EACH<br>OTHER<br>OUTPUT | FUNCTION             |
|-------------------------|-----------------------|---------------------------------|-------------------------|----------------------|
| $\overline{\text{CLR}}$ | $\overline{\text{G}}$ |                                 |                         |                      |
| H                       | L                     | D                               | $Q_iO$                  | Addressable latch    |
| H                       | H                     | $Q_iO$                          | $Q_iO$                  | Memory               |
| L                       | L                     | D                               | L                       | 8-line demultiplexer |
| L                       | H                     | L                               | L                       | Clear                |

LATCH SELECTION

| SELECT INPUTS |    |    | LATCH<br>ADDRESSED |
|---------------|----|----|--------------------|
| S2            | S1 | S0 |                    |
| L             | L  | L  | 0                  |
| L             | L  | H  | 1                  |
| L             | H  | L  | 2                  |
| L             | H  | H  | 3                  |
| H             | L  | L  | 4                  |
| H             | L  | H  | 5                  |
| H             | H  | L  | 6                  |
| H             | H  | H  | 7                  |

### logic diagram



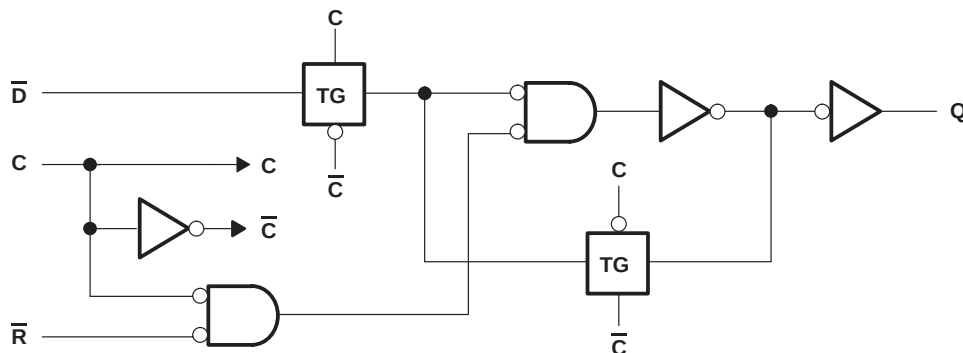
Pin numbers shown are for the D, J, N, NS, PW, and W packages.

# SN54HC259, SN74HC259

## 8-BIT ADDRESSABLE LATCHES

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**logic diagram, each internal latch (positive logic)**



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                                             |               |
|-----------------------------------------------------------------------------|---------------|
| Supply voltage range, $V_{CC}$                                              | -0.5 V to 7 V |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1)  | $\pm 20$ mA   |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1) | $\pm 20$ mA   |
| Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )                  | $\pm 25$ mA   |
| Continuous current through $V_{CC}$ or GND                                  | $\pm 50$ mA   |
| Package thermal impedance, $\theta_{JA}$ (see Note 2):                      |               |
| D package                                                                   | 73°C/W        |
| N package                                                                   | 67°C/W        |
| NS package                                                                  | 64°C/W        |
| PW package                                                                  | 108°C/W       |

Storage temperature range,  $T_{\text{stg}}$  .....  $-65^{\circ}\text{C}$  to  $150^{\circ}\text{C}$

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JEDEC 51-7.

**recommended operating conditions (see Note 3)**

|                     |                                 |                         | SN54HC259 |                 |     | SN74HC259 |                 |     | UNIT |
|---------------------|---------------------------------|-------------------------|-----------|-----------------|-----|-----------|-----------------|-----|------|
|                     |                                 |                         | MIN       | NOM             | MAX | MIN       | NOM             | MAX |      |
| V <sub>CC</sub>     | Supply voltage                  |                         | 2         | 5               | 6   | 2         | 5               | 6   | V    |
| V <sub>IH</sub>     | High-level input voltage        | V <sub>CC</sub> = 2 V   | 1.5       |                 |     | 1.5       |                 |     | V    |
|                     |                                 | V <sub>CC</sub> = 4.5 V | 3.15      |                 |     | 3.15      |                 |     |      |
|                     |                                 | V <sub>CC</sub> = 6 V   | 4.2       |                 |     | 4.2       |                 |     |      |
| V <sub>IL</sub>     | Low-level input voltage         | V <sub>CC</sub> = 2 V   | 0.5       |                 |     | 0.5       |                 |     | V    |
|                     |                                 | V <sub>CC</sub> = 4.5 V | 1.35      |                 |     | 1.35      |                 |     |      |
|                     |                                 | V <sub>CC</sub> = 6 V   | 1.8       |                 |     | 1.8       |                 |     |      |
| V <sub>I</sub>      | Input voltage                   |                         | 0         | V <sub>CC</sub> |     | 0         | V <sub>CC</sub> |     | V    |
| V <sub>O</sub>      | Output voltage                  |                         | 0         | V <sub>CC</sub> |     | 0         | V <sub>CC</sub> |     | V    |
| $\Delta t/\Delta v$ | Input transition rise/fall time | V <sub>CC</sub> = 2 V   | 1000      |                 |     | 1000      |                 |     | ns   |
|                     |                                 | V <sub>CC</sub> = 4.5 V | 500       |                 |     | 500       |                 |     |      |
|                     |                                 | V <sub>CC</sub> = 6 V   | 400       |                 |     | 400       |                 |     |      |
| T <sub>A</sub>      | Operating free-air temperature  |                         | -55       |                 | 125 | -40       |                 | 85  | °C   |

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN54HC259, SN74HC259 8-BIT ADDRESSABLE LATCHES

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER       | TEST CONDITIONS                                           |                           | V <sub>CC</sub> | T <sub>A</sub> = 25°C |       |      | SN54HC259 |       | SN74HC259 |       | UNIT |
|-----------------|-----------------------------------------------------------|---------------------------|-----------------|-----------------------|-------|------|-----------|-------|-----------|-------|------|
|                 |                                                           |                           |                 | MIN                   | TYP   | MAX  | MIN       | MAX   | MIN       | MAX   |      |
| V <sub>OH</sub> | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>       | I <sub>OH</sub> = -20 µA  | 2 V             | 1.9                   | 1.998 |      | 1.9       |       | 1.9       |       | V    |
|                 |                                                           |                           | 4.5 V           | 4.4                   | 4.499 |      | 4.4       |       | 4.4       |       |      |
|                 |                                                           |                           | 6 V             | 5.9                   | 5.999 |      | 5.9       |       | 5.9       |       |      |
|                 |                                                           | I <sub>OH</sub> = -4 mA   | 4.5 V           | 3.98                  | 4.3   |      | 3.7       |       | 3.84      |       |      |
|                 |                                                           | I <sub>OH</sub> = -5.2 mA | 6 V             | 5.48                  | 5.8   |      | 5.2       |       | 5.34      |       |      |
| V <sub>OL</sub> | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>       | I <sub>OL</sub> = 20 µA   | 2 V             |                       | 0.002 | 0.1  |           | 0.1   |           | 0.1   | V    |
|                 |                                                           |                           | 4.5 V           |                       | 0.001 | 0.1  |           | 0.1   |           | 0.1   |      |
|                 |                                                           |                           | 6 V             |                       | 0.001 | 0.1  |           | 0.1   |           | 0.1   |      |
|                 |                                                           | I <sub>OL</sub> = 4 mA    | 4.5 V           |                       | 0.17  | 0.26 |           | 0.4   |           | 0.33  |      |
|                 |                                                           | I <sub>OL</sub> = 5.2 mA  | 6 V             |                       | 0.15  | 0.26 |           | 0.4   |           | 0.33  |      |
| I <sub>I</sub>  | V <sub>I</sub> = V <sub>CC</sub> or 0                     |                           | 6 V             |                       | ±0.1  | ±100 |           | ±1000 |           | ±1000 | nA   |
| I <sub>CC</sub> | V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0 |                           | 6 V             |                       |       | 8    |           | 160   |           | 80    | µA   |
| C <sub>i</sub>  |                                                           |                           | 2 V to 6 V      |                       | 3     | 10   |           | 10    |           | 10    | pF   |

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

|                 |                                                                  |                             | V <sub>CC</sub> | T <sub>A</sub> = 25°C |     | SN54HC259 |     | SN74HC259 |     | UNIT |
|-----------------|------------------------------------------------------------------|-----------------------------|-----------------|-----------------------|-----|-----------|-----|-----------|-----|------|
|                 |                                                                  |                             |                 | MIN                   | MAX | MIN       | MAX | MIN       | MAX |      |
| t <sub>w</sub>  | Pulse duration                                                   | $\overline{\text{CLR}}$ low | 2 V             | 80                    |     | 120       |     | 100       |     | ns   |
|                 |                                                                  |                             | 4.5 V           | 16                    |     | 24        |     | 20        |     |      |
|                 |                                                                  |                             | 6 V             | 14                    |     | 20        |     | 17        |     |      |
|                 | $\overline{\text{G}}$ low                                        | 2 V                         | 80              |                       | 120 |           | 100 |           |     |      |
|                 |                                                                  | 4.5 V                       | 16              |                       | 24  |           | 20  |           |     |      |
|                 |                                                                  | 6 V                         | 14              |                       | 20  |           | 17  |           |     |      |
| t <sub>su</sub> | Setup time, data or address before $\overline{\text{G}}\uparrow$ |                             | 2 V             | 75                    |     | 115       |     | 95        |     | ns   |
|                 |                                                                  |                             | 4.5 V           | 15                    |     | 23        |     | 19        |     |      |
|                 |                                                                  |                             | 6 V             | 13                    |     | 20        |     | 16        |     |      |
| t <sub>h</sub>  | Hold time, data or address after $\overline{\text{G}}\uparrow$   |                             | 2 V             | 5                     |     | 5         |     | 5         |     | ns   |
|                 |                                                                  |                             | 4.5 V           | 5                     |     | 5         |     | 5         |     |      |
|                 |                                                                  |                             | 6 V             | 5                     |     | 5         |     | 5         |     |      |



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## 8-BIT ADDRESSABLE LATCHES

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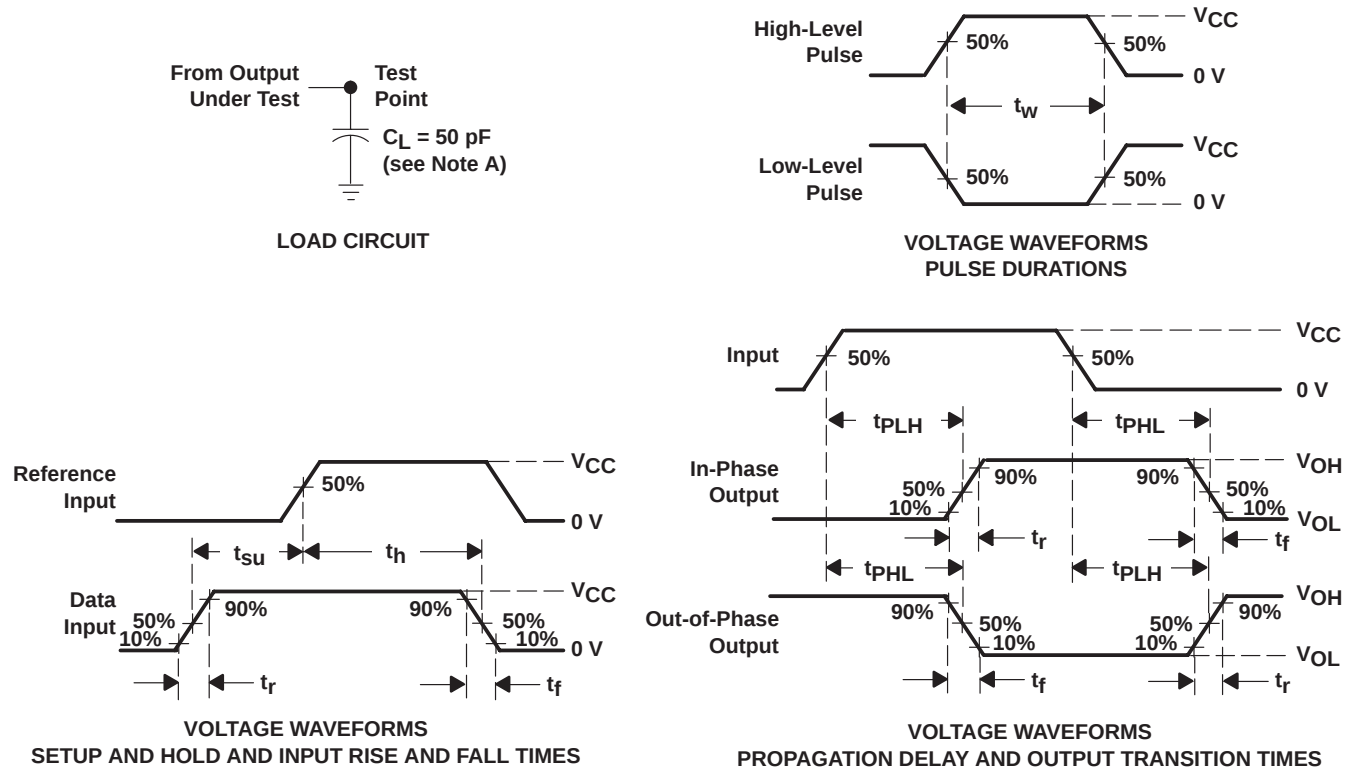
switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM<br>(INPUT)  | TO<br>(OUTPUT) | $V_{CC}$ | $T_A = 25^\circ\text{C}$ |     |     | SN54HC259 |     | SN74HC259 |     | UNIT |
|-----------|------------------|----------------|----------|--------------------------|-----|-----|-----------|-----|-----------|-----|------|
|           |                  |                |          | MIN                      | TYP | MAX | MIN       | MAX | MIN       | MAX |      |
| $t_{PHL}$ | $\overline{CLR}$ | Any Q          | 2 V      |                          | 60  | 150 |           | 225 |           | 190 | ns   |
|           |                  |                | 4.5 V    |                          | 18  | 30  |           | 45  |           | 38  |      |
|           |                  |                | 6 V      |                          | 14  | 26  |           | 38  |           | 32  |      |
| $t_{pd}$  | Data             | Any Q          | 2 V      |                          | 56  | 130 |           | 195 |           | 165 | ns   |
|           |                  |                | 4.5 V    |                          | 17  | 26  |           | 39  |           | 33  |      |
|           |                  |                | 6 V      |                          | 13  | 22  |           | 33  |           | 28  |      |
|           | Address          | Any Q          | 2 V      |                          | 74  | 200 |           | 300 |           | 250 |      |
|           |                  |                | 4.5 V    |                          | 21  | 40  |           | 60  |           | 50  |      |
|           |                  |                | 6 V      |                          | 17  | 34  |           | 51  |           | 43  |      |
|           | $\overline{G}$   | Any Q          | 2 V      |                          | 66  | 170 |           | 255 |           | 215 |      |
|           |                  |                | 4.5 V    |                          | 20  | 34  |           | 51  |           | 43  |      |
|           |                  |                | 6 V      |                          | 16  | 29  |           | 43  |           | 37  |      |
| $t_t$     |                  | Any            | 2 V      |                          | 28  | 75  |           | 110 |           | 95  | ns   |
|           |                  |                | 4.5 V    |                          | 8   | 15  |           | 22  |           | 19  |      |
|           |                  |                | 6 V      |                          | 6   | 13  |           | 19  |           | 16  |      |

operating characteristics,  $T_A = 25^\circ\text{C}$

| PARAMETER |                                         | TEST CONDITIONS | TYP | UNIT |
|-----------|-----------------------------------------|-----------------|-----|------|
| $C_{pd}$  | Power dissipation capacitance per latch | No load         | 33  | pF   |

## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and test-fixture capacitance.
  - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$ .
  - C. The outputs are measured one at a time with one input transition per measurement.
  - D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 85519012A        | ACTIVE                | LCCC         | FK              | 20   | 1           | TBD                     | POST-PLATE       | N / A for Pkg Type           |
| 8551901EA        | ACTIVE                | CDIP         | J               | 16   | 1           | TBD                     | A42 SNPB         | N / A for Pkg Type           |
| 8551901FA        | ACTIVE                | CFP          | W               | 16   | 1           | TBD                     | A42              | N / A for Pkg Type           |
| JM38510/65402BEA | ACTIVE                | CDIP         | J               | 16   | 1           | TBD                     | A42 SNPB         | N / A for Pkg Type           |
| SN54HC259J       | ACTIVE                | CDIP         | J               | 16   | 1           | TBD                     | A42 SNPB         | N / A for Pkg Type           |
| SN74HC259D       | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74HC259DE4     | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74HC259DR      | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74HC259DRE4    | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74HC259DT      | ACTIVE                | SOIC         | D               | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74HC259DTE4    | ACTIVE                | SOIC         | D               | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74HC259N       | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| SN74HC259NE4     | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| SN74HC259NSR     | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74HC259NSRE4   | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74HC259PWLE    | OBSOLETE              | TSSOP        | PW              | 16   |             | TBD                     | Call TI          | Call TI                      |
| SN74HC259PWR     | ACTIVE                | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74HC259PWRE4   | ACTIVE                | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74HC259PWT     | ACTIVE                | TSSOP        | PW              | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74HC259PWTE4   | ACTIVE                | TSSOP        | PW              | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SNJ54HC259FK     | ACTIVE                | LCCC         | FK              | 20   | 1           | TBD                     | POST-PLATE       | N / A for Pkg Type           |
| SNJ54HC259J      | ACTIVE                | CDIP         | J               | 16   | 1           | TBD                     | A42 SNPB         | N / A for Pkg Type           |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered

at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only.
  - Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - The terminals are gold plated.
  - Falls within JEDEC MS-004

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **             | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| DIM                 |                  |                  |                  |                  |
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

## D (R-PDSO-G16)

## PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-012 variation AC.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## PW (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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