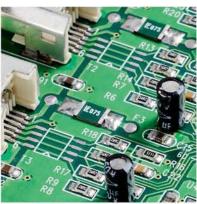




ESD PROTECTION GUIDE





System-Level and Application Specific Electrostatic Discharge (ESD) Protection Guide



SYSTEM-LEVEL AND APPLICATION SPECIFIC ESD PROTECTION GUIDE

Introduction:

Designers of today's electronic devices have demanded more functionality with greater flexibility and higher levels of user interaction. These circumstances have helped in driving the development of nanometer chipsets along with a multitude of user interfaces or ports. The confluence of these two has made electronic devices more susceptible to ESD and required the need for a more robust solution.

ESD Standards:

MIL-STD-883, Method 3015

Historically, analog and digital designers have been required to have ESD protection "on-chip" to protect the IC during manufacturing. The most commonly used ESD standard in the manufacturing environment is the MIL-STD-883, Method 3015 and it's also referred to as the Human Body Model (HBM). This model discharges a 100pF capacitor through a 1500 Ω resistor into the device under test. The table below points out the four test levels as defined in the standard.

HBM Level	Contact Discharge (kV)	Peak Current (A)
1	±0.5	0.33
2	±1	0.67
3	±2	1.33
4	±4	2.67

The maximum level required for a typical IC had been ±2kV up until 2007, but today that level has been drastically reduced to ±0.5kV. Obviously, this has helped chip designers save valuable silicon area for more functionality, but in turn, it has made the IC much more susceptible to damage from ESD.

IEC61000-4-2

Conversely, equipment manufacturers have traditionally used an ESD standard defined by the IEC (International Electrotechnical Commission) for system or application level testing. This model uses a 150pF capacitor which is discharged through a 330Ω resistor. The table below displays the four test levels as defined in the standard.

IEC Level	Contact Discharge (kV)	Peak Current (A)
1	±2	7.5
2	±4	15
3	±6	22.5
4	±8	30

Most all manufacturers require that their equipment pass Level 4, or $\pm 8 \text{kV}$, as a minimum, however, some are looking for increased reliability and require that their devices pass a much higher level like $\pm 15 \text{kV}$ or $\pm 30 \text{kV}$.

Conclusions:

The system level ESD test defined by the IEC produces a substantial increase in peak current compared to the military standard. If an IC is rated for 0.5kV per the MIL-STD and the equipment manufacturer tests this same IC at 8kV per the IEC specification, the chip will see nearly a 100 fold increase in peak current (i.e. 0.33A vs. 30A)!

Ultimately, hardware or board designers must add supplementary ESD devices to protect these sensitive chipsets from the high level ESD threats seen in the field.

Solutions:

Littelfuse's Silicon Protection Arrays are an ideal choice for suppressing ESD as their speed and clamping levels are essential to protect today's integrated circuits unlike the previous MLV, MOV, and polymer technologies. The SPATM portfolio offers a wide range of devices to suit the majority of application needs available in the market today, and this guide will steer the designer toward the appropriate ESD device for the particular application they're trying to protect.

Some of the applications discussed in this guide are:

- USB1.1/2.0/3.0
- HDMI
- DVI
- 10/100/1000 Ethernet
- eSATA
- 1394a/b
- LVDS
- Audio (Speaker/Microphone)
- Analog Video
- SIM Sockets
- RS-232
- RS-485
- CAN Bus
- Keypad/Push button
- LCD/Camera display interfaces

Many of these applications can be found in electronic devices such as:

PC's

- MP3/PMP's
- Portable Medical Devices
- PDA's
- Set Top Boxes
- Digital Cameras
- LCD/PDP TV's
- SIM/SD Cards
- Portable Navigation Devices
- External Storage
- Keyboards/Mouse
- Router/Hub/Modem
- Mobile Handsets
- Smart Phone



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Unidirectional and Bidirectional TVS Arrays for ESD Protection

Series	Schematic (Example)	ESD Level (Contact)	I/O Cap V _R = 0V (@ Bias)	V _{RWM}	Lightning (t _P =8/20μs)	Number of Channels	Package Options		
	1/0 1/0					2	S0T23-3 SC70-3		
	L L					3	S0T143		
SP05		±30kV	50pF (30pF @ 2.5V)	5.5V	N/A	4	S0T23-5 SC70-5		
	* *		(000) © 2.017			5	SOT23-6 SC70-6		
	o <u>†</u> o 1/0					6	MSOP-8		
	1/0 1/0					2	SC70-3 SOT553		
SP1001		±15kV	12pF (8pF @ 2.5V)	12pF (8pF @ 2.5V)	5.5V	2A	4	SC70-5 SOT553	
						5	SC70-6 SOT563		
SP1002	1/O	±8kV	6pF	6pF	6pF	6pF @ 3 F.V. 6V	6V 2A	1	SC70-3
31 1002	WO 1/0	TUNV	(5pF @ 2.5V)	UV	ZA	2	SC70-5		
SP1003	1/O - -	±25kV	30pF (17pF @ 2.5V)	5V	7A	1	SOD723		



Unidirectional and Bidirectional TVS Arrays for ESD Protection (continued)

Series	Schematic (Example)	ESD Level (Contact)	I/O Cap V _R = 0V (@ Bias)	V _{RWM}	Lightning (t _P =8/20μs)	Number of Channels	Package Options
SP1004	1/0 1/0 1/0 1/0 GND	±8kV	6pF (5pF @ 1.5V)	6V	2A	4	S0T953
SP1005	10 0 1 0 10	±30kV	30pF (23pF @ 2.5V)	6V	10A	1	0201 Flipchip
SP1007	1/0 1 1 1 1 1 1 1 1 1 1	±8kV	5pF (3.5pF @ 5V)	6V	2A	1	0201 Flipchip
SP1010	1/0	±8kV	6pF (3.5pF @ 2.5V)	6V	1A	4	μDFN-6 1.25x1.0mm
SP1011	1/0	±15kV	12pF (7pF @ 2.5V)	6V	2A	4	μDFN-6 1.25x1.0mm



Low Capacitance Diode Arrays for ESD Protection

Series	Schematic (Example)	ESD Level (Contact)	I/O Cap V _R = 1.65V	V _{RWM}	Lightning (t _P =8/20µs)	Number of Channels	Package Options
SP3001	V/O V/O V/O V/O	±8kV	0.65pF	6V	2.5A	4	SC70-6
SP3002	1/0 Vcc 1/0 1/0	±12kV	0.85pF	6V	4.5A	4	SC70-6 SOT23-6 μDFN-6 1.6x1.6mm
SP3003	/O /O /O /O	±8kV	0.65pF	6V	2.5A	2	SC70-5 SOT553
	* * *					4	SC70-6 SOT563 MSOP-10
SP3004	NO NO NO	±12kV	0.85pF	6V	4A	4	SOT563



Low Capacitance Diode Arrays for ESD Protection (continued)

Series	Schematic (Example)	ESD Level (Contact)	I/O Cap V _R = 0V	V_{RWM}	Lightning (t _P =8/20μs)	Number of Channels	Package Options
SP3010	1/0 1/0 1/0 1/0	±8kV	0.45pF	6V	3A	4	μDFN-10 2.5x1.0mm
SP3011	1/0 o	±8kV	0.40pF	6V	3A	6	μDFN-14 3.5x1.35mm
SP3050	/O /O /O /O	±20kV	2.4pF	6V	10A	4	S0T23-6
SP4060		±30kV	4.4pF	2.5V	20A	8	MSOP-10



Low Capacitance Diode Arrays for Broadband Protection

Series	Schematic (Example)	ESD Level (Contact)	I/O Cap V _R = 0V	V _{RWM}	Lightning (t _P =8/20μs)	Number of Channels	Package Options
SP03-3.3	Line in Line out	±30kV	16pF	3.3V	150A	2	SOIC-8
SP03-6	Line in Line out	±30kV	16pF	6V	150A	2	SOIC-8
SPLV2.8	3 V V O 1	±30kV	3.8pF	2.8V	24A	1	S0T23-3
SPLV2.8-4	VO 1 0 VO 1 VO 2 VO 3 VO 3 VO 4	±30kV	3.8pF	2.8V	24A	4	SOIC-8



EMI Filter Arrays with ESD Protection

Series	Schematic (Example)	ESD Level (Contact)	Line Cap (V _R =2.5V)	V _{RWM}	Attenuation	Number of Channels	Package Options
						4	μDFN-8 1.7x1.35mm
SP6001		±30kV	24pF (C _{DIODE} =12pF)	6V	≥ -30dB @ 1GHz	6	μDFN-12 2.5x1.35mm
						8	μDFN-16 3.3x1.35mm
000000	5002 ±30kV	30pF	30pF	≥ -30dB @	4	μDFN-8 1.7x1.35mm	
SP6002		±3UkV	(CDIODE=15pF)	6V	1GHz	6	μDFN-12 2.5x1.35mm
SP6003		±15kV	14pF	61/	≥ -20dB @ 1GHz	4	μDFN-8 1.7x1.35mm
31 0003			(C _{DIODE} =7pF)	6V		6	μDFN-12 2.5x1.35mm



SCR/Diode Arrays for ESD Protection

Series	Schematic (Example)	ESD Level (Contact)	I/O Cap	V _{RWM}	Lightning (t _P =8/20μs)	Number of Channels	Package Options
SP720	V+0	±4kV	3pF	30V or (±15V)	3A	14	SOIC-16 PDIP-16
SP721	V+0	±4kV	3pF	30V or (±15V)	3A	6	SOIC-8 PDIP-8
SP723	V+0	±8kV	5pF	30V or (±15V)	7A	6	SOIC-8 PDIP-8
SP724	V+0	±8kV	3pF	20V or (±10V)	3A	4	SOT23-6
SP725	V+0	±8kV	5pF	30V or (±15V)	14A	4	SOIC-8





Silicon Protection Array Ordering Guide

Series	Number of Channels	Package	Orderable Part Number
	2	S0T23-3	SP0502BAHTG
		SC70-3	SP0502BAJTG
	3	S0T143	SP0503BAHTG
SP05	4	S0T23-5	SP0504BAHTG
0100	<u>'</u>	SC70-5	SP0504BAJTG
	5	S0T23-6	SP0505BAHTG
	J	SC70-6	SP0505BAJTG
	6	MSOP-8	SP0506BAATG
	2	SC70-3	SP1001-02JTG
	Z	S0T553	SP1001-02XTG
004004		SC70-5	SP1001-04JTG
SP1001	4	SOT553	SP1001-04XTG
		SC70-6	SP1001-05JTG
	5	SOT56	SP1001-05XTG
004000	1	SC70-3	SP1002-01JTG
SP1002	2	SC70-5	SP1002-02JTG
SP1003	1	SOD723	SP1003-01DTG
SP1004	4	S0T953	SP1004-04VTG
SP1005	1	0201 Flipchip	SP1005-01WTG
SP1007	1	0201 Flipchip	SP1007-01WTG
SP1010	4	μDFN-6 (1.25x1.0mm)	SP1010-04UTG
SP1011	4	μDFN-6 (1.25x1.0mm)	SP1011-04UTG
SP3001	4	SC70-6	SP3001-04JTG
		S0T23-6	SP3002-04HTG
SP3002	4	SC70-6	SP3002-04JTG
		μDFN-6 (1.6x1.6mm)	SP3002-04UTG
		SC70-5	SP3003-02JTG
	2	S0T553	SP3003-02XTG
SP3003		SC70-6	SP3003-04JTG
	4	SOT563	SP3003-04XTG
		MSOP-10	SP3003-04ATG
SP3004	4	SOT563	SP3004-04XTG
SP3010	4	μDFN-10 (2.5x1.0mm)	SP3010-04UTG
SP3011	6	μDFN-14 (3.5x1.35mm)	SP3011-06UTG



SYSTEM-LEVEL AND APPLICATION SPECIFIC ESD PROTECTION GUIDE

Silicon Protection Array Ordering Guide (continued)

Series	Number of Channels	Package	Orderable Part Number
SP3050	4	SOT23-6	SP3050-04HTG
SP4060	8	MSOP-10	SP4060-08ATG
SP03-3.3	2	SOIC-8	SP03-3.3BTG
SP03-6	2	SOIC-8	SP03-6BTG
SPLV2.8	1	SOT23-3	SPLV2.8HTG
SPLV2.8-4	4	SOIC-8	SPLV2.8-4BTG
	4	μDFN-8 (1.7x1.35mm)	SP6001-04UTG-1
SP6001	6	μDFN-12 (2.5x1.35mm)	SP6001-06UTG-1
	8	μDFN-16 (3.3x1.35mm)	SP6001-08UTG-1
SP6002	4	μDFN-8 (1.7x1.35mm)	SP6002-04UTG-1
370002	6	μDFN-12 (2.5x1.35mm)	SP6002-06UTG-1
SP6003	4	μDFN-8 (1.7x1.35mm)	SP6003-04UTG-1
370003	6	μDFN-12 (2.5x1.35mm)	SP6003-06UTG-1
SP720	14	PDIP-16	SP720APP
35720	14	SOIC-16	SP720AB*G
SP721	6	PDIP-8	SP721APP
37/21	6	SOIC-8	SP721AB*G
SP723	6	PDIP-8	SP723APP
SF/23	6	SOIC-8	SP723AB*G
SP724	4	SOT23-6	SP724AHTG
SP725	4	SOIC-8	SP725AB*G

^{*}Add "T" for Tape and Reel, otherwise parts are packed in tubes

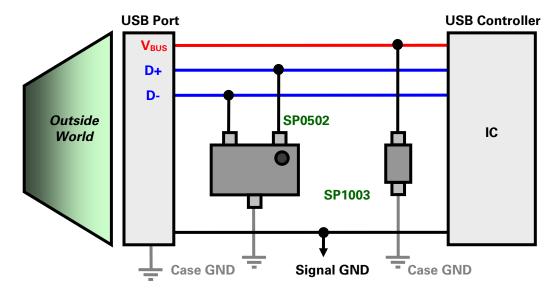


USB1.1

Considerations:

- Each port operates at either 1.5Mbps or 12Mbps (low and full speed respectively)
 - · Parasitic capacitance should be taken into account although these relatively slow speeds can tolerate tens of picofarads
- Requires 2 channels of data line protection per port (i.e. D±)
 - · A 4 channel device can be useful if protecting a USB stack of 2 ports to make the ESD footprint as small as possible
 - V_{BUS} can be protected separately with a single channel device (0402 shown)

Application Schematic:



Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	I/O Capacitance @ V _R =2.5V	# of Channels	V _{RWM}	Packaging
SP0502BAJTG	±30kV	30pF	2	5.5V	SC70-3
SP1001-02XTG	±15kV	8pF	2	5.5V	S0T553
SP1001-04XTG	±15kV	8pF	4	5.5V	S0T553
SP1003-01DTG	±25kV	17pF	1	5.0V	S0D723

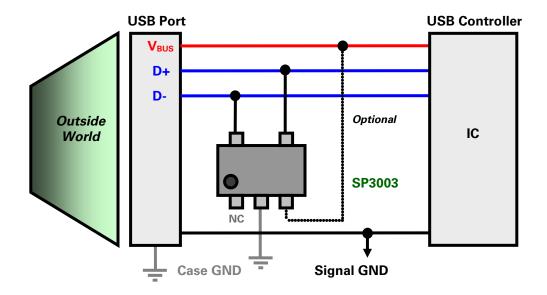


USB2.0

Considerations:

- Each port can operate up to 480Mbps
 - The high data rate requires a low capacitance device to preserve signal integrity
- Requires 2 channels of data line protection per port (i.e. D±)
 - · A 4 channel device can be useful if protecting a USB stack of 2 ports to make the ESD footprint as small as possible
 - V_{BUS} can be protected by connecting it to the VCC pin on the diode array or by using a separate single channel device as previously shown (i.e. SP1003)

Application Schematic:



Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	I/O Capacitance @ V _R =1.65V	# of Channels	V _{RWM}	Packaging
SP3003-02XTG	±8kV	0.65pF	2	6V	S0T553
SP3003-02JTG	±8kV	0.65pF	2	6V	SC70-5
SP3002-04UTG	±12kV	0.85pF	4	6V	μDFN-6 (1.6x1.6mm)
SP3002-04JTG	±12kV	0.85pF	4	6V	SC70-6

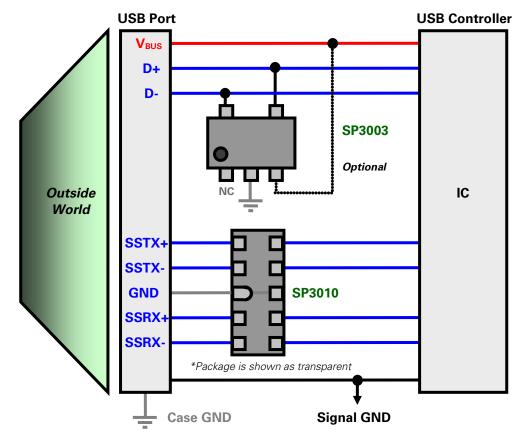


USB3.0 (Two Device Solution)

Considerations:

- Each port depending upon what it's connected to can operate:
 - Up to 5Gbps over the new super-speed data pairs, SSTX± and SSRX±
 - Up to 480Mbps on the legacy data pair, D±
- Requires 4 channels of ultra-low capacitance protection for the super-speed data pair (i.e. SSTX± and SSRX±)
- Requires 2 channels of protection for the legacy D± data pair
 - VBUS can be protected by connecting it to the VCC pin on the SPA or by using a separate single channel device

Application Schematic:



Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	I/O Capacitance @ V _R =1.65V	# of Channels	V _{RWM}	Packaging
SP3003-02XTG	±8kV	0.65pF	2	6V	S0T553
SP3010-04UTG	±8kV	0.45pF	4	6V	μDFN-10

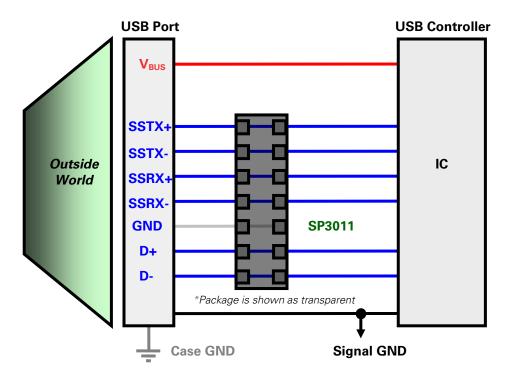


USB3.0 (Fully Integrated Solution)

Considerations:

- Each port depending upon what it's connected to can operate:
 - Up to 5Gbps over the new super-speed data pairs, SSTX± and SSRX±
 - Up to 480Mbps on the legacy data pair, D±
- Requires 4 channels of ultra-low capacitance protection for the super-speed data pair (i.e. SSTX± and SSRX±) and 2 channels of protection for the legacy D± data pair. The SP3011 shown below integrates all 6 channels of protection into a small form factor µDFN-14 package.

Application Schematic:



Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	I/O Capacitance @ V _R =0V	# of Channels	V_{RWM}	Packaging
SP3011-06UTG	±8kV	0.40pF	6	6V	μDFN-14

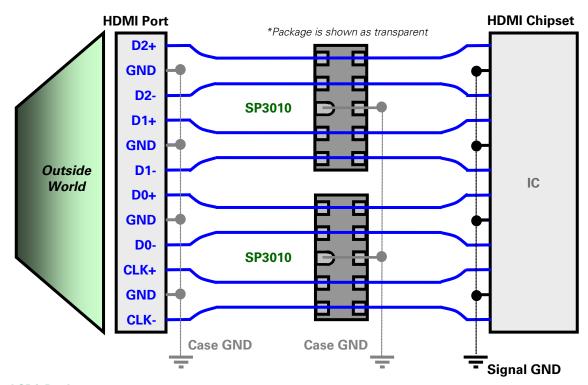


HDMI

Considerations:

- Each port has 3 differential lanes of data (i.e. D0±, D1±, D2±) plus a clock (CLK±)
 - For HDMI 1.1-1.2 the throughput is a total of 4.95Gbps (1.65Gbps per lane)
 - For HDMI 1.3 the throughput is a total of 10.2Gbps (3.4Gbps per lane)
- To maintain the differential impedance per the HDMI Compliance Test Specification (and consequently signal integrity) a very low capacitance device must be used
- To maintain the differential impedance the designer should avoid using 90° angles and vias
 - This can be accomplished by the use of an ESD device that offers a "straight-through" routing scheme
- Requires 8 channels of protection per port (D0±, D1±, D2±, CLK±)
- \bullet The V_{CC} pin on the SP3003-04ATG should be "NC" if backdrive is a concern. There is no V_{CC} pin on the SP3010-04UTG

Application Schematic:



Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	I/O Capacitance @ V _R =1.65V	# of Channels	V _{RWM}	Packaging
SP3010-04UTG	±8kV	0.45pF	4	6V	μDFN-10
SP3003-04ATG	±8kV	0.65pF	4	6V	MSOP-10

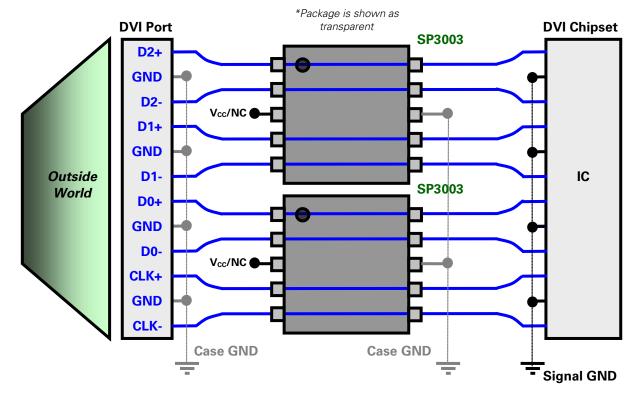


DVI

Considerations:

- A DVI port may have single or dual link capability
 - Each link has 3 differential lanes of data (i.e. D0±, D1±, D2±) plus a clock (CLK±)
 - For single link, the maximum throughput can approach a total of 4.95Gbps or 1.65Gbps per lane
 - For dual link, the maximum throughput can approach a total of 8Gbps or 2.67Gbps per lane
- To maintain signal integrity a very low capacitance device must be used
- To maintain the differential impedance the designer should avoid using 90° angles and vias
 - This can be accomplished by the use of an ESD device that offers a "straight-through" routing scheme
- Requires 8 channels of protection per port (D0±, D1±, D2±, CLK±)

Application Schematic:



Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	I/O Capacitance @ V _R =1.65V	# of Channels	V _{RWM}	Packaging
SP3003-04ATG	±8kV	0.65pF	4	6V	MSOP-10
SP3010-04UTG	±8kV	0.45pF	4	6V	μDFN-10

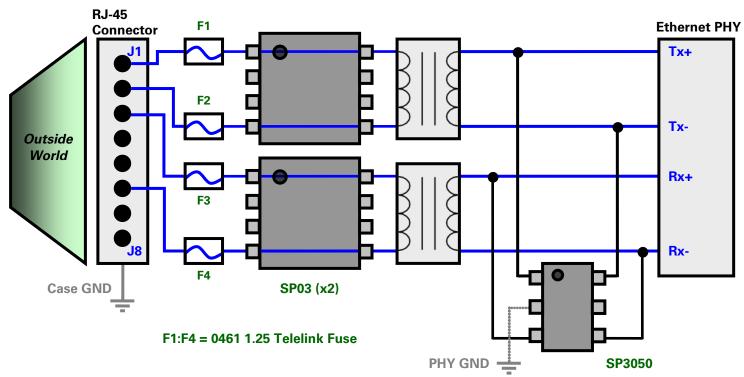


10/100/1000 Ethernet, Intra-building Lighting Immunity (GR-1089)

Considerations:

- 10/100/1000 relates to the data rate in Mbps (i.e. 10Mbps, 100Mbps, and 1000Mbps)
 - For 10 Base-T, data is transmitted over 2 UTP (unshielded twisted pairs) using a 10MHz clock
 - For 100 Base-TX, data is transmitted over 2 UTP using a 125MHz clock
 - For 1000 Base-T data is transmitted over 4 UTP using a 125MHz clock
 - For these data rates the parasitic capacitance needs to be taken into account to preserve signal integrity
- The 4 data lines below (Tx± and Rx±) are being protected against intra-building (i.e. 100A, t_P=2/10μs) lightning transients by a two-stage protection scheme
- 1000Mbps Ethernet (or 1GbE) will require 8 channels of protection for the 4 differential pair so the below scheme should be replicated for the remaining 2 data pair

Application Schematic:



Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	Lightning (t _P =8/20μs)	I/O Capacitance @ V _R =0V	# of Channels	V _{RWM}	Packaging
SP03-xBTG	±30kV	150A	8pF (I/O to I/O)	2	3.3V,6V	SOIC-8
SP3050-04HTG	±20kV	10A	2.4pF	4	6V	S0T23-6

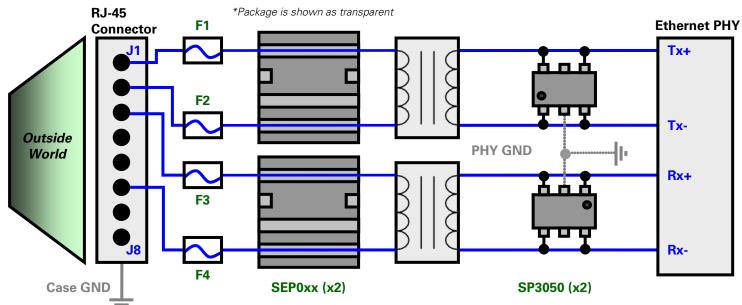


10/100/1000 Ethernet, Inter-building Lighting Immunity (GR-1089)

Considerations:

- 10/100/1000 relates to the data rate in Mbps (i.e. 10Mbps, 100Mbps, and 1000Mbps)
 - For 10 Base-T, data is transmitted over 2 UTP (unshielded twisted pairs) using a 10MHz clock
 - For 100 Base-TX, data is transmitted over 2 UTP using a 125MHz clock
 - For 1000 Base-T data is transmitted over 4 UTP using a 125MHz clock
 - For these data rates the parasitic capacitance needs to be taken into account to preserve signal integrity
- The 4 data lines below are being protected against inter-building (i.e. 500A, tp=2/10µs) lightning transients by a two-stage protection scheme. The 8 channel, SP4060 can be used in place of the SP3050 if a lower clamping and higher surge rated device is needed.
- The standoff voltage of the SEP Series device will be dictated by the use of PoE. If PoE is present the SEP0640 should be used; otherwise, the SEP0080 is ok for non-PoE applications. *Note: Higher voltage options are available for atypical PoE voltages.*
- 1000Mbps Ethernet (or 1GbE) will require 8 channels of protection for the 4 differential pair so the below scheme should be replicated for the remaining 2 data pair

Application Schematic:



F1:F4 = 0461 1.25 Telelink Fuse

Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	Lightning (t _P =8/20μs)	I/O Capacitance @ V _R =0V	# of Channels	V _{RWM}	Packaging
SEP0080Q38CB	±30kV	400A	See datasheet	2	6V	QFN
SEP0640Q38CB	±30kV	400A	See datasheet	2	58V	QFN
SP3050-04HTG	±20kV	10A	2.4pF	4	6V	S0T23-6
SP4060-08ATG	±30kV	20A	4.4pF	8	2.5V	MSOP-8

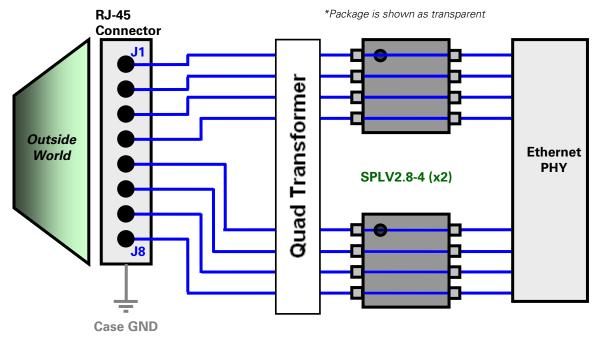


10/100/1000 Ethernet, General Lighting Immunity (GR-1089)

Considerations:

- 10/100/1000 relates to the data rate in Mbps (i.e. 10Mbps, 100Mbps, and 1000Mbps)
 - For 10 Base-T, data is transmitted over 2 UTP (unshielded twisted pairs) using a 10MHz clock
 - For 100 Base-TX, data is transmitted over 2 UTP using a 125MHz clock
 - For 1000 Base-T data is transmitted over 4 UTP using a 125MHz clock
 - For these data rates the parasitic capacitance needs to be taken into account to preserve signal integrity
- Some designers choose to use a robust transformer in their design to act as the first line of protection against an incoming surge event. This is usually done to minimize the parasitic capacitance on the data line and to save on the cost of the primary protector
- Using such a technique will require a robust PHY side protection device and one such option is the SPLV2.8-4 shown below. It should be noted that this device will only provide differential protection between the data pairs
- If longitudinal and differential protection are required, the SP3050-04HTG (with 2 I/O's tied per line) or SP4060-08ATG can be considered as alternatives
- Protection for 1000Mbps Ethernet (or 1GbE) is shown below. For 10 or 100Mbps interfaces only 1 SPLV2.8-4BTG is required

Application Schematic:



Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	Lightning (t _P =8/20μs)	I/O Capacitance @ V _R =0V	# of Channels	V_{RWM}	Packaging
SPLV2.8-4BTG	±30kV	24A	3.8pF	4	2.8V	SOIC-8
SP3050-04HTG	±20kV	10A	2.4pF	4	6V	S0T23-6
SP4060-08ATG	±30kV	20A	4.4pF	8	2.5V	MSOP-8

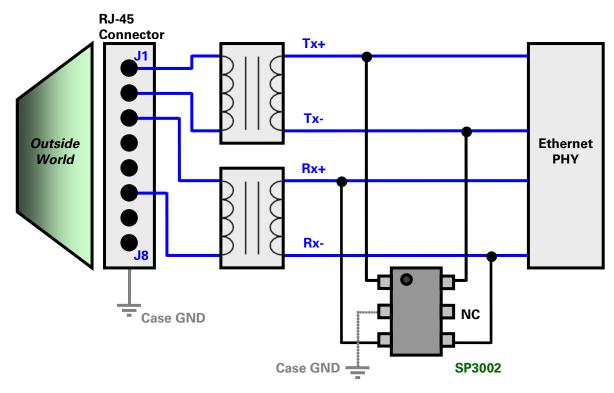


10/100/1000 Ethernet (ESD only)

Considerations:

- Some Ethernet ports only need be protected for ESD and not for lightning induced transients
 - These are sometimes referred to as "2M" ports or 2 Meter ports that have very short CAT5 cable installations
- Parasitic capacitance should be taken into account especially for 1GbE
- The 4 data lines below (Tx± and Rx±) are being protected against ESD by a low capacitance SP3002 which is suitable for all Ethernet data rates
 - In fact, any low capacitance SP30xx device is suitable for any "ESD only" Ethernet application
- 1000Mbps Ethernet (or 1GbE) will require 8 channels of protection for the 4 differential pair so the below scheme should be replicated for the remaining 2 data pair

Application Schematic:



Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	Lightning (t _P =8/20μs)	I/O Capacitance @ V _R =1.65V	# of Channels	V _{RWM}	Packaging
SP3002-04JTG	±12kV	4.5A	0.85pF	4	6V	SC70-6
SP3003-04XTG	±8kV	2.5A	0.65pF	4	6V	S0T563
SP3004-04XTG	±12kV	4A	0.85pF	4	6V	S0T563

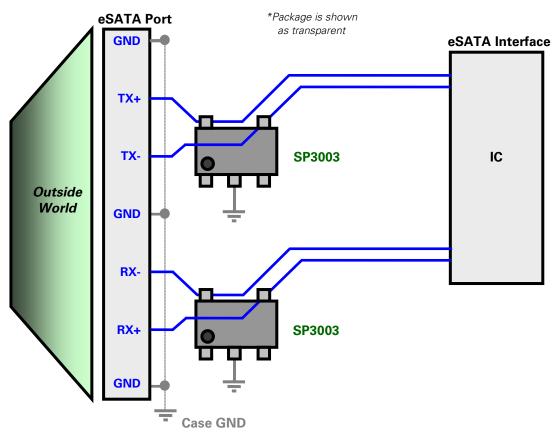


eSATA

Considerations:

- eSATA is a subset of the SATA protocol that uses 2 differential pairs for communication
 - Four lines need to be protected per port (i.e. TX± and RX±)
 - Currently eSATA is capable of running raw data rates of 1.5Gbps (Gen 1) and 3.0Gbps (Gen 2)
- These high bus speeds require very low capacitance devices to prevent signal degradation
- To maintain the line impedance the designer should avoid using 90° angles and vias

Application Schematic:



Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	I/O Capacitance @ V _R =1.65V	# of Channels	V _{RWM}	Packaging
SP3003-02XTG	±8kV	0.65pF	2	6V	S0T553
SP3003-04JTG	±8kV	0.65pF	4	6V	SC70-6
SP3010-04UTG	±8kV	0.45pF	4	6V	μDFN-10



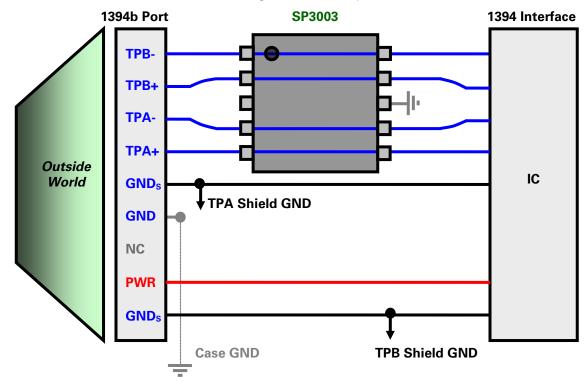
1394a/b

Considerations:

- 1394a (FireWire 400 or S400) was the original (1st generation) implementation
 - Allowed for two connectors, powered (6 pin) and unpowered (4 pin)
 - Data rates up to 400Mbps using 2 differential pair
- 1394b (FireWire 800 or S800) was the 2nd generation
 - Required a new 9 pin connector but was backwards compatible to S400
 - Data rates up to 800Mbps using 2 differential pair
- 1394b also had provisions for 1600Mbps and 3200Mbps (or S1600 and S3200)
 - Uses same 9 pin connector as \$800
- \$800, \$1600, and \$3200 require very low capacitance devices for the high speed data rates
 - Protection of 4 data lines is needed (i.e. TPB± and TPA±)

Application Schematic:

*Package is shown as transparent



Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	I/O Capacitance @ V _R =1.65V	# of Channels	V _{RWM}	Packaging
SP3003-04ATG	±8kV	0.65pF	4	6V	MSOP-10
SP3010-04UTG	±8kV	0.45pF	4	6V	μDFN-10

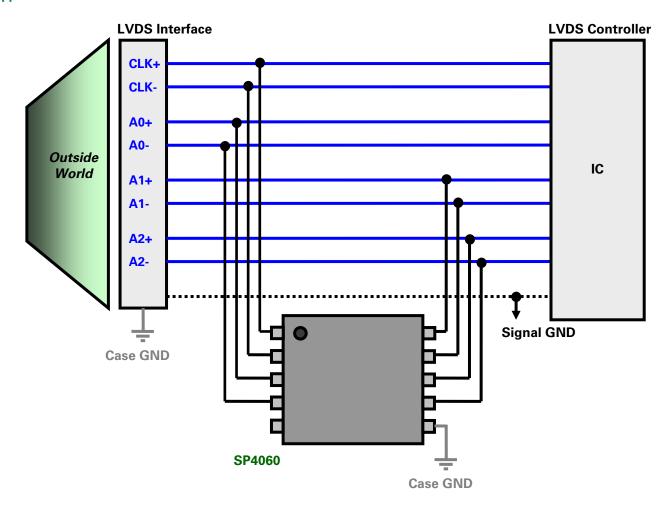


LVDS (Low Voltage Differential Signaling)

Considerations:

- LVDS is a low noise, low-voltage signal scheme that uses a small current (typically 3.5mA) to generate a voltage drop across a 100Ω resistor to convey information or data
 - Data rates can vary per application but the ANSI/TIA/EIA-644-A standard recommends a maximum of 655Mbps
- The medium/high speed bus requires a low capacitance device in 1-6pF range (typically)
 - · LVDS schemes will vary in terms of the total number of channels used
 - Protection of 8 data lines is shown below (i.e. CLK± and Ax±)

Application Schematic:



Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	Lightning (t _P =8/20µs)	I/O Capacitance @ V _R =0V	# of Channels	V _{RWM}	Packaging
SP4060-08ATG	±30kV	20A	4.4pF	8	2.5V	MSOP-10
SP3050-04HTG	±20kV	10A	2.4pF	4	6V	S0T23-6

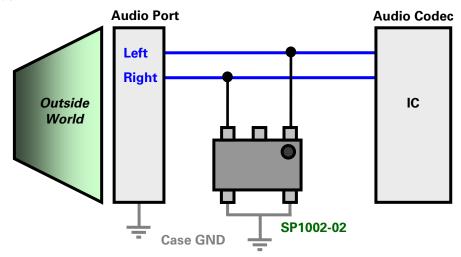


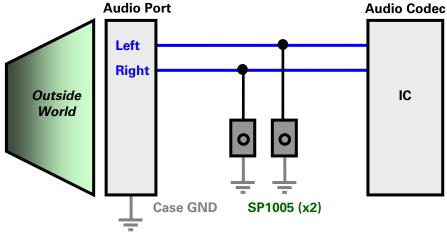
Audio (Speaker/Microphone)

Considerations:

- Audio ports typically have signals that swing above and below GND (i.e. ±2.5V)
 - If no DC bias is applied, a bidirectional protection device should be used as these devices will not clip the analog signal
 - · Protection of 2 data lines is shown below (i.e. Left and Right) with an array and with discrete 0201s
- Some audio ports will bias the data bus so that the signal never swings below GND (i.e. 0-5V)
 - If a bias is applied, a unidirectional OR bidirectional protection device could be used as neither device would clip the analog signal
 - The SP1001-02XTG is a good option in this case (not shown for Left and Right but is listed below)

Application Schematic:





Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	Lightning (t _P =8/20μs)	I/O Capacitance @ V _R =2.5V	# of Channels	V_{RWM}	Packaging
SP1002-02JTG	±8kV	2A	5pF	2	6V	SC70-5
SP1005-01WTG	±30kV	10A	23pF	1	6V	0201 Flipchip
SP1001-02XTG	±15kV	2A	8pF	2	5.5V	S0T553

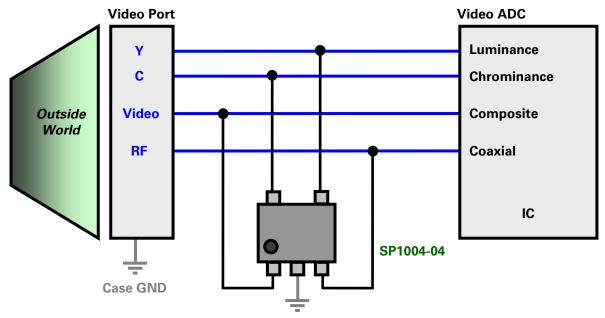


Analog Video

Considerations:

- Analog video ports typically have signals that swing above and below GND (i.e. ±2V)
 - · A bidirectional protection device should be used as these devices will not clip the analog signal
- S-Video, Composite, and RF/Coaxial are a few of the common low-speed analog video signals in use today
 - Typical bus speeds will not exceed 5MHz so capacitance is not much of a concern
 - Protection of the three are shown below (Y, C, Video, and RF)

Application Schematic:



Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	Lightning (t _P =8/20µs)	I/O Capacitance @ V _R =2.5V	# of Channels	V _{RWM}	Packaging
SP1004-04VTG	±8kV	2A	4.5pF	4	6V	S0T953
SP1002-01JTG	±8kV	2A	5pF	1	6V	SC70-3
SP1002-02JTG	±8kV	2A	5pF	2	6V	SC70-5
SP1005-01WTG	±30kV	10A	23pF	1	6V	0201 Flipchip
SP1007-01WTG	±8kV	2A	3.5pF	1	6V	0201 Flipchip

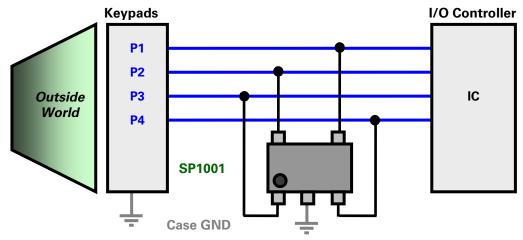


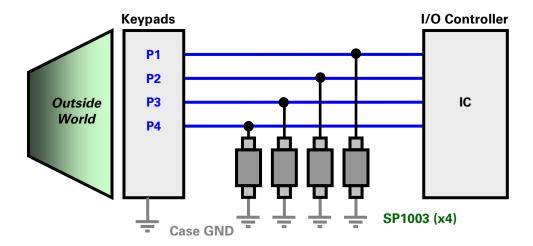
Keypad/Push Buttons

Considerations:

- Keypads and push buttons on electronic devices are particularly susceptible to ESD due to constant human interaction
 - · Most are DC switches that operate at less than 5V, and for most applications capacitance will not be a concern
- The number of ports will vary with the particular application, but as an example, 4 data lines are shown below (i.e.Px)
- For space constrained applications the SP1003 or SP1005 may be considered as they are 0402 and 0201 footprints, respectively

Application Schematics:





Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	Lightning (t _P =8/20µs)	I/O Capacitance @ V _R =2.5V	# of Channels	V _{RWM}	Packaging
SP1001-04XTG	±15kV	2A	8pF	4	6V	S0T553
SP1003-01DTG	±25kV	7A	17pF	1	5V	S0D723
SP1005-01WTG	±30kV	10A	23pF	1	6V	0201 Flipchip

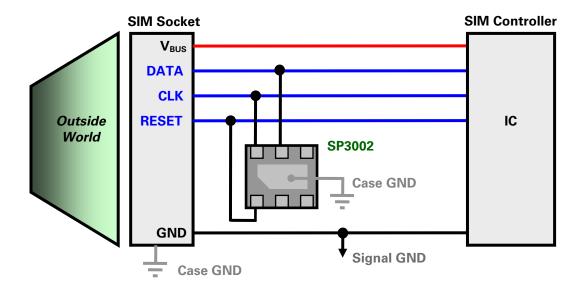


SIM Socket

Considerations:

- The SIM (Subscriber Identification Module) card has 3 data lines that are low-speed and low-voltage
 - Given the low speed of the signals, the capacitance will not be a concern
- The low-voltage signal lines are best protected by a device which has a low standoff voltage or V_{RWM}
- Protection of the 3 data lines is shown below (i.e. CLK, DATA, and RESET)

Application Schematics:



Recommended SPA Devices:

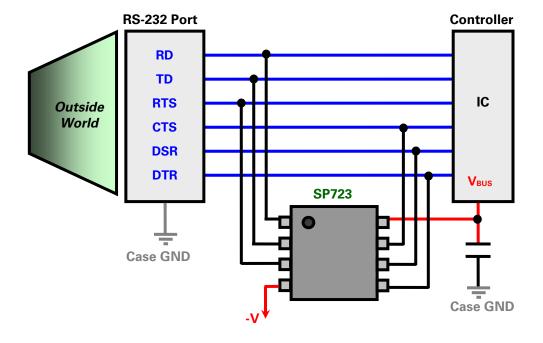
Ordering Number	ESD Level (Contact)	Lightning (t _P =8/20μs)	I/O Capacitance @ V _R =1.65V	# of Channels	V _{RWM}	Packaging
SP3002-04UTG	±12kV	4.5A	0.85pF	4	6V	μDFN-6 (1.6x1.6mm)
SP1011-04UTG	±15kV	2A	7pF	4	6V	μDFN-6 (1.25x1.0mm)



RS-232

Considerations:

- There are numerous implementations of RS-232
 - Most involve 6 wires (as shown below) though some may only include 2, 3, or 5 wires
- The maximum data rate is 20kbps
- Typically bus voltages are bipolar and can swing as high as ±24V though most installations are limited to ±12V or even lower
- For ±12V systems the SP72x Series is recommended and shown below
- Some implementations are a unipolar (i.e. 0-3.3V or 0-5V) or use bus voltages generally below 6V
 - In this event the SP1001 Series can be used for ESD protection or the SP03 Series could be used if lightning is the primary threat
- Every application should be evaluated thoroughly before using the recommended devices below



Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	Lightning (t _P =8/20μs)	I/O Capacitance @ V _R =1.65V	# of Channels	V _{RWM}	Packaging
SP721ABTG	±4kV	3A	3pF	6	30V	SOIC-8
SP723ABTG	±8kV	7A	5pF	6	30V	SOIC-8
SP724AHTG	±8kV	3A	3pF	4	20V	S0T23-6
SP725ABTG	±8kV	14A	5pF	4	30V	SOIC-8

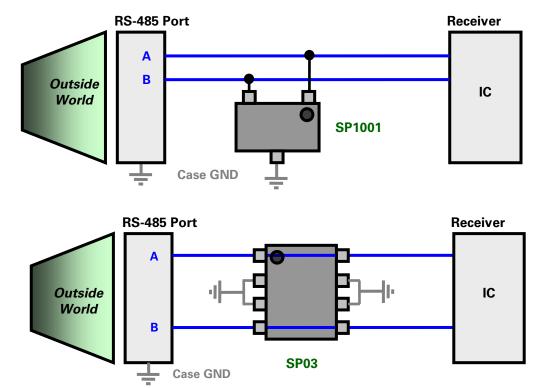


RS-485

Considerations:

- There are numerous implementations and applications of RS-485
 - Most applications involve two wires (i.e. A and B) while a few are four wire (i.e. full duplex)
 - Depending on cable length, data rates can vary from 100kbps-10Mbps
 - Bus voltages can be unipolar (i.e. 0-6V) or bipolar (i.e. ±3V) and every application should be evaluated thoroughly before using the recommended devices below
- For a unipolar bus with a voltage ≤ 6V (MAX):
 - The SP1001 Series is shown for ESD protection only
 - The SP03 Series is shown for lightning/surge protection
- For differential protection between A and B, the GND connection can be removed from the schematics below
- For a bipolar bus with a maximum voltage swing of ±3V:
 - The SP1002 or SP1004 Series can be used ESD protection only
 - The SP03 Series (x2) can still be used for lightning/surge protection with one I/O tied to GND

Application Schematic:



Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	Lightning (t _P =8/20μs)	I/O Capacitance @ V _R =2.5V/0V	# of Channels	V _{RWM}	Packaging
SP1001-02JTG	±15kV	2A	8pF	2	6V	SC70-3
SP03-xBTG	±30kV	150A	16pF	2	3.3V, 6V	SOIC-8

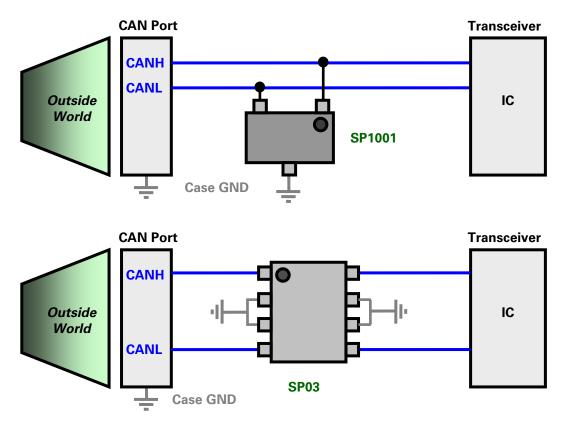


CAN Bus

Considerations:

- There are numerous implementations and applications of a CAN bus
 - Most applications involve two wires (i.e. CANH and CANL)
 - Depending on cable length, data rates can vary from 10kbps-1Mbps
 - Most applications do not exceed 0-5V to transmit a Low/High signal, however, every application should be evaluated thoroughly before using the recommended devices below
- For the described application of unipolar bus with voltages between 0 and 5V:
 - The SP1001 Series is shown for ESD protection only
 - The SP03 Series is shown for lightning/surge protection
- For differential protection between CANH and CANL, the GND connection can be removed from the schematics below

Application Schematic:



Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	Lightning (t _P =8/20μs)	I/O Capacitance @ V _R =2.5V/0V	# of Channels	V _{RWM}	Packaging
SP1001-02JTG	±15kV	2A	8pF	2	6V	SC70-3
SP03-xBTG	±30kV	150A	16pF	2	3.3V, 6V	SOIC-8

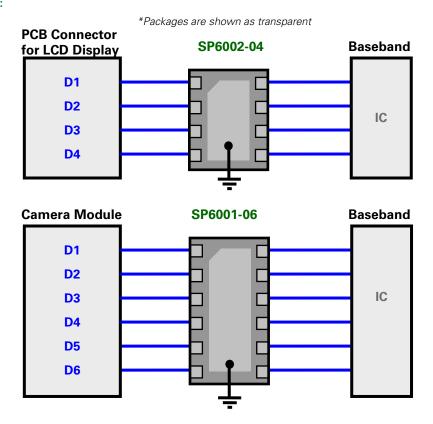


LCD and Camera Interfaces (Mobile)

Considerations:

- LCD and camera interfaces in mobile devices are vulnerable to EMI from the cellular band
 - Frequencies between 800-3000MHz should be attenuated to prevent distortion on the display
- The pixel clocks vary depending upon the display size but the frequency will typically fall between 5-65MHz
 - This corresponds to data rates between 10-60Mbps and with these speeds line capacitances need to be considered
 - In the majority of applications line capacitances of 20-40pF will not cause signal integrity issues
- The protection schemes below for data lines Dx are only examples and will vary with the particular application

Application Schematic:



Recommended SPA Devices:

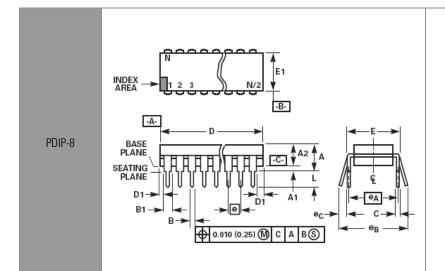
Ordering Number	ESD Level (Contact)	Cut-off Frequency	Line Capacitance @ V _R =2.5V	# of Channels	V _{RWM}	Packaging
SP6001-0xUTG-1	±30kV	115MHz	24pF	4/6/8	6V	μDFN-8/12/16
SP6002-0xUTG-1	±30kV	100MHz	30pF	4/6	6V	μDFN-8/12
SP6003-0xUTG-1	±15kV	175MHz	14pF	4/6	6V	μDFN-8/12



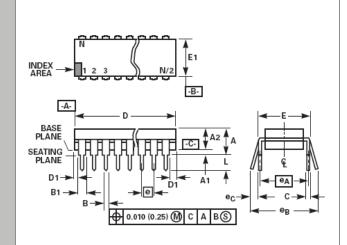
APPENDIX A SPA Package Outlines

PDIP-16

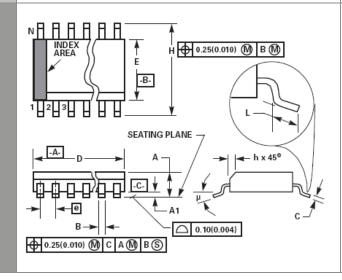
SOIC-8



Package			PDIP					
Pins		8						
JEDEC	E8	3.3 (JEDEC	MS-001-BA	(Issue D				
	Millimeters Inches				Nister			
	Min	Max	Min	Max	Notes			
Α	-	5.33	-	0.210	4			
A1	0.39	-	0.015	-	4			
A2	2.93	4.95	0.115	0.195	-			
В	0.356	0.558	0.014	0.022	-			
B1	1.15	1.77	0.045	0.070	8, 10			
С	0.204	0.355	0.008	0.014	-			
D	9.01	10.16	0.355	0.400	5			
D1	0.13	-	0.005	-	5			
Е	7.62	8.25	0.300	0.325	6			
E1	6.1	7.11	0.240	0.280	5			
е	2.54 E	BSC	0.100	BSC	-			
e _A	7.62 BSC		0.300	BSC	6			
e _B	-	10.92	-	0.430	7			
Ľ	2.93	3.81	0.115	0.150	4			
N	8		8		9			



Package			PDIP	PDIP								
Pins		16 Lea	ad Dual-in-L	ine								
JEDEC		E16.3 MS-001-BB Issue D										
	Millimeters Inches			Notes								
	Min	Max	Min	Max	Notes							
Α	-	5.33	-	0.210	4							
A1	0.39	-	0.015	-	4							
A2	2.93	4.95	0.115	0.195	-							
В	0.356	0.558	0.014	0.022	-							
B1	1.15	1.77	0.045	0.070	8, 10							
С	0.204	0.355	0.008	0.014	-							
D	18.66	19.68	0.735	0.775	5							
D1	0.13	-	0.005	-	5							
E	7.62	8.25	0.300	0.325	6							
E1	6.10	7.11	0.240	0.280	5							
е	2.54 E	3SC	0.100	BSC	-							
e _A	7.62 E	BSC	0.300	BSC	6							
e _B	-	10.92	-	0.430	7							
L	2.93	3.81	0.115	0.150	4							
N	16		16	3	9							

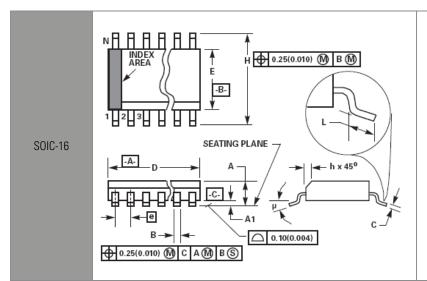


Package		SOIC							
Pins			16						
JEDEC	M1	6.15 (JEDE	C MS-012-	AC Issue C	;)				
	Millim	eters	Inch	ies	Notes				
	Min	Max	Min	Max	Notes				
Α	1.35	1.75	0.0532	0.0688	-				
A1	0.10	0.25	0.0040	0.0098	-				
В	0.33	0.51	0.013	0.020	9				
С	0.19	0.25	0.0075	0.0098	-				
D	9.80	10.00	0.3859	0.3937	3				
E	3.80	4.00	0.1497	0.1574	4				
e	1.27 E	BSC	0.050 BSC		-				
Н	5.80	6.20	0.2284	0.2440	-				
h	0.25	0.50	0.0099	0.0196	5				
L	0.40	1.27	0.016 0.050		6				
N	16	3	16	3	7				
μ	0°	8°	0°	8°	-				

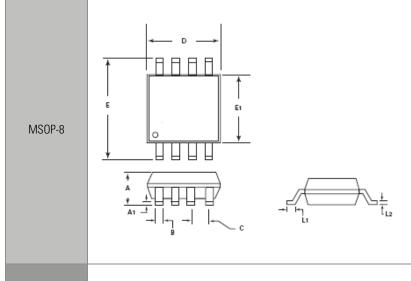


MSOP-10

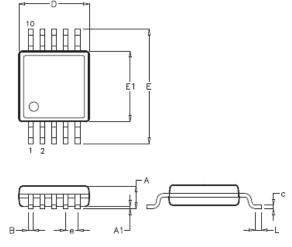
SPA Package Outlines (continued)



Package		SOIC						
Pins			16					
JEDEC	M1	6.15 (JEDE	C MS-012-	AC Issue C	;)			
	Millim	eters	Inch	ies	Notes			
	Min	Max	Min	Max	Notes			
Α	1.35	1.75	0.0532	0.0688	-			
A1	0.10	0.25	0.0040	0.0098	-			
В	0.33	0.51	0.013	0.020	9			
С	0.19	0.25	0.0075	0.0098	-			
D	9.80	10.00	0.3859	0.3937	3			
Е	3.80	4.00	0.1497	0.1574	4			
e	1.27 E	3SC	0.050	-				
Н	5.80	6.20	0.2284	0.2440	-			
h	0.25	0.50	0.0099	0.0196	5			
L	0.40	1.27	0.016	0.050	6			
N	16		16	7				
μ	0°	8°	0°	8°	-			

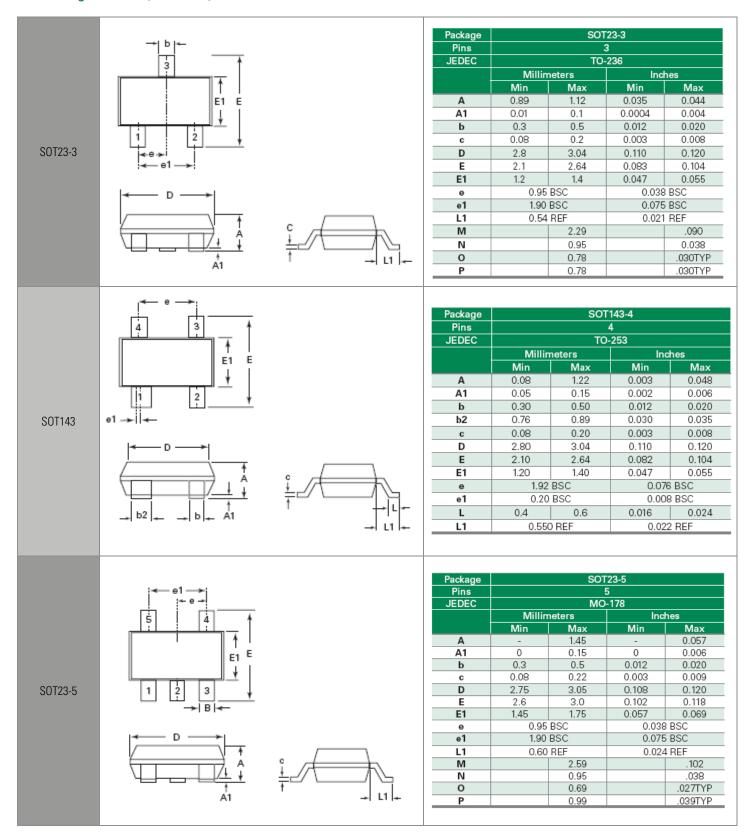


Package		MS	OP-8	
Pins			3	
	Millin	neters	Inc	hes
	Min	Max	Min	Max
D	2.90	3.10	0.114	.122
E	4.78	4.98	.188	.196
E1	2.90	3.10	.114	.122
Α	0.87	1.17	.034	.046
A1	0.05	0.25	.002	0.010
В	-	0.30TYP	-	0.012TYP
С	-	0.65TYP	-	0.026TYP
L1	0.52	0.54	0.020	0.021
L2	-	0.18TYP	-	.007TYP
F	-	5.28	-	.208
F1	-	4.24	-	.167
G	-	0.65	-	0.026
Н	-	0.38	-	.015
1	-	1.04	-	.041

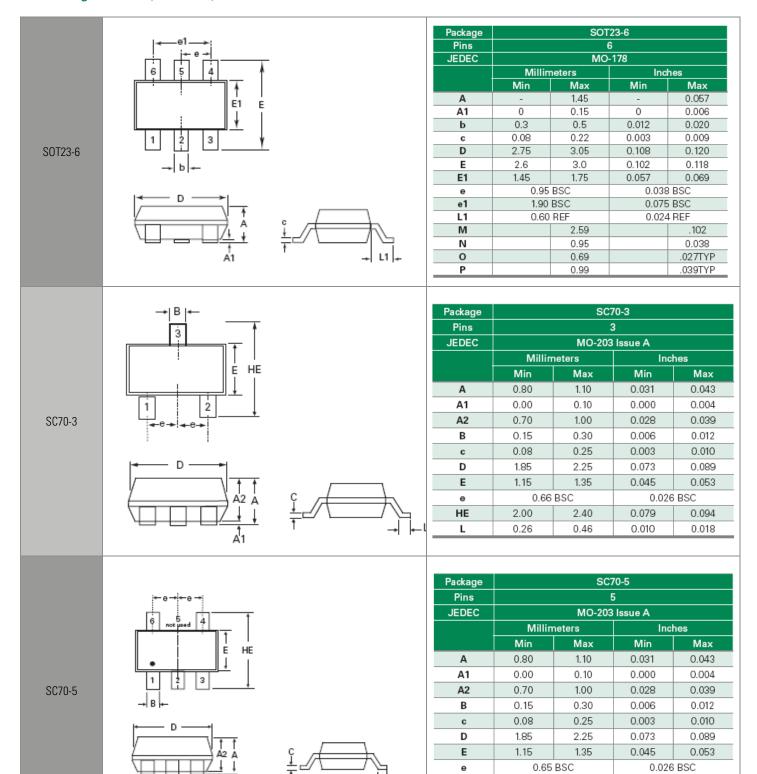


Package		MSOP10					
Pins		10					
	Millin	neters	Inches				
	Min	Max	Min	Max			
Α	-	1.10	-	0.043			
A1	0.00	0.15	0.000	0.006			
В	0.17	0.27	0.007	0.011			
С	0.08	0.23	0.003	0.009			
D	2.90	3.10	0.114	0.122			
E	4.67	5.10	0.184	0.200			
E1	2.90	3.10	0.114	0.122			
е	0.50	BSC	0.020 BSC				
HE	0.40	0.80	0.016 0.031				









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HE

L

2.00

0.26

2.40

0.46

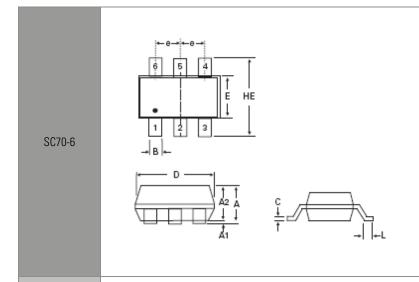
0.079

0.010

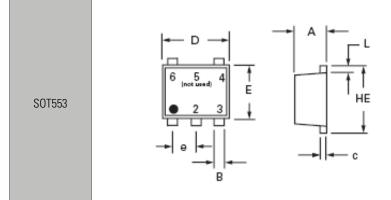
0.094

0.018

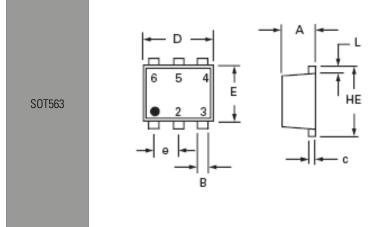




Package		SC70-6				
Pins		(6			
JEDEC		MO-203	Issue A			
	Millin	neters	Inc	hes		
	Min	Max	Min	Max		
Α	0.80	1.10	0.031	0.043		
A1	0.00	0.10	0.000	0.004		
A2	0.70	1.00	0.028	0.039		
В	0.15	0.30	0.006	0.012		
С	0.08	0.25	0.003	0.010		
D	1.85	2.25	0.073	0.089		
E	1.15	1.35	0.045 0.053			
е	0.65	BSC	0.026 BSC			
HE	2.00	2.40	0.079	0.094		
L	0.26	0.46	0.010	0.018		

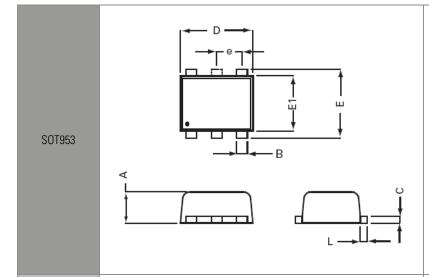


Package		SOT 553					
Pins		į	5				
	Millin	neters	Inc	hes			
	Min	Max	Min	Max			
Α	0.50	0.60	0.020	0.024			
В	0.17	0.27	0.007	0.011			
С	0.08	0.18	0.003	0.007			
D	1.50	1.70	0.059	0.067			
E	1.10	1.30	0.043	0.051			
е	0.50	BSC	0.020 BSC				
L	0.10	0.30	0.004	0.012			
HE	1.50	1.70	0.059	0.067			

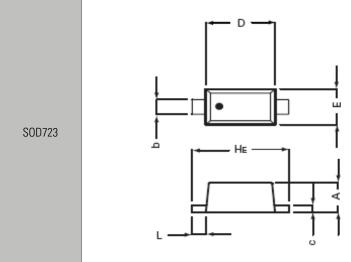


Package	SOT 563					
Pins	6					
	Millin	neters	Incl	nes		
	Min	Max	Min	Max		
Α	0.50	0.60	0.020	0.024		
В	0.17	0.27	0.007	0.011		
С	0.08	0.18	0.003	0.007		
D	1.50	1.70	0.059	0.067		
E	1.10	1.30	0.043	0.051		
е	0.50	BSC	0.020 BSC			
L	0.10	0.30	0.004	0.012		
HE	1.50	1.70	0.059	0.067		

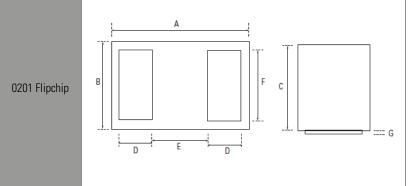




	SOT953					
Symbol	Millin	neters	Inches			
	Min	Max	Min	Max		
Α	0.44	0.5	0.170	0.020		
В	0.10	0.20	0.004	0.008		
С	0.05	0.15	0.002	0.006		
D	0.95	1.05	0.037	0.041		
E	0.95	1.05	0.037	0.041		
E1	0.75	0.85	0.029	0.033		
е	0.35	BSC	0.014 BSC			
L	0.05	0.15	0.002 0.006			

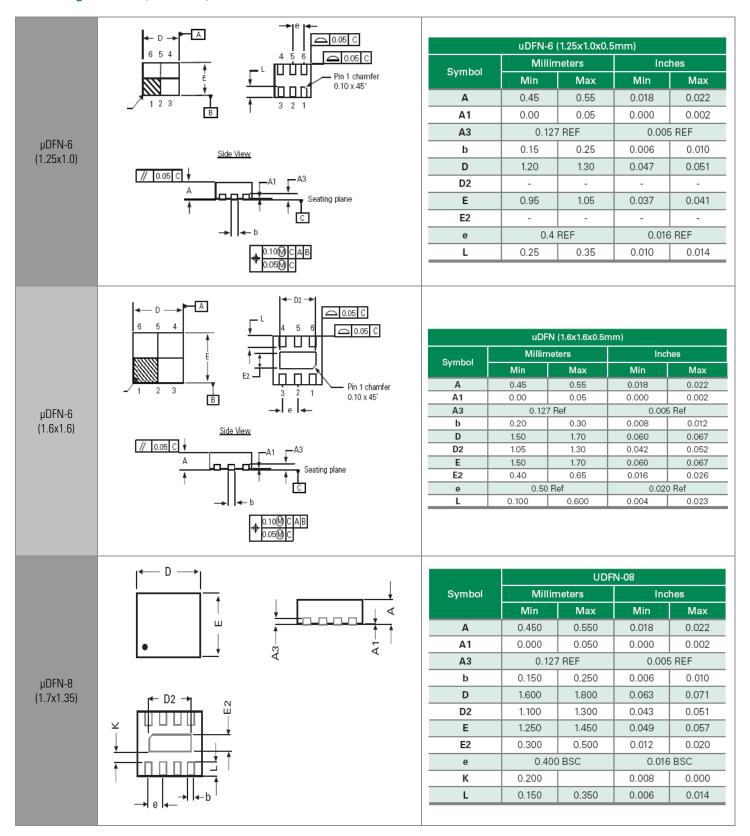


	SOD723					
Symbol	Millin	neters	Inches			
	Min	Max	Min	Max		
Α	0.46	0.51	0.018	0.020		
b	0.23	0.28	0.009	0.011		
С	0.08	0.13	0.003	0.005		
D	0.99	1.04	0.039	0.041		
E	0.58	0.64	0.023	0.025		
HE	1.37	1.47	0.054	0.058		
L	0.15	0.25	0.006	0.010		

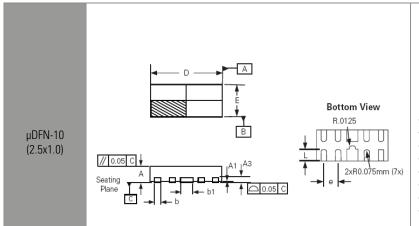


	0201 Flipchip						
Symbol	Millimeters			Inches			
	Min	Тур	Max	Min	Тур	Max	
Α	0.595	0.620	0.645	0.0234	0.0244	0.0254	
В	0.295	0.320	0.345	0.0116	0.0126	0.0136	
С	0.245	0.275	0.305	0.0096	0.0108	0.0120	
D	0.145	0.150	0.155	0.0057	0.0059	0.0061	
E	0.245	0.250	0.255	0.0096	0.0098	0.0100	
F	0.245	0.250	0.255	0.0096	0.0098	0.0100	
G	0.005	0.010	0.015	0.0002	0.0004	0.0006	

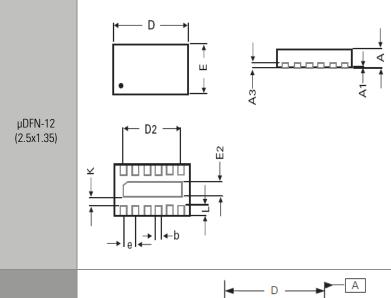




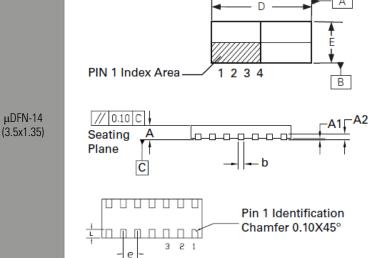




uDFN-10 (2.5x1.0x0.5mm)							
Combal	Millimeters				Inches		
Symbol	Min	Nom	Max	Min	Nom	Max	
А	0.48	0.515	0.55	0.019	0.020	0.021	
A1	0.00		0.05	0.000		0.022	
А3		0.125 Ref		0.005 Ref			
b	0.15	0.20	0.25	0.006	0.008	0.012	
b1	0.35	0.40	0.45	0.014	0.016	0.018	
D	2.40	2.50	2.60	0.094	0.098	0.102	
E	0.90	1.00	1.10	0.035	0.039	0.043	
е	0.50 BSC			0.020 BSC			
L	0.30	0.365	0.43	0.012	0.014	0.016	



	UDFN-12					
Symbol	Millin	neters	Inc	hes		
	Min	Max	Min	Max		
А	0.450	0.550	0.018	0.022		
A1	0.000	0.050	0.000	0.002		
А3	0.127	7 REF	0.005	5 REF		
b	0.150	0.250	0.006	0.010		
D	2.400	2.600	0.094	0.102		
D2	1.900	2.100	0.075	0.083		
E	1.250	1.450	0.049	0.057		
E2	0.300	0.500	0.012	0.020		
е	0.400 BSC		0.016 BSC			
K	0.200		0.008	0.000		
L	0.150	0.350	0.006	0.014		



uDFN-14 (3.5x1.35x0.5mm)							
		Millimeters			Inches		
Symbol	Min	Nom	Max	Min	Nom	Max	
Α	0.45	0.50	0.55	0.018	0.020	0.022	
A1	0.00	0.02	0.05	0.000	0.001	0.002	
A2	0.203 Ref			0.008 Ref			
b	0.15	0.20	0.25	0.006	0.008	0.012	
D	3.40	3.50	3.60	0.134	0.138	0.142	
D2	-	-	-	-	-	-	
E	1.25	1.35	1.45	0.050	0.054	0.058	
E1	-	-	-	-	-	-	
е	0.500 BSC			0.020 BSC			
L	0.25	0.30	0.35	0.010	0.012	0.014	





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