# 12V Input 6A Output Power Supply in Inductor (PSI²) Module

RoHS compliant

## FEATURES

- **Integrated Point of Load power module using PSI² Power Supply in Inductor technology**
- **Small footprint, low-profile, 15mm x 9mm x 3mm, with LGA Package (with 0.63 mm pads)**
- **Efficiency of 95.2% at 3A and 94.2% at 6A for 5V output**
- **High output current, 6A without derating at 85°C ambient with no air flow**
- **Wide output voltage selections: from 0.8V to 5V output voltages with ±10% trim capability**
- **Output voltage remote sensing**
- **Pre-bias startup capability**
- **Adjustable soft-start time**
- **Enable signal input and Power Good signal output**
- **Programmable Under Voltage Lock Out (UVLO)**
- **Output Over-Current Protection (OCP)**
- **Operating temperature range -40°C to 85°C**
- **Qualified to IPC9592B, Class II**
- **MSL 3 and RoHS compliant**

## APPLICATIONS

- **Broadband and communications equipment**
- **DSP and FPGA Point of Load applications**
- **High density distributed power systems**
- **Systems using PCI / PCI express / PXI express**
- **Automated test and medical equipment**

## DESCRIPTION

SPM1004 is an easy-to-use 6A output integrated Point of Load (POL) power supply module. It contains integrated power MOSFETs, driver, PWM controller, a high performance inductor, input and output capacitors and other passive components in one low profile LGA package using PSI² technology.

Only one external input capacitor and one external output capacitor are needed for typical applications. There is no need for loop compensation, sensitive PCB layout, inductor selection, or in-circuit production testing.

SPM1004 integrated POL power module series are offered with eight models for eight different output voltages: 5.0V, 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, 1.0V, and 0.8V. Each output voltage can be trimmed by ±10%.

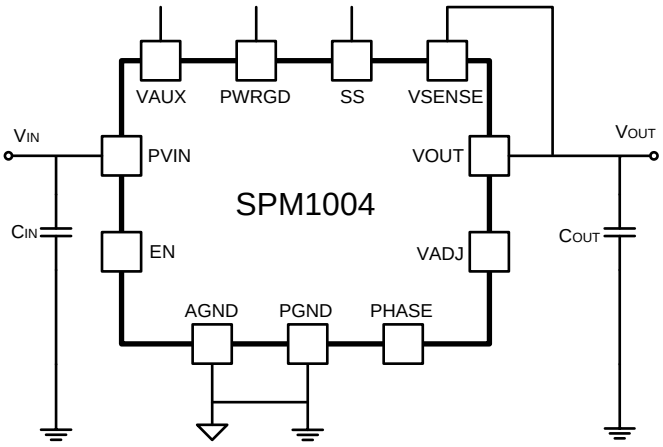
All SPM1004 models deliver full 6A load current without derating at 85°C ambient temperature with no airflow.

Small size (15mm x 9mm) and low profile (3mm) allows SPM1004 to be placed very close to its load or on the back side of the PCB for high density applications.

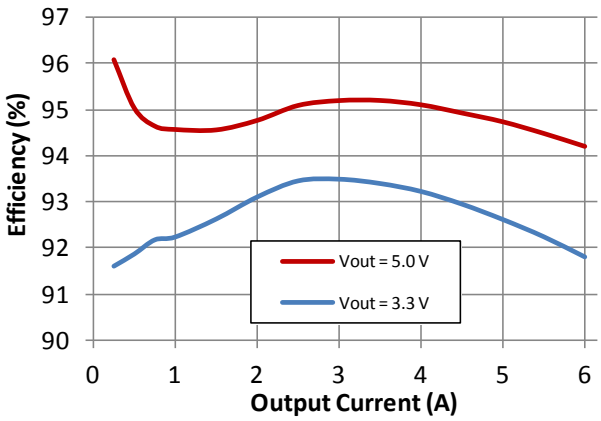
Constant-on-time (COT) control is used to achieve excellent transient response to line and load changes without sacrificing stability and high efficiency at light load.

Sumida's PSI² technology ensures optimal inductor design, uniform temperature distribution and very low temperature difference between case and IC die.

### SIMPLIFIED APPLICATION




### EFFICIENCY VS LOAD CURRENT (VIN = 12V)



## ABSOLUTE MAXIMUM(1) RATINGS over operating temperature range (unless otherwise noted)

| | | VALUE | | Unit |
|---|---|---|---|---|
| | | MIN | MAX | |
| Input Signals | PVIN | -0.3 | 18 | V |
| | EN | -0.3 | 6 | V |
| | VSENSE | -0.3 | 6 | V |
| | VADJ | -0.3 | 6 | V |
| | SS | -0.3 | 6 | V |
| Output Signals | VOUT | -0.6 | PVIN | V |
| | PHASE | -0.6 | PVIN | V |
| | PWRGD | -0.3 | 6 | V |
| | VAUX | -0.3 | 6 | V |
| Current | EN | | 2.5 | mA |
| Temperature | Operating Junction Temperature | -40 | 150 | °C |
| | Storage Temperature | -65 | 150 | °C |
| | Lead Temperature (soldering) | | 260 | °C |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the module. These are stress ratings only, and functional operation of the module at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect reliability.

## ELECTRICAL CHARACTERISTICS

The electrical characteristics are presented in two parts. Part 1 provides the electrical characteristics that are common to all models and Part 2 provides the electrical characteristics that are specific to each model.

The electrical performance is based on the following conditions unless otherwise stated: 25°C ambient temperature, no air flow; $V_{IN}$ = 12V, $I_{OUT}$ = 6A, $C_{IN}$ = 100µF ceramic, $C_{OUT}$ = 200µF ceramic.

### Part 1: Electrical Characteristics Common to All Models:

| PARAMETERS | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{OUT}$: Output current | $T_A$ = -40°C to 85°C, natural convection | | 0 | | 6 | A |
| $V_{IN}$: Input voltage | $T_A$ = -40°C to 85°C; $I_{OUT}$ 0 to max | | 9 | 12 | 15 | V |
| $V_{EN\_ON}$ Enable on voltage | Enable high voltage (module turned on) | | 1.1 | 1.3 | | V |
| $V_{EN\_OFF}$ Enable off voltage | Enable low voltage (module turned off) | | | 0.5 | 0.6 | V |
| $I_{EN}$ Enable input current | $V_{EN}$ = 2V | | | 0.1 | | mA |
| | $V_{EN}$ = 0V | | | 0 | | µA |
| $I_{STBY}$ Input standby current | EN pin to PGND (shut down) | | | 0.2 | 0.5 | mA |
| | EN = 2V, $I_{OUT}$ = 0A | | | 1.0 | 2.5 | mA |
| PWRGD Power Good Signal | $V_{OUT}$ rising (% of $V_{OUT}$) | PWRGD high | 87% | 91% | 94% | |
| | | Leakage current | | 10 | 100 | nA |
| | | PWRGD delay | | 2.5 | | ms |
| | $V_{OUT}$ falling (% of $V_{OUT}$) | PWRGD low | | 80% | | V |
| | | At 4mA sink current | | | 0.4 | V |
| OVP Over-Voltage Protection | OVP threshold (percentage of nominal) | | 117% | 120% | 123% | |
| | OVP shutdown delay | | | 2 | | µs |
| Thermal shutdown (die temperature) | Thermal shutdown | | | 170 | | °C |
| | Thermal shutdown recovery hysteresis | | | 15 | | °C |
| $V_{AUX}$: Auxiliary output | Output voltage | | 4.6 | 4.8 | 5.0 | V |
| | Output current | | | | 1 | mA |
| $C_{VAUX}$: External capacitor at VAUX | Ceramic | | | 22 | | µF |
| $C_{PVIN}$: External capacitor at PVIN | Ceramic | | 47 | | | µF |
| | Non-ceramic | | | 220 | | µF |
| $C_{OUT}$: External output capacitor | Ceramic | | 100 | 200 | 500 | µF |
| | Non-ceramic (Electrolytic or tantalum) | | | | 2000 | µF |

## Part 2: Electrical Characteristics Specific for Each Individual Model

### SPM1004-5V0

| PARAMETERS | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{START}$ | Startup voltage | Over $I_{OUT}$ range | | 8.5 | 9.0 | 9.5 | V |
| UVLO | Under Voltage Lock Out | Over $I_{OUT}$ range | | 7.0 | 7.5 | 8.0 | V |
| $V_{OUT(adj)}$: Output voltage trim range | | Over $I_{OUT}$ range | | 4.5 | 5.0 | 5.5 | V |
| $V_{OUT}$ | Set point accuracy | $T_A$ = 25°C, $V_{IN}$ = 12V, $I_{OUT}$ = 3A | | | ±1% | | |
| | Temperature variation | -40°C < $T_A$ < +85°C, $I_{OUT}$ = 3A | | | ±0.5% | | |
| | Line regulation | Over $V_{IN}$ range, $T_A$ = 25°C, $I_{OUT}$ = 3A | | | ±0.5% | | |
| | Load regulation | Over $I_{OUT}$ range, $T_A$ = 25°C, $V_{IN}$ = 12V | | | ±1% | | |
| | Total variation | Set-point, line, load, temperature variation | | | | ±4% | |
| $V_{o\_rip}$, | Output voltage ripple | 20MHz bandwidth, $V_{IN}$ = 12V, $I_{OUT}$ = 6A | | | 20 | | mVpp |
| η | Efficiency | $V_{IN}$ = 12V | $I_{OUT}$ = 3A | | 95.2% | | |
| | | | $I_{OUT}$ = 6A | | 94.2% | | |
| | | $V_{IN}$ = 9V | $I_{OUT}$ = 3A | | 96.1% | | |
| | | | $I_{OUT}$ = 6A | | 94.5% | | |
| | | $V_{IN}$ = 15V | $I_{OUT}$ = 3A | | 94.3% | | |
| | | | $I_{OUT}$ = 6A | | 93.7% | | |
| Transient Response | | 1A/µs load step between 2A and 5A | Over/undershoot | | 30 | | mV |
| | | | Recovery time | | 75 | | µs |
| $F_S$ | Switching frequency | $V_{IN}$ = 12V, $I_{OUT}$ = 6A | | | 800 | | kHz |
| $I_{LIM}$ | Current Limit Point | $V_{IN}$ = 12V | | | 8.5 | | A |

### SPM1004-3V3

| PARAMETERS | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{START}$ | Startup voltage | Over $I_{OUT}$ range | | 8.0 | 8.5 | 9.0 | V |
| UVLO | Under Voltage Lock Out | Over $I_{OUT}$ range | | 6.5 | 7.0 | 7.5 | V |
| $V_{OUT(adj)}$: Output voltage trim range | | Over $I_{OUT}$ range | | 2.97 | 3.3 | 3.63 | V |
| $V_{OUT}$ | Set point accuracy | $T_A$ = 25°C, $V_{IN}$ = 12V, $I_{OUT}$ = 3A | | | ±1% | | |
| | Temperature variation | -40°C < $T_A$ < +85°C, $I_{OUT}$ = 3A | | | ±0.5% | | |
| | Line regulation | Over $V_{IN}$ range, $T_A$ = 25°C, $I_{OUT}$ = 3A | | | ±0.5% | | |
| | Load regulation | Over $I_{OUT}$ range, $T_A$ = 25°C, $V_{IN}$ = 12V | | | ±1% | | |
| | Total variation | Set-point, line, load, temperature variation | | | | ±3% | |
| $V_{o\_rip}$, | Output voltage ripple | 20MHz bandwidth, $V_{IN}$ = 12V, $I_{OUT}$ = 6A | | | 20 | | mVpp |
| η | Efficiency | $V_{IN}$ = 12V | $I_{OUT}$ = 3A | | 93.5% | | |
| | | | $I_{OUT}$ = 6A | | 91.8% | | |
| | | $V_{IN}$ = 9V | $I_{OUT}$ = 3A | | 94.3% | | |
| | | | $I_{OUT}$ = 6A | | 92.2% | | |
| | | $V_{IN}$ = 15V | $I_{OUT}$ = 3A | | 92.7% | | |
| | | | $I_{OUT}$ = 6A | | 91.3% | | |
| Transient Response | | 1A/µs load step between 2A and 5A | Over/undershoot | | 25 | | mV |
| | | | Recovery time | | 50 | | µs |
| $F_S$ | Switching frequency | $V_{IN}$ = 12V, $I_{OUT}$ = 6A | | | 800 | | kHz |
| $I_{LIM}$ | Current Limit Point | $V_{IN}$ = 12V | | | 8.5 | | A |

## SPM1004-2V5

| PARAMETERS | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{START}$ | Startup voltage | Over $I_{OUT}$ range | | 8.0 | 8.5 | 9.0 | V |
| UVLO | Under Voltage Lock Out | Over $I_{OUT}$ range | | 6.5 | 7.0 | 7.5 | V |
| $V_{OUT(adj)}$: Output voltage trim range | | Over $I_{OUT}$ range | | 2.25 | 2.5 | 2.75 | V |
| $V_{OUT}$ | Set point accuracy | $T_A$ = 25°C, $V_{IN}$ = 12V, $I_{OUT}$ = 3A | | | ±1% | | |
| | Temperature variation | -40°C < $T_A$ < +85°C, $I_{OUT}$ = 3A | | | ±0.5% | | |
| | Line regulation | Over $V_{IN}$ range, $T_A$ = 25°C, $I_{OUT}$ = 3A | | | ±0.5% | | |
| | Load regulation | Over $I_{OUT}$ range, $T_A$ = 25°C, $V_{IN}$ = 12V | | | ±1% | | |
| | Total variation | Set-point, line, load, temperature variation | | | | ±3% | |
| $V_{o\_rip}$, | Output voltage ripple | 20MHz bandwidth, $V_{IN}$ = 12V, $I_{OUT}$ = 6A | | | 20 | | mVpp |
| η | Efficiency | $V_{IN}$ = 12V | $I_{OUT}$ = 3A | | 92.5% | | |
| | | | $I_{OUT}$ = 6A | | 90.2% | | |
| | | $V_{IN}$ = 9V | $I_{OUT}$ = 3A | | 93.2% | | |
| | | | $I_{OUT}$ = 6A | | 90.6% | | |
| | | $V_{IN}$ = 15V | $I_{OUT}$ = 3A | | 91.7% | | |
| | | | $I_{OUT}$ = 6A | | 89.7% | | |
| Transient Response | | 1A/µs load step between 2A and 5A | Over/undershoot | | 25 | | mV |
| | | | Recovery time | | 50 | | µs |
| $F_S$ | Switching frequency | $V_{IN}$ = 12V, $I_{OUT}$ = 6A | | | 600 | | kHz |
| $I_{LIM}$ | Current Limit Point | $V_{IN}$ = 12V | | | 8.5 | | A |

## SPM1004-1V8

| PARAMETERS | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{START}$ | Startup voltage | Over $I_{OUT}$ range | | 8.0 | 8.5 | 9.0 | V |
| UVLO | Under Voltage Lock Out | Over $I_{OUT}$ range | | 6.5 | 7.0 | 7.5 | V |
| $V_{OUT(adj)}$: Output voltage trim range | | Over $I_{OUT}$ range | | 1.62 | 1.8 | 1.98 | V |
| $V_{OUT}$ | Set point accuracy | $T_A$ = 25°C, $V_{IN}$ = 12V, $I_{OUT}$ = 3A | | | ±1% | | |
| | Temperature variation | -40°C < $T_A$ < +85°C, $I_{OUT}$ = 3A | | | ±0.5% | | |
| | Line regulation | Over $V_{IN}$ range, $T_A$ = 25°C, $I_{OUT}$ = 3A | | | ±0.5% | | |
| | Load regulation | Over $I_{OUT}$ range, $T_A$ = 25°C, $V_{IN}$ = 12V | | | ±1% | | |
| | Total variation | Set-point, line, load, temperature variation | | | | ±3% | |
| $V_{o\_rip}$, | Output voltage ripple | 20MHz bandwidth, $V_{IN}$ = 12V, $I_{OUT}$ = 6A | | | 20 | | mVpp |
| η | Efficiency | $V_{IN}$ = 12V | $I_{OUT}$ = 3A | | 91.0% | | |
| | | | $I_{OUT}$ = 6A | | 87.6% | | |
| | | $V_{IN}$ = 9V | $I_{OUT}$ = 3A | | 91.6% | | |
| | | | $I_{OUT}$ = 6A | | 87.9% | | |
| | | $V_{IN}$ = 15V | $I_{OUT}$ = 3A | | 89.7% | | |
| | | | $I_{OUT}$ = 6A | | 86.7% | | |
| Transient Response | | 1A/µs load step between 2A and 5A | Over/undershoot | | 20 | | mV |
| | | | Recovery time | | 50 | | µs |
| $F_S$ | Switching frequency | $V_{IN}$ = 12V, $I_{OUT}$ = 6A | | | 600 | | kHz |
| $I_{LIM}$ | Current Limit Point | $V_{IN}$ = 12V | | | 8.5 | | A |

## SPM1004-1V5

| PARAMETERS | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{START}$ | Startup voltage | Over $I_{OUT}$ range | | 8.0 | 8.5 | 9.0 | V |
| UVLO | Under Voltage Lock Out | Over $I_{OUT}$ range | | 6.5 | 7.0 | 7.5 | V |
| $V_{OUT(adj)}$: Output voltage trim range | | Over $I_{OUT}$ range | | 1.35 | 1.5 | 1.65 | V |
| $V_{OUT}$ | Set point accuracy | $T_A$ = 25°C, $V_{IN}$ = 12V, $I_{OUT}$ = 3A | | | ±1% | | |
| | Temperature variation | -40°C < $T_A$ < +85°C, $I_{OUT}$ = 3A | | | ±0.5% | | |
| | Line regulation | Over $V_{IN}$ range, $T_A$ = 25°C, $I_{OUT}$ = 3A | | | ±0.5% | | |
| | Load regulation | Over $I_{OUT}$ range, $T_A$ = 25°C, $V_{IN}$ = 12V | | | ±1% | | |
| | Total variation | Set-point, line, load, temperature variation | | | | ±3% | |
| $V_{o\_rip}$, | Output voltage ripple | 20MHz bandwidth, $V_{IN}$ = 12V, $I_{OUT}$ = 6A | | | 20 | | mVpp |
| η | Efficiency | $V_{IN}$ = 12V | $I_{OUT}$ = 3A | | 90.2% | | |
| | | | $I_{OUT}$ = 6A | | 86.1% | | |
| | | $V_{IN}$ = 9V | $I_{OUT}$ = 3A | | 90.8% | | |
| | | | $I_{OUT}$ = 6A | | 86.4% | | |
| | | $V_{IN}$ = 15V | $I_{OUT}$ = 3A | | 89.3% | | |
| | | | $I_{OUT}$ = 6A | | 85.4% | | |
| Transient Response | | 1A/µs load step between 2A and 5A | Over/undershoot | | 20 | | mV |
| | | | Recovery time | | 50 | | µs |
| $F_S$ | Switching frequency | $V_{IN}$ = 12V, $I_{OUT}$ = 6A | | | 550 | | kHz |
| $I_{LIM}$ | Current Limit Point | $V_{IN}$ = 12V | | | 8.5 | | A |

## SPM1004-1V2

| PARAMETERS | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{START}$ | Startup voltage | Over $I_{OUT}$ range | | 8.0 | 8.5 | 9.0 | V |
| UVLO | Under Voltage Lock Out | Over $I_{OUT}$ range | | 6.5 | 7.0 | 7.5 | V |
| $V_{OUT(adj)}$: Output voltage trim range | | Over $I_{OUT}$ range | | 1.08 | 1.2 | 1.32 | V |
| $V_{OUT}$ | Set point accuracy | $T_A$ = 25°C, $V_{IN}$ = 12V, $I_{OUT}$ = 3A | | | ±1% | | |
| | Temperature variation | -40°C < $T_A$ < +85°C, $I_{OUT}$ = 3A | | | ±0.5% | | |
| | Line regulation | Over $V_{IN}$ range, $T_A$ = 25°C, $I_{OUT}$ = 3A | | | ±0.5% | | |
| | Load regulation | Over $I_{OUT}$ range, $T_A$ = 25°C, $V_{IN}$ = 12V | | | ±1% | | |
| | Total variation | Set-point, line, load, temperature variation | | | | ±3% | |
| $V_{o\_rip}$, | Output voltage ripple | 20MHz bandwidth, $V_{IN}$ = 12V, $I_{OUT}$ = 6A | | | 20 | | mVpp |
| η | Efficiency | $V_{IN}$ = 12V | $I_{OUT}$ = 3A | | 89.9% | | |
| | | | $I_{OUT}$ = 6A | | 84.5% | | |
| | | $V_{IN}$ = 9V | $I_{OUT}$ = 3A | | 89.9% | | |
| | | | $I_{OUT}$ = 6A | | 84.7% | | |
| | | $V_{IN}$ = 15V | $I_{OUT}$ = 3A | | 88.6% | | |
| | | | $I_{OUT}$ = 6A | | 83.7% | | |
| Transient Response | | 1A/µs load step between 2A and 5A | Over/undershoot | | 20 | | mV |
| | | | Recovery time | | 30 | | µs |
| $F_S$ | Switching frequency | $V_{IN}$ = 12V, $I_{OUT}$ = 6A | | | 450 | | kHz |
| $I_{LIM}$ | Current Limit Point | $V_{IN}$ = 12V | | | 8.5 | | A |

## SPM1004-1V0

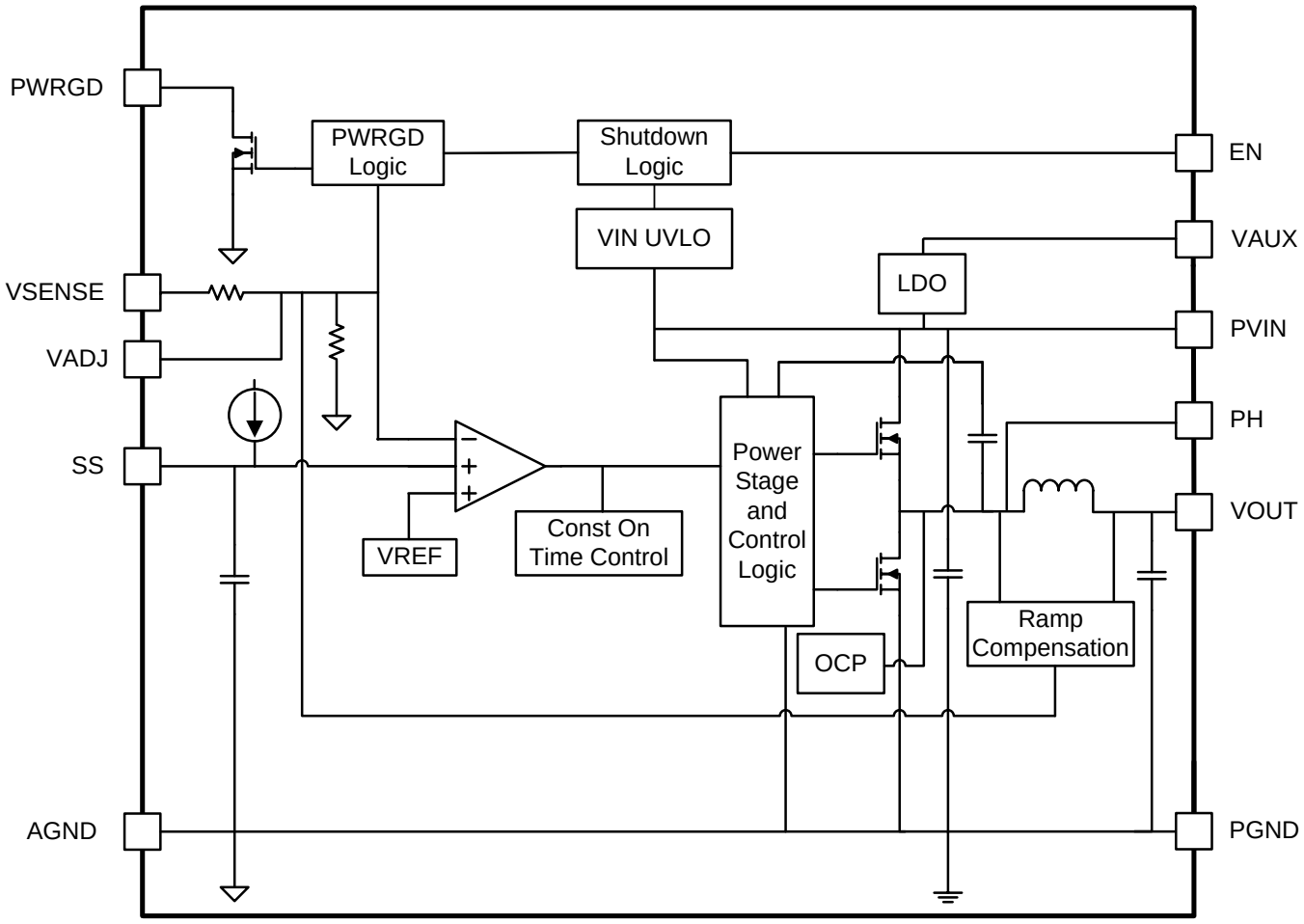
| PARAMETERS | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{START}$ | Startup voltage | Over $I_{OUT}$ range | | 8.0 | 8.5 | 9.0 | V |
| UVLO | Under Voltage Lock Out | Over $I_{OUT}$ range | | 6.5 | 7.0 | 7.5 | V |
| $V_{OUT(adj)}$: Output voltage trim range | | Over $I_{OUT}$ range | | 0.9 | 1.0 | 1.1 | V |
| $V_{OUT}$ | Set point accuracy | $T_A$ = 25°C, $V_{IN}$ = 12V, $I_{OUT}$ = 3A | | | ±1% | | |
| | Temperature variation | -40°C < $T_A$ < +85°C, $I_{OUT}$ = 3A | | | ±0.5% | | |
| | Line regulation | Over $V_{IN}$ range, $T_A$ = 25°C, $I_{OUT}$ = 3A | | | ±0.5% | | |
| | Load regulation | Over $I_{OUT}$ range, $T_A$ = 25°C, $V_{IN}$ = 12V | | | ±1% | | |
| | Total variation | Set-point, line, load, temperature variation | | | | ±3% | |
| $V_{o\_rip}$, | Output voltage ripple | 20MHz bandwidth, $V_{IN}$ = 12V, $I_{OUT}$ = 6A | | | 20 | | mVpp |
| η | Efficiency | $V_{IN}$ = 12V | $I_{OUT}$ = 3A | | 87.8% | | |
| | | | $I_{OUT}$ = 6A | | 82.1% | | |
| | | $V_{IN}$ = 9V | $I_{OUT}$ = 3A | | 88.3% | | |
| | | | $I_{OUT}$ = 6A | | 82.3% | | |
| | | $V_{IN}$ = 15V | $I_{OUT}$ = 3A | | 86.6% | | |
| | | | $I_{OUT}$ = 6A | | 81.3% | | |
| Transient Response | | 1A/µs load step between 2A and 5A | Over/undershoot | | 20 | | mV |
| | | | Recovery time | | 30 | | µs |
| $F_S$ | Switching frequency | $V_{IN}$ = 12V, $I_{OUT}$ = 6A | | | 400 | | kHz |
| $I_{LIM}$ | Current Limit Point | $V_{IN}$ = 12V | | | 8.5 | | A |

## SPM1004-0V8

| PARAMETERS | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{START}$ | Startup voltage | Over $I_{OUT}$ range | | 8.0 | 8.5 | 9.0 | V |
| UVLO | Under Voltage Lock Out | Over $I_{OUT}$ range | | 6.5 | 7.0 | 7.5 | V |
| $V_{OUT(adj)}$: Output voltage trim range | | Over $I_{OUT}$ range | | 0.72 | 0.8 | 0.88 | V |
| $V_{OUT}$ | Set point accuracy | $T_A$ = 25°C, $V_{IN}$ = 12V, $I_{OUT}$ = 3A | | | ±0.5% | | |
| | Temperature variation | -40°C < $T_A$ < +85°C, $I_{OUT}$ = 3A | | | ±0.5% | | |
| | Line regulation | Over $V_{IN}$ range, $T_A$ = 25°C, $I_{OUT}$ = 3A | | | ±0.5% | | |
| | Load regulation | Over $I_{OUT}$ range, $T_A$ = 25°C, $V_{IN}$ = 12V | | | ±1% | | |
| | Total variation | Set-point, line, load, temperature variation | | | | ±3% | |
| $V_{o\_rip}$, | Output voltage ripple | 20MHz bandwidth, $V_{IN}$ = 12V, $I_{OUT}$ = 6A | | | 20 | | mVpp |
| η | Efficiency | $V_{IN}$ = 12V | $I_{OUT}$ = 3A | | 85.7% | | |
| | | | $I_{OUT}$ = 6A | | 78.7% | | |
| | | $V_{IN}$ = 9V | $I_{OUT}$ = 3A | | 86.4% | | |
| | | | $I_{OUT}$ = 6A | | 79.0% | | |
| | | $V_{IN}$ = 15V | $I_{OUT}$ = 3A | | 84.3% | | |
| | | | $I_{OUT}$ = 6A | | 77.8% | | |
| Transient Response | | 1A/µs load step between 2A and 5A | Over/undershoot | | 20 | | mV |
| | | | Recovery time | | 25 | | µs |
| $F_S$ | Switching frequency | $V_{IN}$ = 12V, $I_{OUT}$ = 6A | | | 400 | | kHz |
| $I_{LIM}$ | Current Limit Point | $V_{IN}$ = 12V | | | 8.5 | | A |

# POWER MODULE INFORMATION

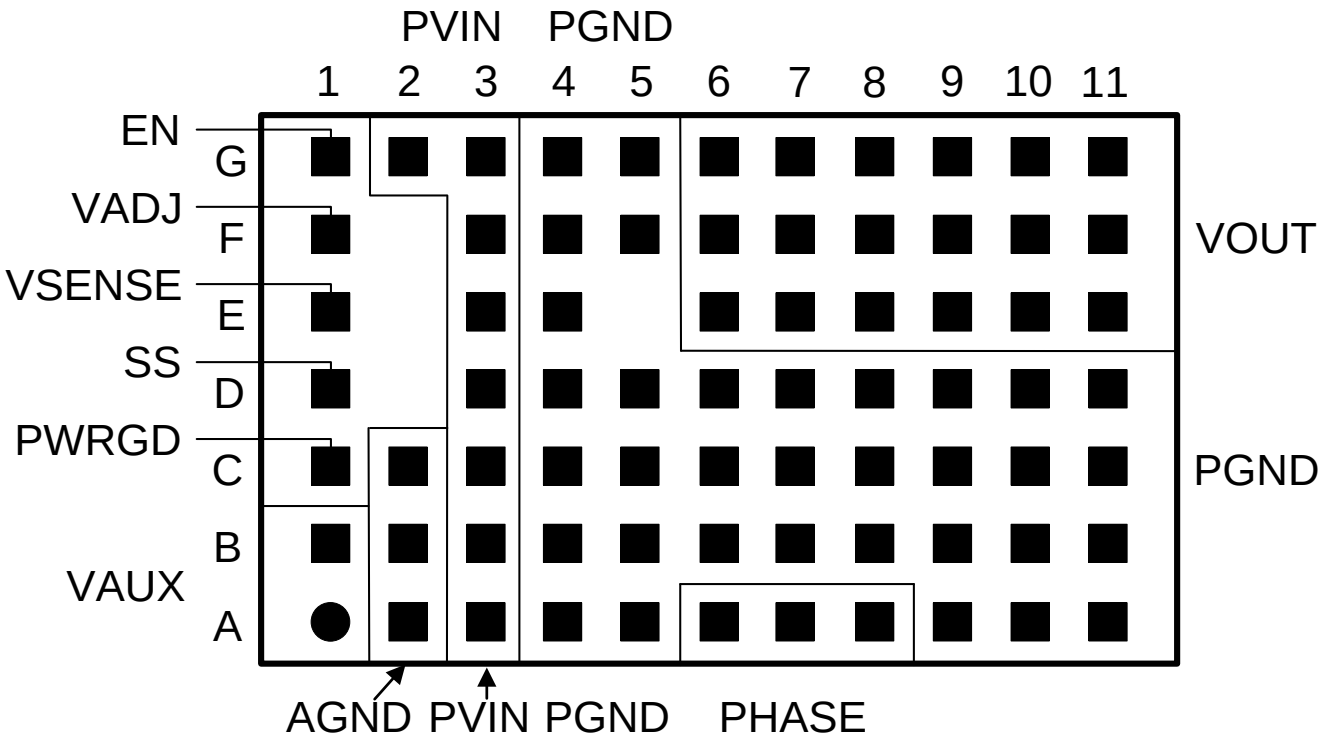
## FUNCTIONAL BLOCK DIAGRAM for SPM1004 (FOR ALL MODELS)



## PIN DESCRIPTIONS (ALL SPM1004 Models)

| PIN Name | Description |
|---|---|
| PVIN<br>(A3, B3, C3, D3, E3, F3, G2-G3) | **Input voltage pins, referenced to PGND**. Connect input ceramic capacitors between these pins and PGND plane, close to the power module. It is suggested to place the ceramic capacitors at both sides of the module, one between PIN A3 and PIN A4-A5 and one between PIN G2-G3 and PIN G4-G5. |
| VAUX<br>(A1, B1) | **Auxiliary output** from an LDO in the module, which is referenced to AGND. An external capacitor is not normally necessary but can be added if required.<br>**Note:** VAUX pin can only provide 1mA maximum current. |
| PHASE<br>(A6-A8) | **Switching node of the Buck converter**. Connect these pins together using a small and isolated copper plane under the module for best thermal performance. Do not connect any external component to these pins. Do not use these pins for other functions. |
| VOUT<br>(E6-E11, F6-F11, G6-G11) | **Output voltage pins**. Connect these pins together onto a copper plane. Connect external output filter capacitors between these pins and PGND plane, close to the module. |
| PGND<br>(A4-A5, A9-A11, B4-B11, C4-C11, D4-D11, E4, F4-F5, G4-G5) | **Zero DC voltage reference for power circuitry**. These pins should be connected directly to the PCB ground plane. All pins must be connected together externally with a copper plane located directly under the module. |
| AGND<br>(A2, B2, C2) | **Zero DC voltage reference for the analog control circuitry**. A small analog ground plane is recommended, and these pins should be connected directly to the PCB analog ground plane. A single point external connection between AGND and PGND is recommended. VADJ, SS, and VSENSE pins should be referenced to analog ground. |
| EN<br>(G1) | **Enable and Under Voltage Lock Out (UVLO) pin**. When floating or above Enable On Voltage ($V_{EN\_ON}$), the power module will be turned on when the power input voltage (PVIN) is above startup voltage ($V_{START}$). When EN pin is below Enable Off Voltage ($V_{EN\_OFF}$), the power module will be off.<br>Different startup voltage can be programmed by an external resistor if required, as discussed on page 18. |
| VADJ<br>(F1) | **Output voltage adjustment pin**. The output voltage can be adjusted up to ±10% of its nominal value. A resistor between VADJ and VSENSE will trim the output voltage down. A resistor between VADJ and AGND will trim the output voltage up. Refer to page 15. |
| VSENSE<br>(E1) | **Remote sensing pin**. Connect this pin to VOUT close to the load for improved voltage regulation.<br>**Note**: this pin is not connected to VOUT inside the module, and must be connected externally. |
| SS<br>(D1) | **Soft-start pin**. Soft-start time can be increased by connecting a capacitor between this pin and AGND. |
| PWRGD<br>(C1) | **Power Good pin**, an open drain output. A resistor connected between PWRGD and VAUX can be used as a pull-up. PWRGD is high if the output voltage is higher than 91% of the nominal value. It will be pulled down if the output voltage is less than 80% or higher than 120% of the nominal value. |

**LGA PACKAGE**
**73 PINS,**
**(TOP VIEW)**



# TYPICAL EFFICIENCY AND POWER LOSS DATA (Note 1)

### SPM1004-5V0, $V_{OUT}$ = 5V

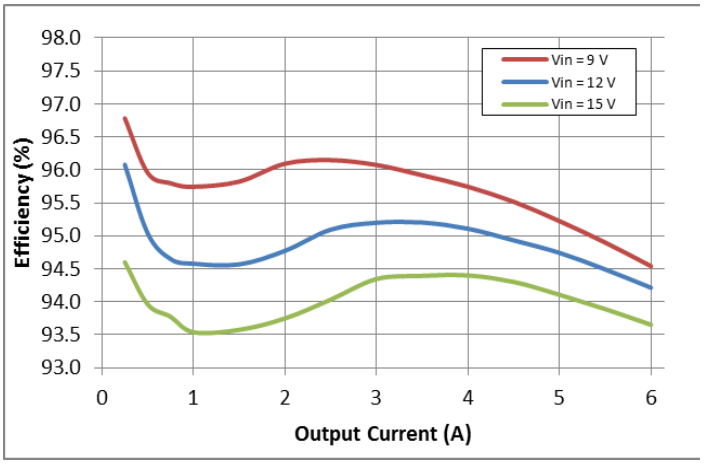



Fig. 1 Efficiency vs Output Current

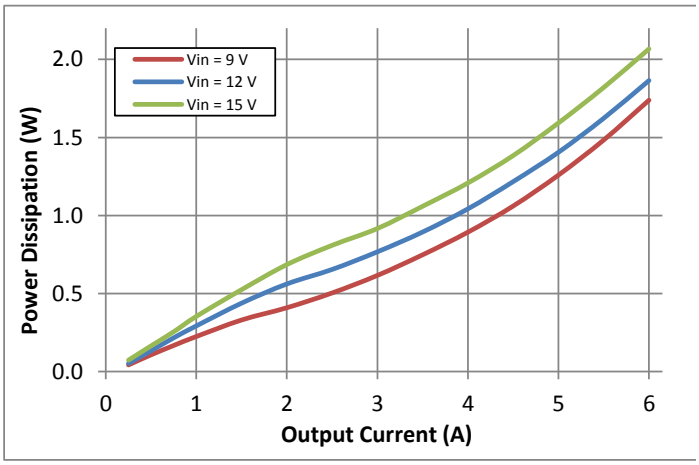



Fig. 2 Power Dissipation vs Output Current

### SPM1004-3V3, $V_{OUT}$ = 3.3V

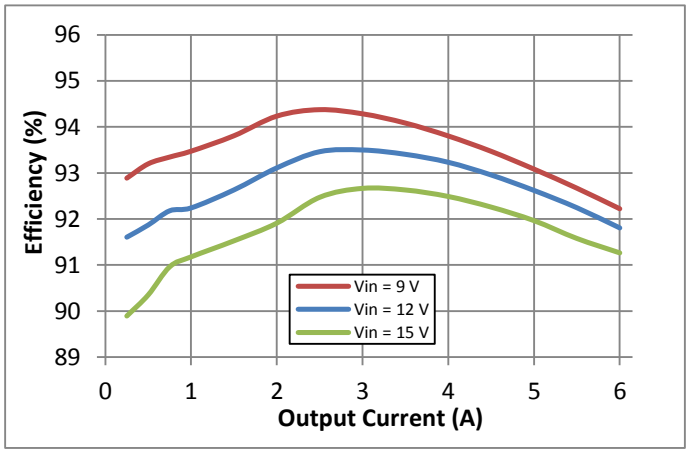



Fig. 3 Efficiency vs Output Current

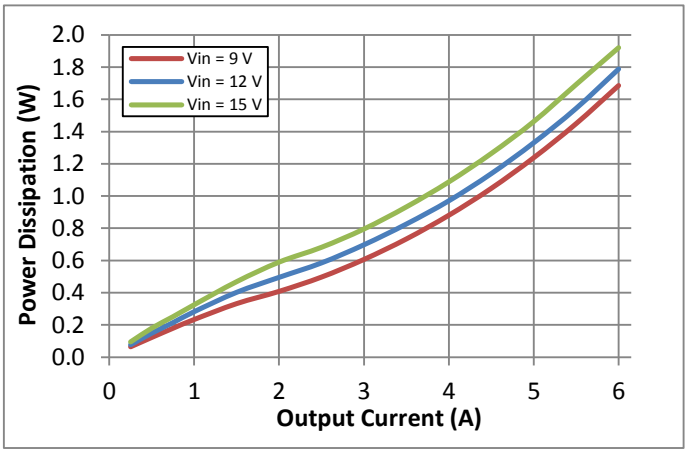



Fig. 4 Power Dissipation vs Output Current

### SPM1004-2V5, $V_{OUT}$ = 2.5V

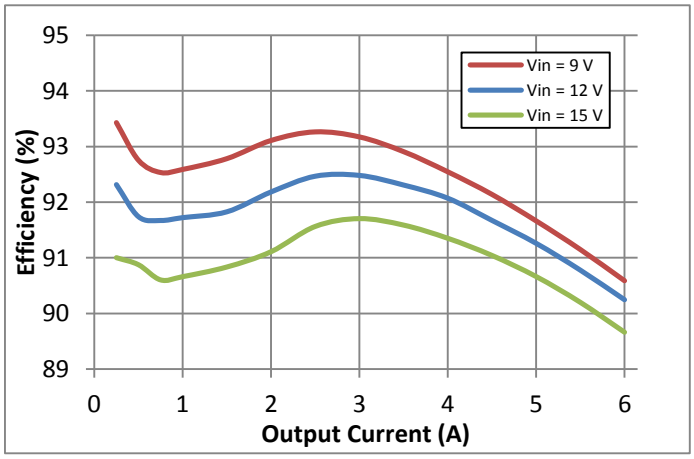



Fig. 5 Efficiency vs Output Current

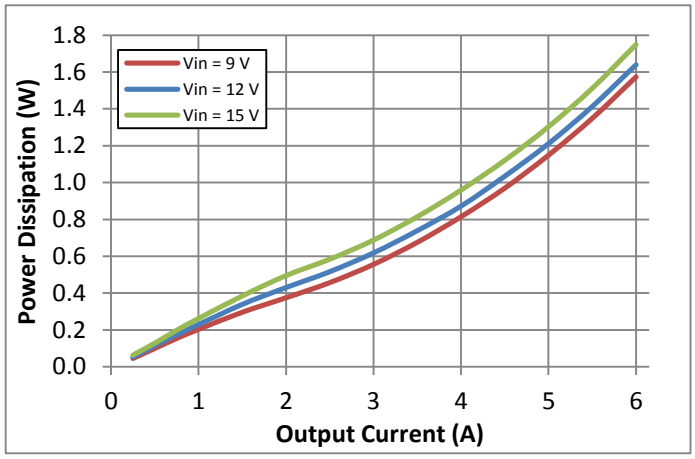



Fig. 6 Power Dissipation vs Output Current

### SPM1004-1V8, $V_{OUT}$ = 1.8V

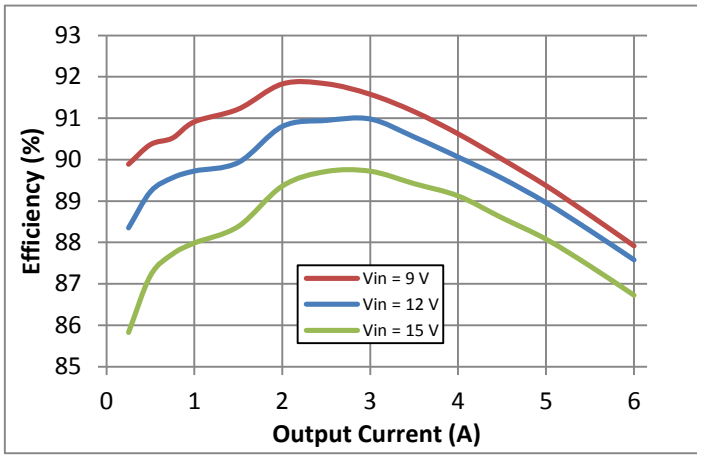



Fig. 7 Efficiency vs Output Current

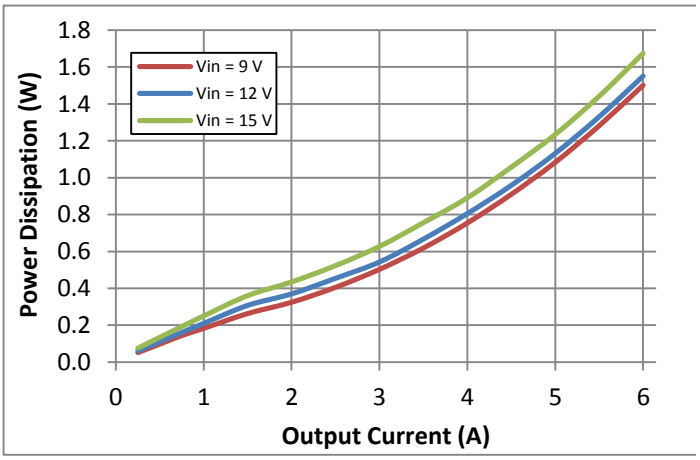



Fig. 8 Power Dissipation vs Output Current

### SPM1004-1V5, $V_{OUT}$ = 1.5V

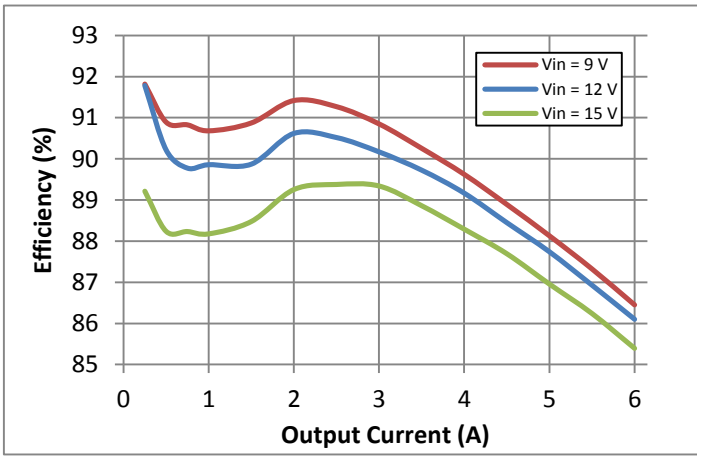



Fig. 9 Efficiency vs Output Current

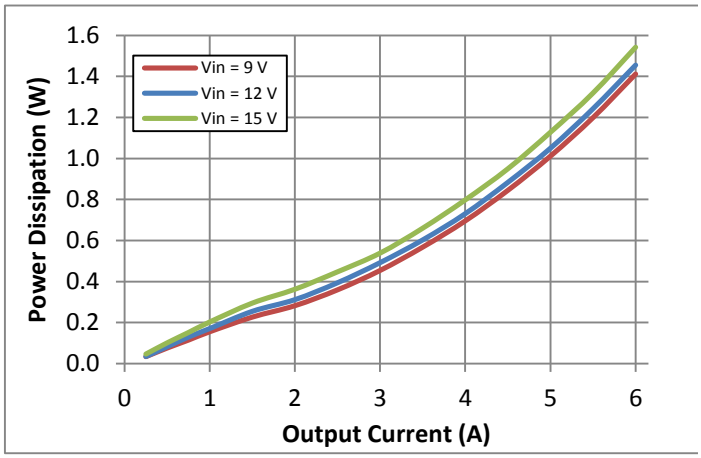



Fig. 10 Power Dissipation vs Output Current

### SPM1004-1V2, $V_{OUT}$ = 1.2V

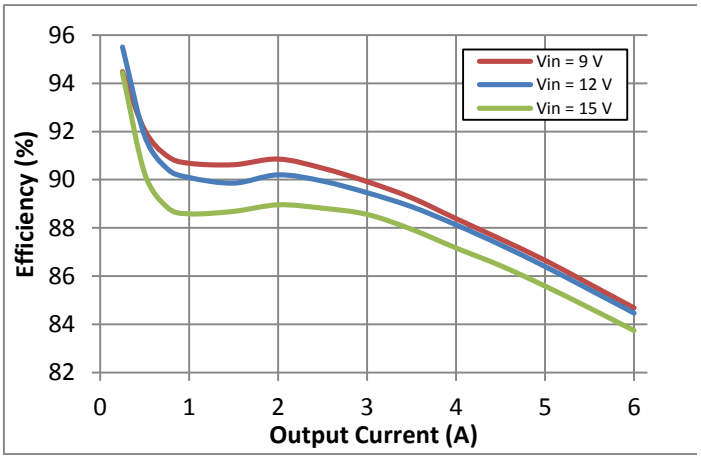



Fig. 11 Efficiency vs Output Current

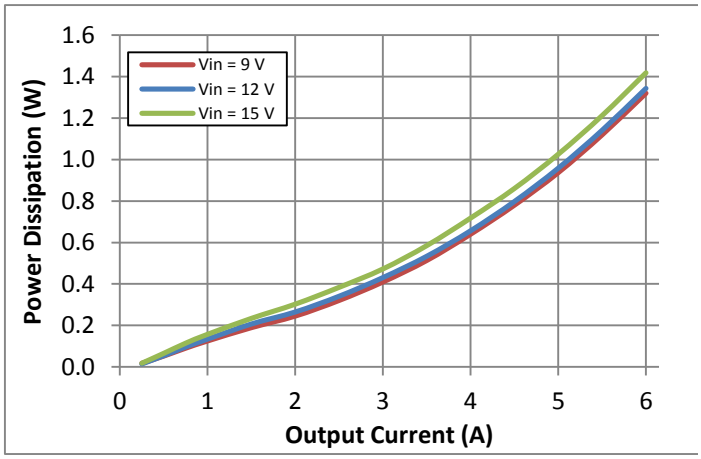



Fig. 12 Power Dissipation vs Output Current

**SPM-1004-1V0, $V_{OUT}$ = 1.0V**

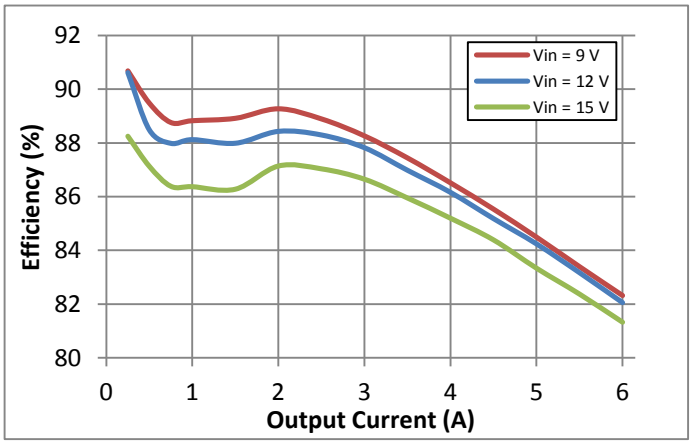



Fig. 13 Efficiency vs Output Current

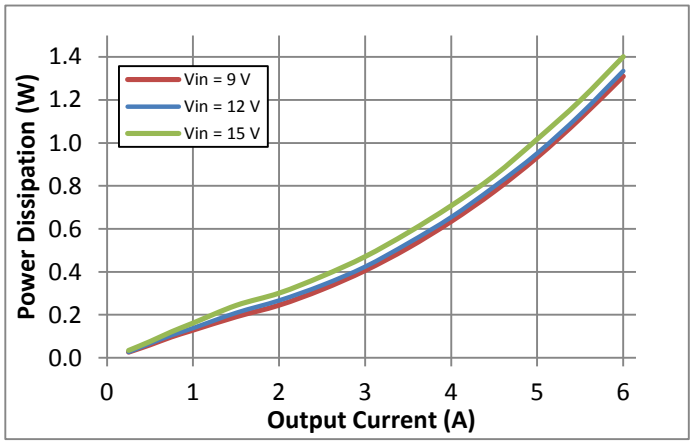



Fig. 14 Power Dissipation vs Output Current

**SPM1004-0V8, $V_{OUT}$ = 0.8V**

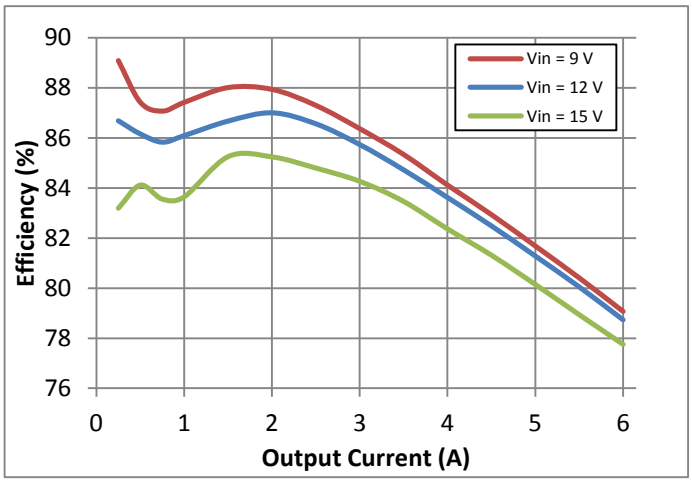



Fig. 15 Efficiency vs Output Current

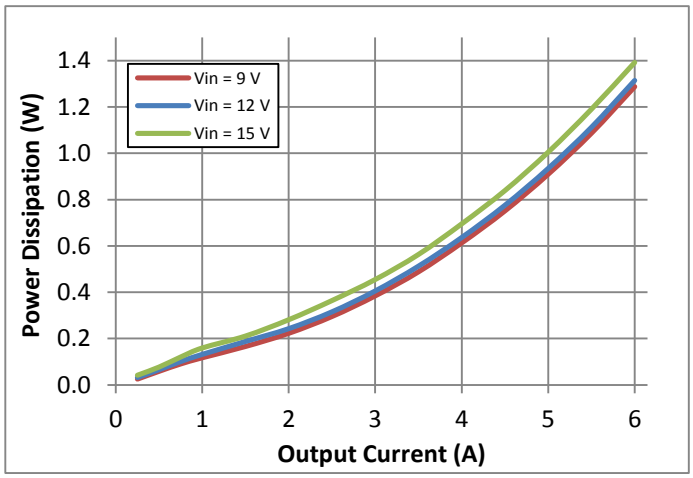



Fig. 16 Power Dissipation vs Output Current

Note 1: The above curves (Figure 1 to Figure 16) are derived from measured data taken on samples of the SPM1004 tested at room temperature (25°C), and are considered to be typical for the product.

## APPLICATION INFORMATION

## Output Voltage Adjustment

The output voltage of each model of SPM1004 can be trimmed by ±10% from its nominal value. To trim output voltage up, a resistor ($R_{UP}$) should be connected between output voltage adjustment pin (VADJ) and analog ground pin (AGND), as shown in Fig. 17. To trim output voltage down, a resistor ($R_{DOWN}$) should be connected between remote sensing pin (VSENSE) and output voltage adjustment pin (VADJ), as shown in Fig. 18. It is recommended to use 1% tolerance or better for these resistors.

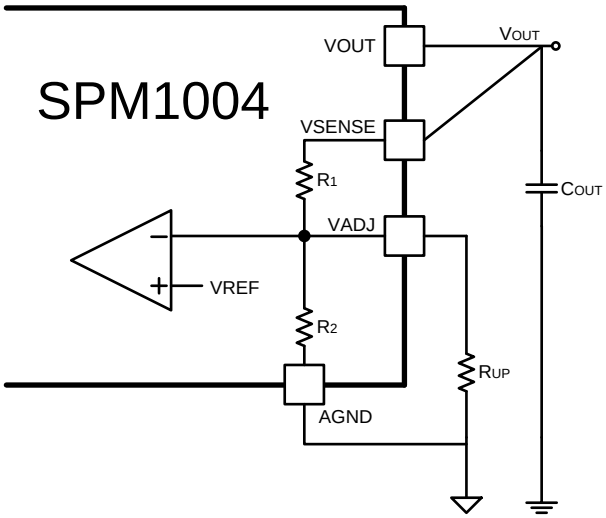



Fig. 17 Output Voltage Trim Up Circuit

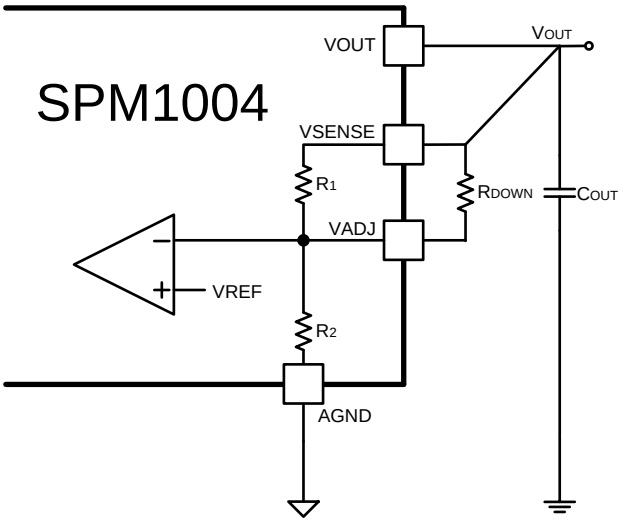



Fig. 18 Output Voltage Trim Down Circuit

Following equations can be used to calculate the trim resistor value (in kΩ) for 5V output (SPM1004-5V0). In the equation, $V_{OUT}$ is the desired output voltage. It should be within ±10% of the nominal output voltage of 5V.

SPM1004-5V0, $V_{OUT}$ = 5.0V

$$R_{UP\_5V0} = \frac{101.4}{1.964V_{OUT} - 9.65} \quad \text{(for trim up only)} \qquad \text{Eq. (1)}$$

$$R_{DOWN\_5V0} = \frac{166V_{OUT} - 101.4}{9.65 - 1.964V_{OUT}} \quad \text{(for trim down only)} \qquad \text{Eq. (2)}$$

Following equations can be used to calculate the trim resistor value (in kΩ) for 3.3V output (SPM1004-3V3). In the equation, $V_{OUT}$ is the desired output voltage. It should be within ±10% of the nominal output voltage of 3.3V.

SPM1004-3V3, $V_{OUT}$ = 3.3V

$$R_{UP\_3V3} = \frac{63.3}{1.98V_{OUT} - 6.44} \quad \text{(for trim up only)} \qquad \text{Eq. (3)}$$

$$R_{DOWN\_3V3} = \frac{103.6V_{OUT} - 63.3}{6.44 - 1.98V_{OUT}} \quad \text{(for trim down only)} \qquad \text{Eq. (4)}$$

Following equations can be used to calculate the trim resistor value (in kΩ) for 2.5V output (SPM1004-2V5). In the equation, $V_{OUT}$ is the desired output voltage. It should be within ±10% of the nominal output voltage of 2.5V.

SPM1004-2V5, $V_{OUT}$ = 2.5V

$$R_{UP\_2V5} = \frac{43.8}{1.964V_{OUT} - 4.85}$$ (for trim up only) Eq. (5)

$$R_{DOWN\_2V5} = \frac{71.7V_{OUT} - 43.8}{4.85 - 1.964V_{OUT}}$$ (for trim down only) Eq. (6)

Following equations can be used to calculate the trim resistor value (in kΩ) for 1.8V output (SPM1004-1V8). In the equation, $V_{OUT}$ is the desired output voltage. It should be within ±10% of the nominal output voltage of 1.8V.

SPM1004-1V8, $V_{OUT}$ = 1.8V

$$R_{UP\_1V8} = \frac{19.1}{1.637V_{OUT} - 2.91}$$ (for trim up only) Eq. (7)

$$R_{DOWN\_1V8} = \frac{31.26V_{OUT} - 19.1}{2.91 - 1.637V_{OUT}}$$ (for trim down only) Eq. (8)

Following equations can be used to calculate the trim resistor value (in kΩ) for 1.5V output (SPM1004-1V5). In the equation, $V_{OUT}$ is the desired output voltage. It should be within ±10% of the nominal output voltage of 1.5V.

SPM1004-1V5, $V_{OUT}$ = 1.5V

$$R_{UP\_1V5} = \frac{14.3}{1.637V_{OUT} - 2.43}$$ (for trim up only) Eq. (9)

$$R_{DOWN\_1V5} = \frac{23.4V_{OUT} - 14.3}{2.43 - 1.637V_{OUT}}$$ (for trim down only) Eq. (10)

Following equations can be used to calculate the trim resistor value (in kΩ) for 1.2V output (SPM1004-1V2). In the equation, $V_{OUT}$ is the desired output voltage. It should be within ±10% of the nominal output voltage of 1.2V.

SPM1004-1V2, $V_{OUT}$ = 1.2V

$$R_{UP\_1V2} = \frac{9.31}{1.637V_{OUT} - 1.931}$$ (for trim up only) Eq. (11)

$$R_{DOWN\_1V2} = \frac{15.2V_{OUT} - 9.31}{1.931 - 1.637V_{OUT}}$$ (for trim down only) Eq. (12)

Following equations can be used to calculate the trim resistor value (in kΩ) for 1.0V output (SPM1004-1V0). In the equation, $V_{OUT}$ is the desired output voltage. It should be within ±10% of the nominal output voltage of 1.0V.

SPM1004-1V0, $V_{OUT}$ = 1.0V

$$R_{UP\_1V0} = \frac{24.2}{3.273V_{OUT} - 3.21}$$ (for trim up only) Eq. (13)

$$R_{DOWN\_1V0} = \frac{39.6V_{OUT} - 24.2}{3.21 - 3.273V_{OUT}}$$ (for trim down only) Eq. (14)

Following equations can be used to calculate the trim resistor value (in kΩ) for 0.8V output (SPM1004-0V8). In the equation, $V_{OUT}$ is the desired output voltage. It should be within ±10% of the nominal output voltage of 0.8V.

SPM1004-0V8, $V_{OUT}$ = 0.8V

$$R_{UP\_0V8} = \frac{26}{4.91V_{OUT} - 3.866}$$ (for trim up only) Eq. (15)

$$R_{DOWN\_0V8} = \frac{42.52V_{OUT} - 26}{3.866 - 4.91V_{OUT}}$$ (for trim down only) Eq. (16)

## Power Up with and without Enable (EN) Control

The EN pin provides an external on/off control of the power module. Once the voltage at EN pin exceeds the threshold voltage (1.3V) or is left open, the power module starts operation when the input voltage is higher than the input start up voltage ($V_{START}$).

When the voltage at EN pin is pulled below the threshold voltage, the switching converter stops switching and the power module enters low quiescent current state.

If an application requires controlling the EN pin, an open drain or open collector output logic can be used to interface with the pin, as shown in Fig. 19, where high ON/OFF signal (low EN) disables the power module.

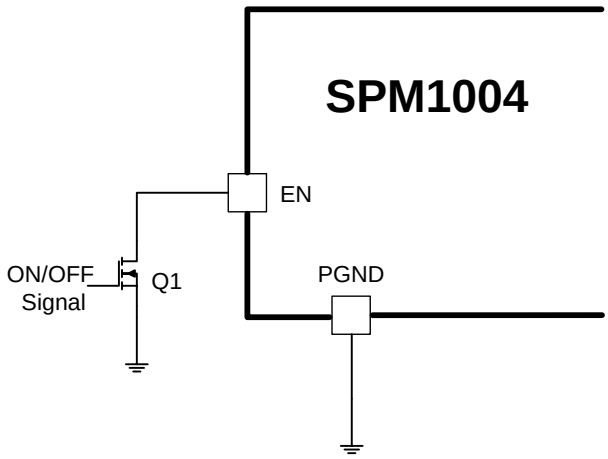



Fig. 19 Typical ON/OFF Control

When EN pin is open (or connected to a logic high voltage), SPM1004 produces a regulated output voltage following the application of a valid input voltage. Fig. 20 shows the startup waveform for SPM1004-1V8 without EN control.

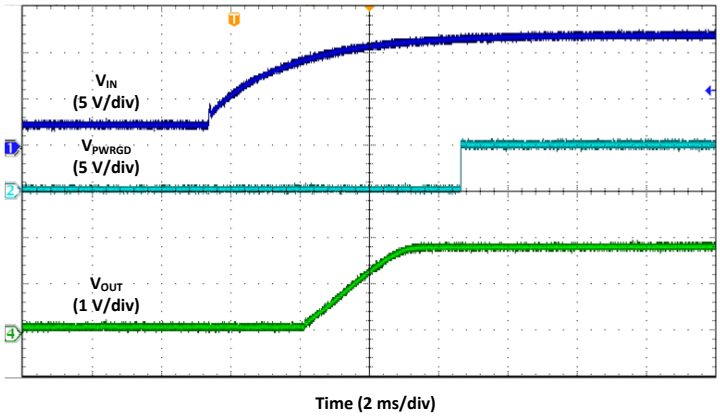



Fig. 20 Startup Waveforms for SPM1004-1V8 without EN Control

Fig. 21 and Fig. 22 show the typical output voltage waveforms when SPM1004-1V8 is turned on and turned off by the EN pin. In these figures, the top trace is enable signal (EN), the middle trace Power Good voltage (PWRGD), and the bottom trace is the output voltage.

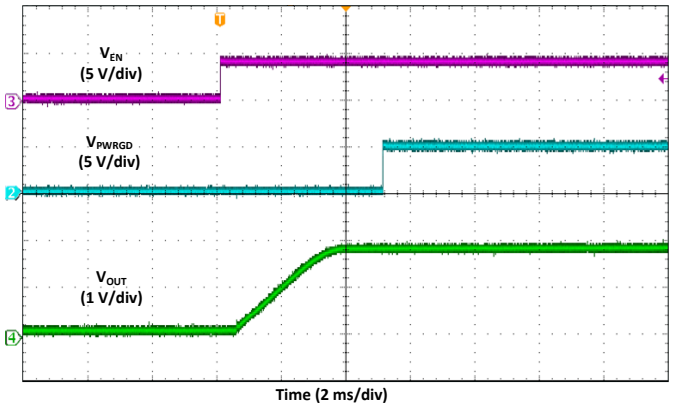



Fig. 21 Enable Turn-On for SPM1004-1V8, ($I_{OUT}$ = 6A)

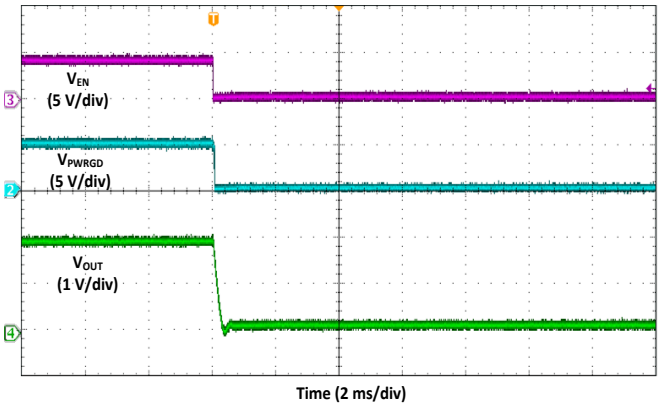



Fig. 22 Enable Turn-Off for SPM1004-1V8, ($I_{OUT}$ = 6A)

The startup and enable waveforms are similar for other output voltages.

## Startup Voltage Setup

By default, the power modules will be turned on when the input voltage reaches the startup voltage ($V_{START}$), and will be turned off when the input voltage reduces to below the Under-Voltage Lock-Out (UVLO) level. Startup voltage cannot be reduced from the values provided in the table of Electrical Characteristics. Startup voltage can be increased by an external resistor ($R_{EN}$) connected between EN pin and PGND pin.

For SPM1004-5V0, the resistor value $R_{EN}$ (in kΩ) can be calculated using (17) below based on the required startup voltage, $V_{START\_5V0}$. **Note**: $V_{START\_5V0}$ must be higher than 9V.

$$R_{EN\_5V0} = \frac{325}{2.5V_{START\_5V0} - 22.5} \qquad 17)$$

For all other models, the resistor value $R_{EN}$ (in kΩ) can be calculated using (18) below based on the required startup voltage, $V_{START}$. **Note**: $V_{START}$ must be higher than 8.5V.

$$R_{EN} = \frac{325}{2.5V_{START} - 21.3} \qquad \text{Eq. (18)}$$

## Power Good (PWRGD)

The PWRGD pin is an open drain output, and can be used to indicate when the output voltage is within the normal operating range. It is recommended to connect a pull up resistor (10KΩ to 100KΩ) between PWRGD pin and VAUX pin of the module. The PWRGD signal becomes high when the output voltage reaches 91% of normal output voltage. The PWRGD signal is pulled low when the output voltage is lower than 80% or higher than 120% of the normal output voltage.

## Soft-Start Operation (SS)

The soft-start function forces the output voltage to rise gradually to its nominal value rather than rising as rapidly as possible. When an external soft-start capacitor is not connected, the soft-start time is set to 3.3ms nominal for all the SPM1004 models. The soft-start time can be increased by connecting an external capacitor between soft-start pin (SS) and analog ground (AGND) pin. The relationship between the required soft-start time and the external capacitor is given by the following equation:

$$C_{SS}(nF) = 32.7T_{SS}(ms) - 100 \qquad \text{Eq. (19)}$$

The following table gives some typical external soft-start capacitor values for different soft-start times.

**Table 1. Soft-start capacitor values and soft-start time (typical)**

| External capacitor (nF) | open | 68 | 100 | 470 | 1000 | 2200 | 3300 |
|---|---|---|---|---|---|---|---|
| Nominal SS time (ms) | 3.3 | 5.1 | 6.6 | 17.5 | 33.6 | 70.3 | 104 |

## Application Schematics

Fig. 23 shows a typical application schematic for 12V input and 3.3V output application. The on / off of the power module is controlled by an external ON/OFF signal through a MOSFET.

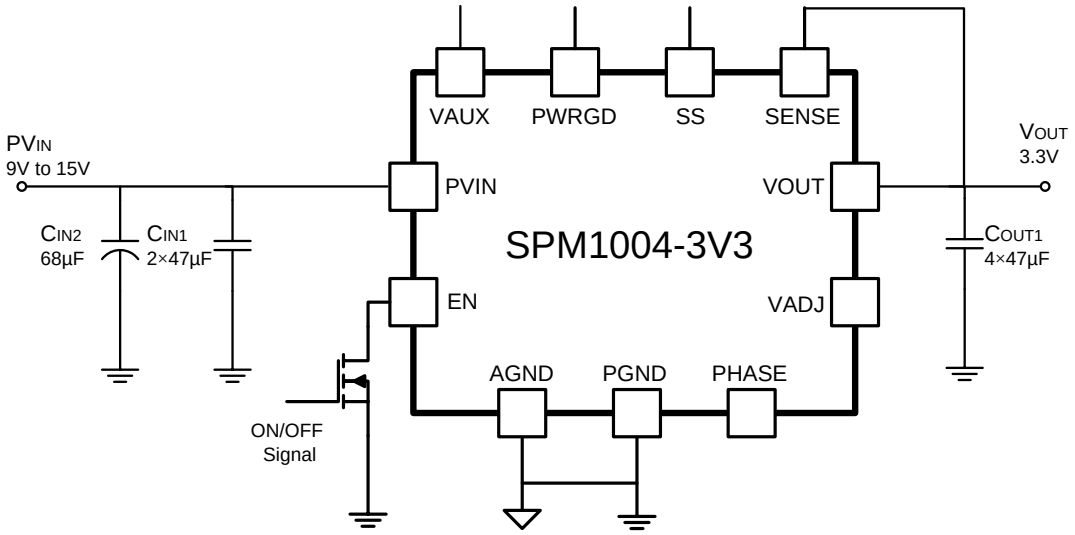



Fig. 23 Schematic for $V_{IN}$ = 12V, $V_{OUT}$ = 3.3V with External ON/OFF Signal Control

Fig. 24 shows a typical schematic for 12V input and 1.8V output application. In this example, the startup voltage has been changed to 10V with EN resistor $R_{EN}$ of 88.7kΩ. The soft-start time has been set to 17.5ms with an external soft-start capacitor of 0.47µF.

**Note**: in Fig. 23 the VSENSE pin is shown connected directly to the output capacitor $C_{OUT}$. This module uses a constant on-time control and the feedback needs to sense the output voltage ripple as accurately as possible to provide the best regulation. If there is a significant distance between the SPM1004 and the load, the bulk output capacitor should be physically located close to the load, and the VSENSE connected at that point. When the recommended capacitance of 4x 47uF is used, one capacitor can be located at the module and the other three close to the load.

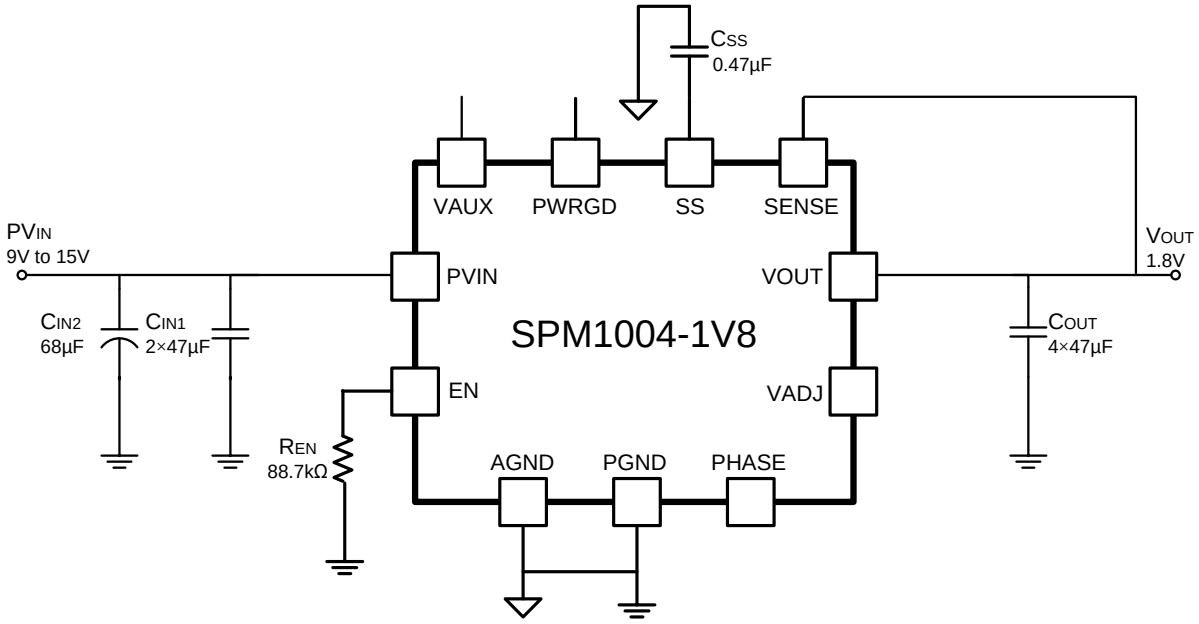



Fig. 24 Schematic for $V_{IN}$ = 12V, $V_{OUT}$ = 1.8V with Startup Voltage of 10V and Soft-start Time of 17.5ms

## Sequencing Operation

The term *sequencing* is used when two or more separate modules are configured to start one after the other, in sequence.

Sequencing operation between two or more SPM1004 power modules can be implemented with PWRGD pin and EN pin. Fig. 25 shows an example configuration when SPM1004-2V5 starts first and SPM1004-1V8 starts after the output voltage of SPM1004-2V5 has reached 2.5V. In this case, the Power Good signal (PWRGD) of SPM1004-2V5 turns on SPM1004-1V8 through the EN pin of SPM1004-1V8.

Fig. 26 shows the output voltage waveforms of two SPM1004 modules used in sequential startup mode. It shows that PWRGD signal becomes high when SPM1004-2V5 enters into regulation and then the SPM1004-1V8 starts up.

**Note**: The SPM1004 can start in sequence with another SPM1004 or with any other POL having a compatible Power Good output.

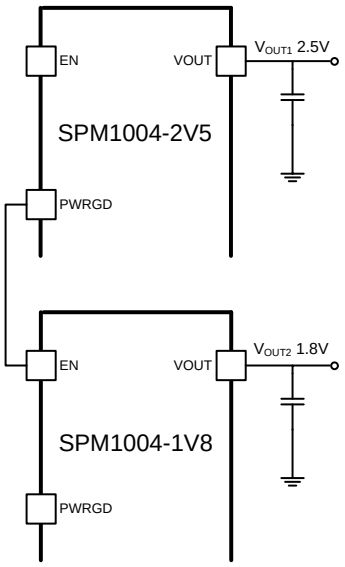



Fig. 25 Sequencing Startup Schematic, $V_{OUT1}$ = 2.5V, $V_{OUT2}$ = 1.8V

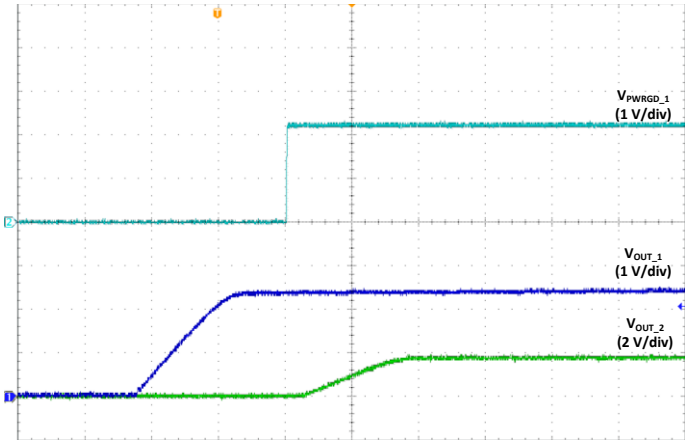



Fig. 26 Sequencing Startup Waveform, $V_{OUT1}$ = 2.5V, $V_{OUT2}$ = 1.8V

## Transient Response

SPM1004 uses Constant-On-Time (COT) control and achieves excellent transient performance. The following table summarizes the measured data for each output voltage when the load current undergoes a 3A step between 2A and 5A. The slew rate for the load current change is 1A/µs. The measured transient waveforms are given from Fig. 27 to Fig. 34.

**Table 2. Output Voltage Transient Response**

Test Conditions: $C_{IN}$ = 3 x 47µF ceramic capacitor, $C_{OUT}$ = 4 × 47µF ceramic capacitor

| Module Part Number | $V_{IN}$ | $V_{OUT}$ | 3A Load Step (2A to 5A) at 1A/µs | |
|---|---|---|---|---|
| | | | Voltage Deviation (mV) | Recovery Time (µs) |
| SPM1004-5V0 | 12V | 5V | 30 | 75 |
| SPM1004-3V3 | 12V | 3.3V | 25 | 50 |
| SPM1004-2V5 | 12V | 2.5V | 25 | 50 |
| SPM1004-1V8 | 12V | 1.8V | 20 | 50 |
| SPM1004-1V5 | 12V | 1.5V | 20 | 50 |
| SPM1004-1V2 | 12V | 1.2V | 20 | 30 |
| SPM1004-1V0 | 12V | 1.0V | 20 | 30 |
| SPM1004-0V8 | 12V | 0.8V | 20 | 25 |

The following figures show the typical output voltage waveforms when the load current undergoes a step change between 2A and 5A (3A step), showing that the SPM1004 series achieves excellent dynamic performance.

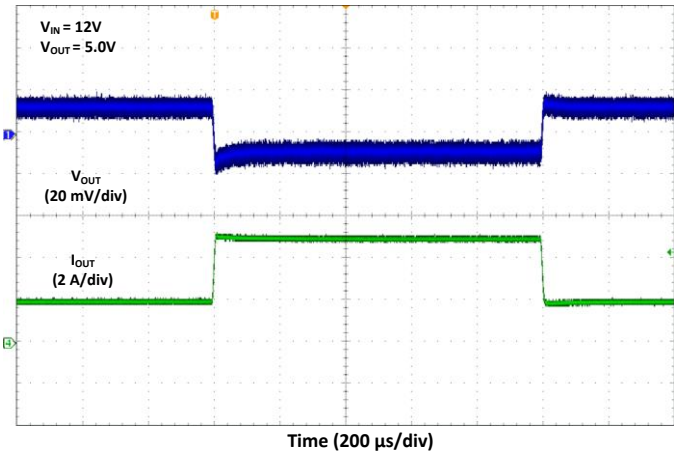



Fig. 27 SPM1004-5V0, $V_{IN}$ = 12V, $V_{OUT}$ = 5V

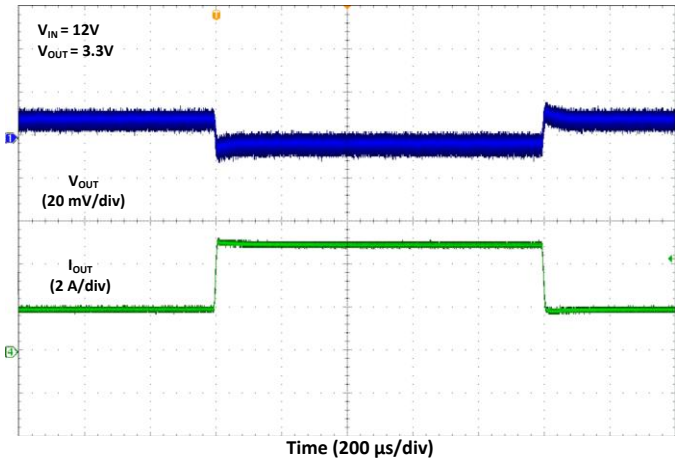



Fig. 28 SPM1004-3V3, $V_{IN}$ = 12V, $V_{OUT}$ = 3.3V

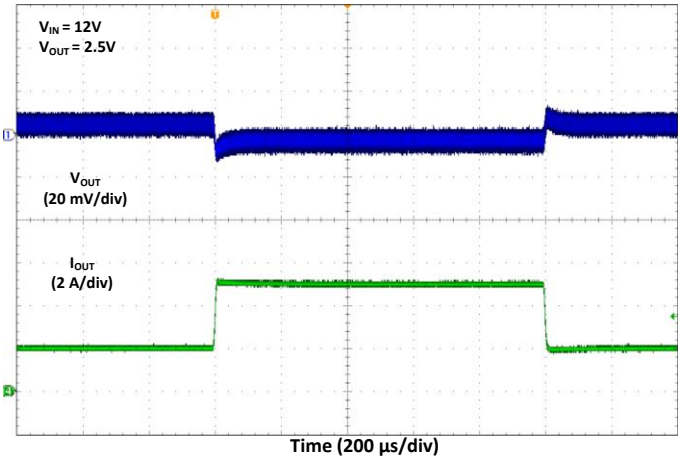



Fig. 29 SPM1004-2V5, $V_{IN}$ = 12V, $V_{OUT}$ = 2.5V

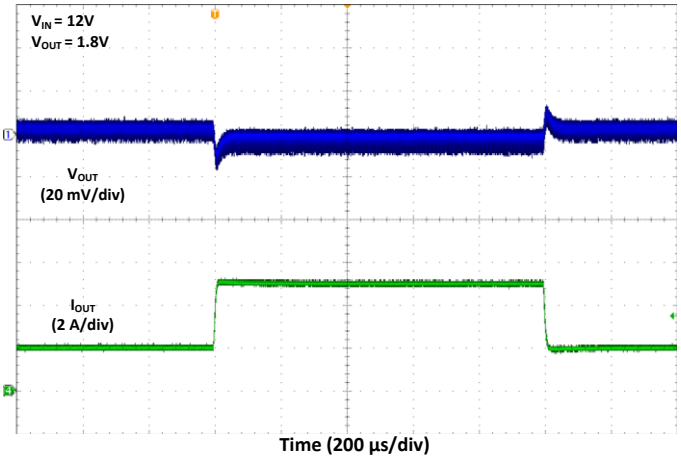



Fig. 30 SPM1004-1V8, $V_{IN}$ = 12V, $V_{OUT}$ = 1.8V

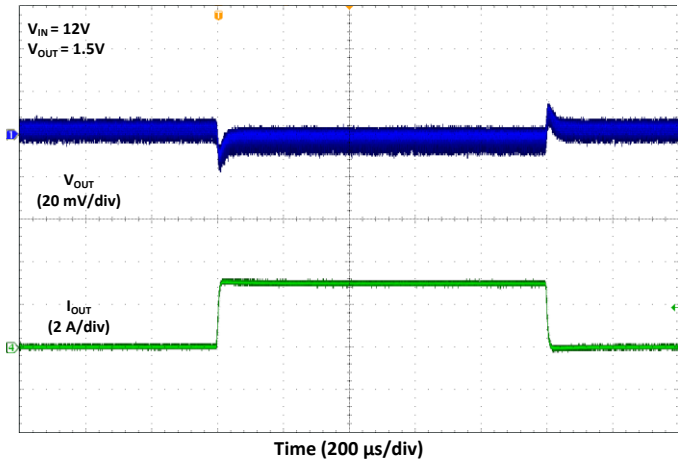



Fig. 31 SPM1004-1V5, $V_{IN}$ = 12V, $V_{OUT}$ = 1.5V

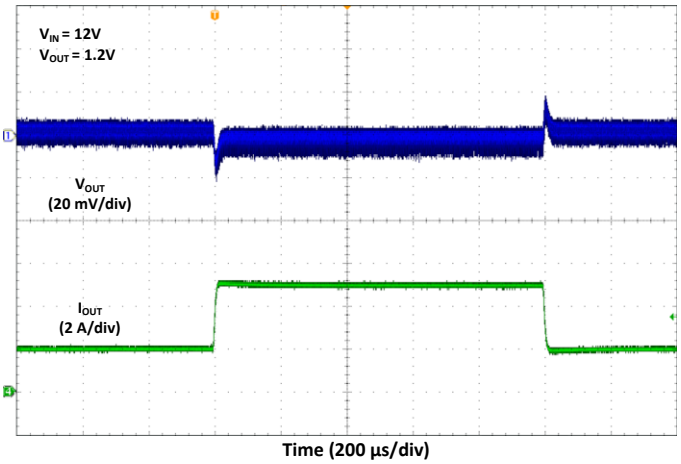



Fig. 32 SPM1004-1V2, $V_{IN}$ = 12V, $V_{OUT}$ = 1.2V

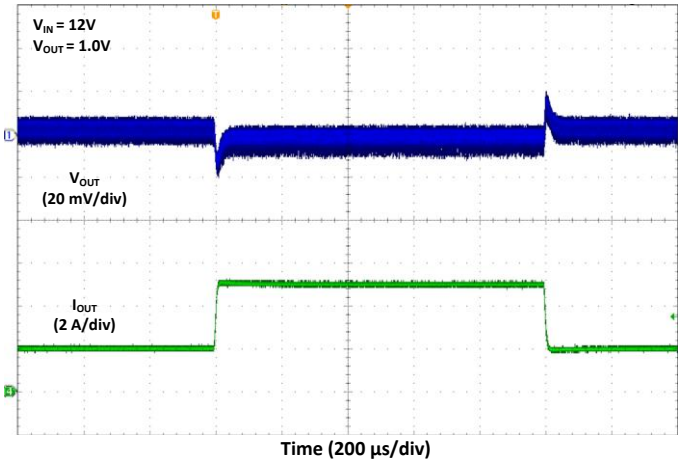



Fig. 33 SPM1004-1V0, $V_{IN}$ = 12V, $V_{OUT}$ = 1.0V

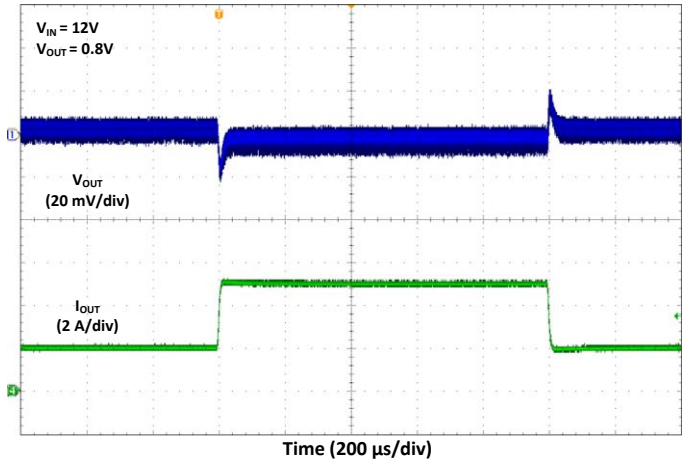



Fig. 34 SPM1004-0V8, $V_{IN}$ = 12V, $V_{OUT}$ = 0.8V

## Over Current Protection

For protection against over-current faults, SPM1004 will shut down when the load current is higher than the over-current protection (OCP) level. During an over-current condition, the SPM1004 will operate in hiccup mode and will try to restart automatically. The hiccup operation will continue until the over-current condition is removed or the input power is removed.

Fig. 35 shows the output voltage and output current waveforms during over-current protection operation for SPM1004-1V8. When the over-current condition is removed, the output voltage recovers automatically to the nominal voltage, as shown in Fig. 36.

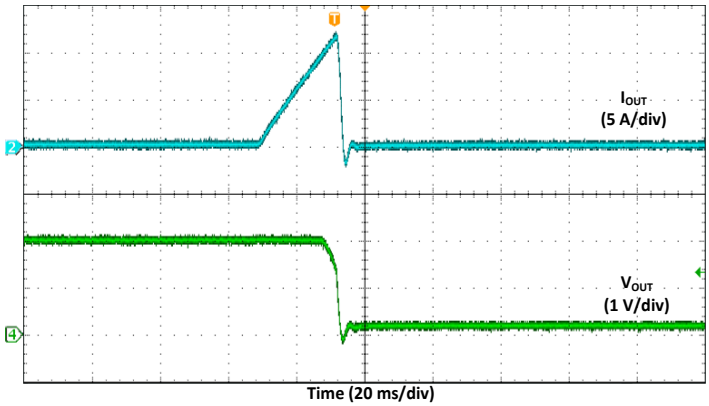



Fig. 35 $V_{OUT}$ and $I_{OUT}$ Waveforms During Over-current Shutdown

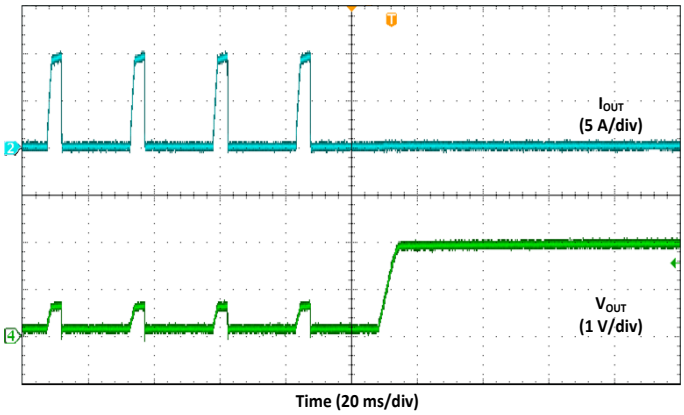



Fig. 36 Recovery from Over-current Shutdown

## Input protection

In most applications the input power source provides current limiting (typically fold-back or hiccup mode) and as long as the average fault current is limited to approximately 10A or less, no further protection is required.

If the SPM1004 is powered from a battery or other high current source, it is recommended to include an external fuse (maximum 10A) in the input to the module. The SPM1004 includes full protection against output overcurrent or short-circuit, and the fuse will not operate under any output overload condition. For more information refer to PM_AN-2 “Input Protection”.

## Thermal Considerations

The absolute maximum junction temperature is 150°C but it is recommended to keep the operating temperature well below this value. Maximum recommended case temperature is 115°C, which corresponds to a junction temperature of approximately 122°C.

The thermal resistance from case to ambient ($\theta_{CA}$) depends on the PCB layout as well as the amount of cooling airflow. When mounted on the EVM, $\theta_{CA}$ is approximately 12°C/watt in still air. Please refer to the EVM User Guide for EVM PCB layout information.

SPM1004 implements an internal thermal shutdown to protect itself against over-temperature conditions. When the junction temperature of the power MOSFET is above 170°C, the power module stops operating to protect itself from thermal damage. When the MOSFET temperature reduces to 155°C (hysteresis of 15°C), the SPM1004 will restart automatically.

## Layout Considerations

To achieve the best electrical and thermal performance, an optimized PCB layout is required. Some considerations for the PCB layout are:

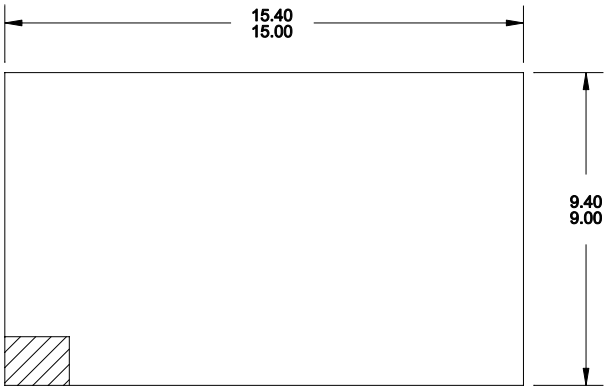
- Use large copper areas for power planes (PVIN, VOUT, and PGND) to minimize conduction loss and thermal stress;
- Place ceramic input and output capacitors close to the module pins to minimize high frequency noise;
- Place any additional output capacitors between the main ceramic capacitor and the load (see note on page 19);
- Connect AGND plane and PGND plane at a single point;
- Place resistors and capacitors connected to SENSE, VADJ, and SS pins as close as possible to their respective pins;
- Do not connect PHASE pins to any other components;
- Use multiple vias to connect the power planes to internal layers.

Refer to SPM1004 Evaluation Module (EVM) User Manual for suggested PCB layout.

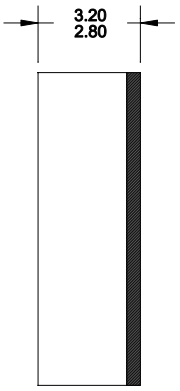
## MECHANICAL DATA

# Package Dimensions and PCB pads

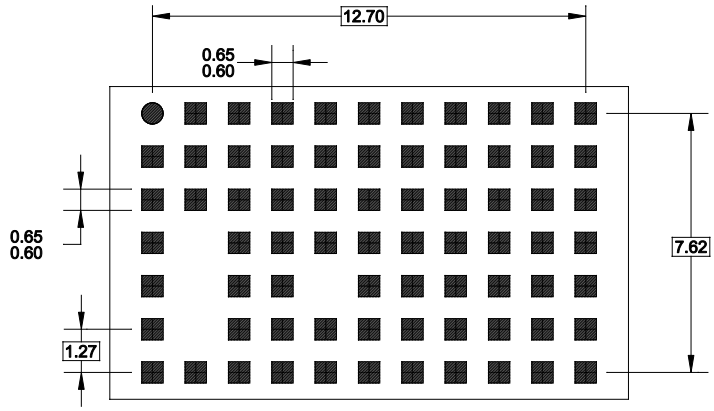
ALL DIMENSIONS IN MILLIMETERS



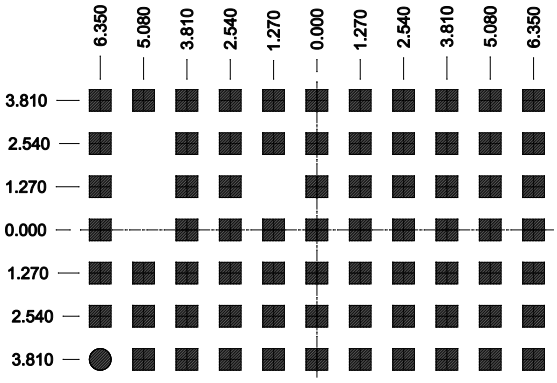

Package Top View




Package Side View




Package Bottom View




Suggested PCB Layout
Top View

## Tape and Reel Packaging Information

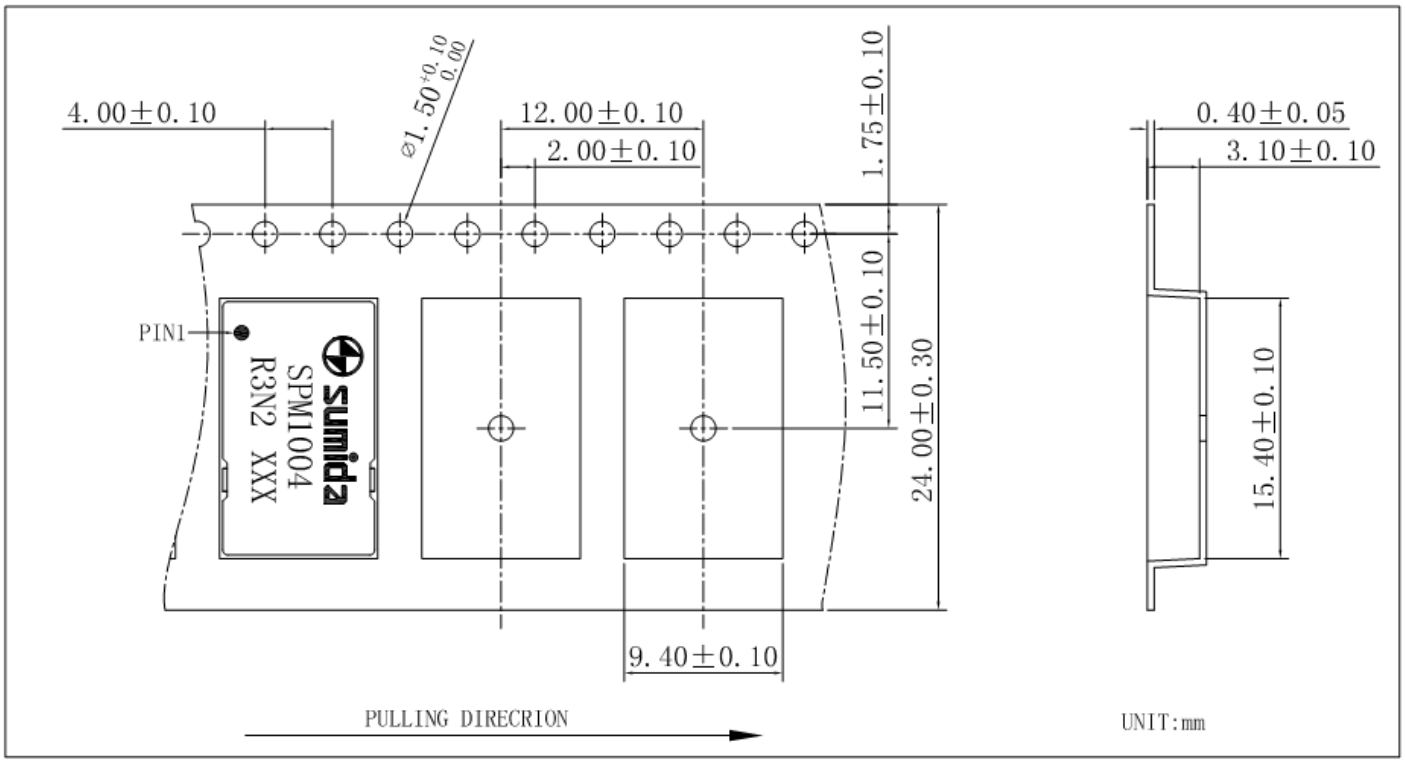



Fig. 37 Tape Dimensions and Loading Information

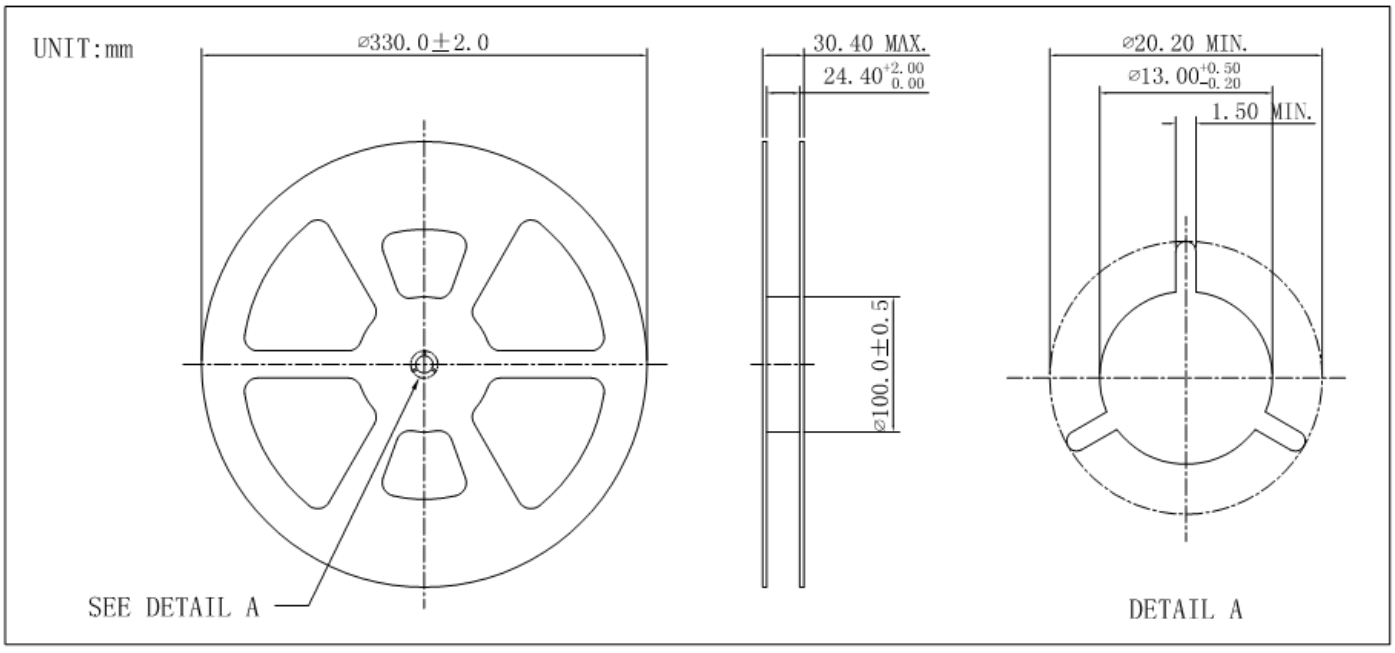



Fig. 38 Reel Dimensions

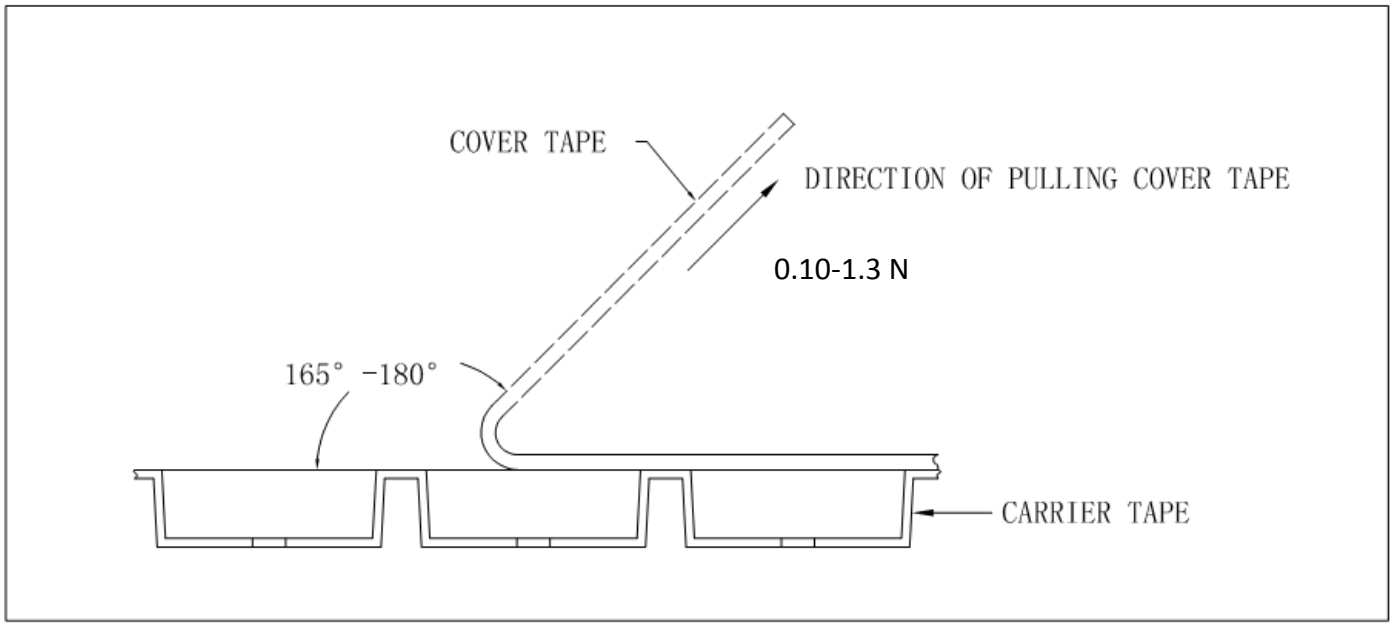



Fig. 39 Peel Speed and Strength of Cover Tape

**Note**:

1. The peel speed shall be approximately 300mm/min.
2. The peel force of the top cover tape shall be between 0.1N and 1.3N.

## Storage and handling

### Moisture barrier bag

The modules are packed in a reel, and then an aluminum foil moisture barrier bag is used to pack the reel in order to prevent moisture absorption. Silica gel is put into the aluminum moisture barrier bag as absorbent material.

### Storage

SPM1004 is classified MSL level 3 according to JEDEC J-STD-033 and J-STD-020 standards, with a floor life of 168 hours after the outer bag is opened. Any unused SPM1004 modules should be resealed in the original moisture barrier bag as soon as possible. If the module's floor life exceeds 168 hours, the modules should be dehumidified before use by baking in an oven at 125℃/1% RH (e.g. hot nitrogen gas atmosphere) for 48 hours.

### Handling precautions

1. Handle carefully to avoid unnecessary mechanical stress. Excessive external stress may cause damage.

2. Normal ESD handling procedures are recommended to be used whenever handling the module.

3. If cleaning the module is necessary, use isopropyl alcohol solution at normal room temperature. Avoid the use of other solvents.

## Reflow soldering

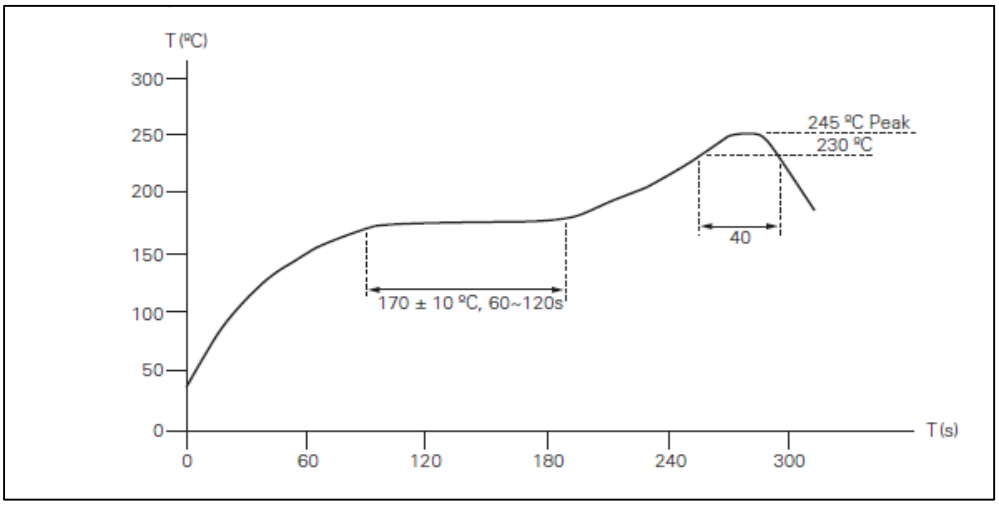



Fig. 40 Recommended Reflow Solder Profile (Lead-free)

## Ordering Information

| Output Voltage | Module Part Number | Pad Finish | Package Type | Temperature Range |
|---|---|---|---|---|
| 5.0V | SPM1004-5V0C | Au (RoHS) | LGA | -40˚C to 85˚C |
| 3.3V | SPM1004-3V3C | Au (RoHS) | LGA | -40˚C to 85˚C |
| 2.5V | SPM1004-2V5C | Au (RoHS) | LGA | -40˚C to 85˚C |
| 1.8V | SPM1004-1V8C | Au (RoHS) | LGA | -40˚C to 85˚C |
| 1.5V | SPM1004-1V5C | Au (RoHS) | LGA | -40˚C to 85˚C |
| 1.2V | SPM1004-1V2C | Au (RoHS) | LGA | -40˚C to 85˚C |
| 1.0V | SPM1004-1V0C | Au (RoHS) | LGA | -40˚C to 85˚C |
| 0.8V | SPM1004-0V8C | Au (RoHS) | LGA | -40˚C to 85˚C |