



SPN75T04

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN75T04 is the N-Channel logic enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suitable for synchronous rectifier application, Motor control power management and other Power Tool circuits. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

FEATURES

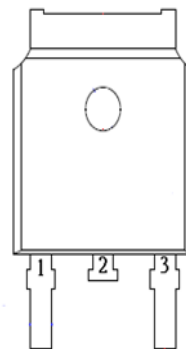
- ◆ 45V/75A, $R_{DS(ON)}=9.5m\Omega@V_{GS}=10V$
- ◆ 45V/75A, $R_{DS(ON)}=14m\Omega@V_{GS}=4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ TO-252-2L/PPAK5x6-8L package design

APPLICATIONS

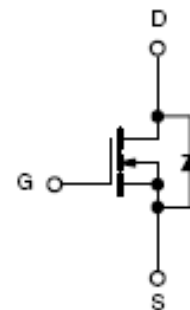
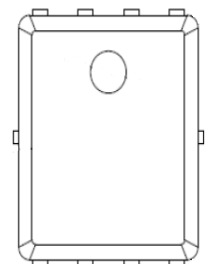
- DC/DC Converter
- Load Switch
- SMPS Secondary Side Synchronous Rectifier
- Motor Control
- Power Tool

PIN CONFIGURATION

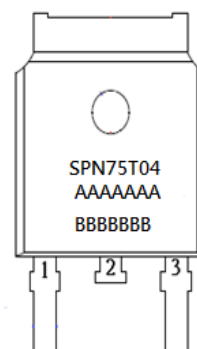
TO-252



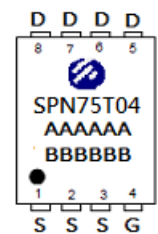
PPAK5x6



PART MARKING



A : Lot Code
B : Date Code



A : Lot Code
B : Date Code
(YY/MM/DD)



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TO-252 PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

PPAK5x6 PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN75T04T252RGB	TO-252-2L	SPN75T04
SPN75T04DN8RGB	PPAK5x6-8L	SPN75T04

※ SPN75T04T252RGB : Tube ; Pb – Free ; Halogen – Free

※ SPN75T04DN8RGB : Tape&Reel ; Pb – Free ; Halogen - Free



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ABSOLUTE MAXIMUM RATINGS

(T_A=25°C Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V _{DSS}	45	V
Gate –Source Voltage		V _{GSS}	±20	V
Continuous Drain Current (TO-220)	T _C =25°C	I _D	75	A
	T _C =100°C		58	
Continuous Drain Current (TO-251/PPAK5x6)	T _C =25°C	I _D	56	A
	T _C =100°C		39	
Pulsed Drain Current (TO-220)		I _{DM}	280	A
Pulsed Drain Current (TO-251/PPAK5x6)		I _{DM}	150	A
Power Dissipation @ T _C =25°C	TO-220-3L	P _D	104	W
Power Dissipation @ T _C =25°C	TO-252-2L		93	
Power Dissipation @ T _C =25°C	PPAK5x6-8L		83	
Avalanche Energy with Single Pulse (T _C =25°C, L=0.1mH.)		E _{AS}	141	mJ
Operating Junction Temperature		T _J	-55/150	°C
Storage Temperature Range		T _{STG}	-55/150	°C
Thermal Resistance-Junction to Case (TO-220)		R _{θJC}	1.2	°C/W
Thermal Resistance-Junction to Case (TO-252)		R _{θJC}	1.35	°C/W
Thermal Resistance-Junction to Case (PPAK5x6)		R _{θJC}	1.5	°C/W

Note :

The maximum current rating is package limited at 70A for TO-252-2L

The maximum current rating is package limited at 80A for PPAK5x6-8L



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ELECTRICAL CHARACTERISTICS

(T_A=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =250uA	45			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250uA	1.0	1.55	2.2	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =45V, V _{GS} =0V, T _J =25°C			1	uA
		V _{DS} =45V, V _{GS} =0V, T _J =100°C			100	
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =15A		7.5	9.5	mΩ
		V _{GS} =4.5V, I _D =8A		10	14	
Forward Transconductance	g _{fs}	V _{DS} =5V, I _D =10A		25		S
Gate Resistance	R _G	V _{GS} =0V, V _{DS} =Open, f=1MHz		1.5		Ω
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V		0.9	1.2	V
Dynamic						
Total Gate Charge (10V)	Q _g	V _{DS} =20V, V _{GS} =10V I _D =10A		14.5		nC
Total Gate Charge (4.5V)	Q _g			7		
Gate-Source Charge	Q _{gs}			2		
Gate-Drain Charge	Q _{gd}			2.5		
Input Capacitance	C _{iss}	V _{DS} =20V, V _{GS} =0V f=1MHz		942		pF
Output Capacitance	C _{oss}			309		
Reverse Transfer Capacitance	C _{rss}			29		
Turn-On Time	t _{d(on)}	V _{DD} =20V, I _D =10A, V _{GS} =10V R _G =10Ω		6		nS
	t _r			5		
Turn-Off Time	t _{d(off)}			21		
	t _f			5		
Gate resistance	R _g	V _{GS} =0V, V _{DS} =0V, f=1MHz		1.5		Ω



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TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

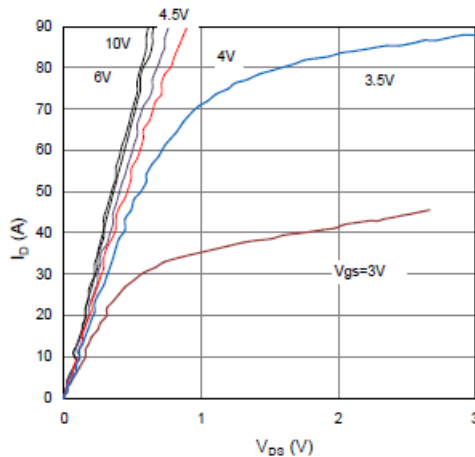


Figure 2. On-Resistance vs. Gate-Source Voltage

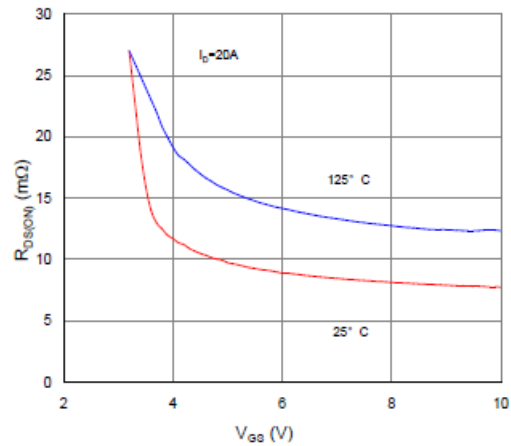


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

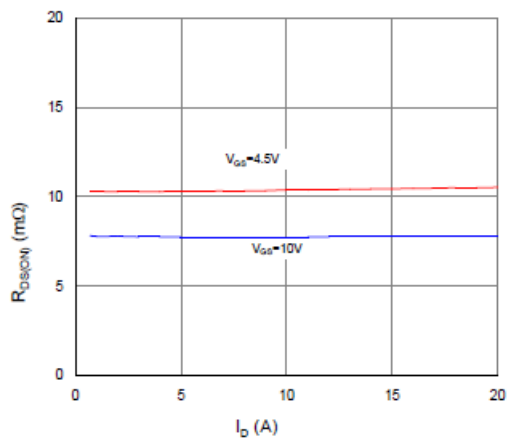


Figure 4. Normalized On-Resistance vs. Junction Temperature

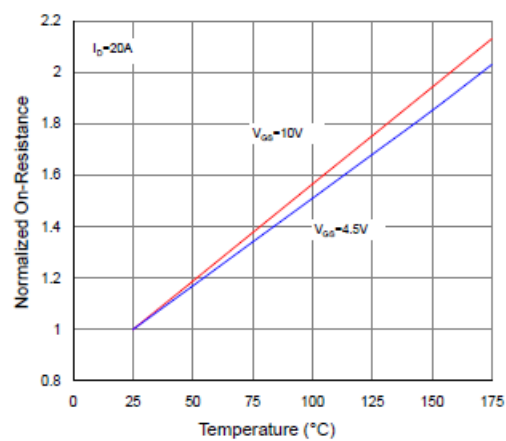


Figure 5. Typical Transfer Characteristics

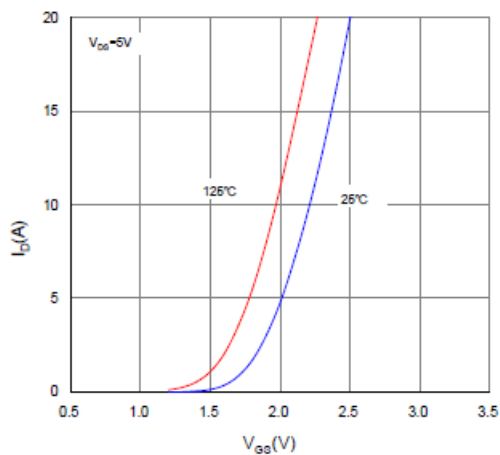
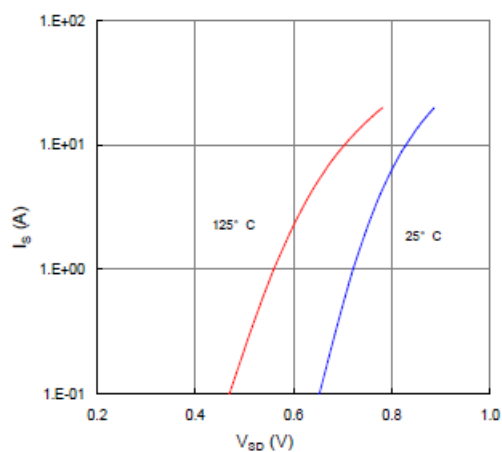


Figure 6. Typical Source-Drain Diode Forward Voltage





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TYPICAL CHARACTERISTICS

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

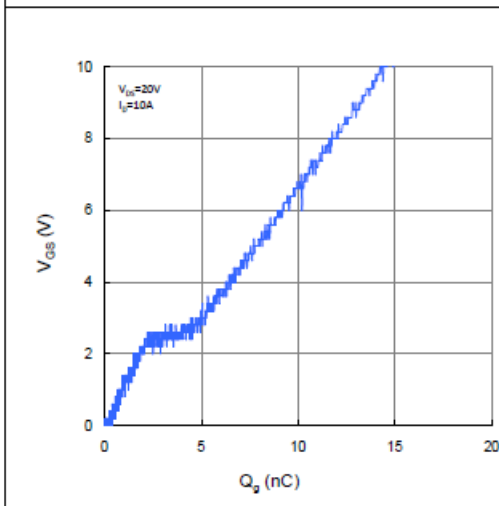


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

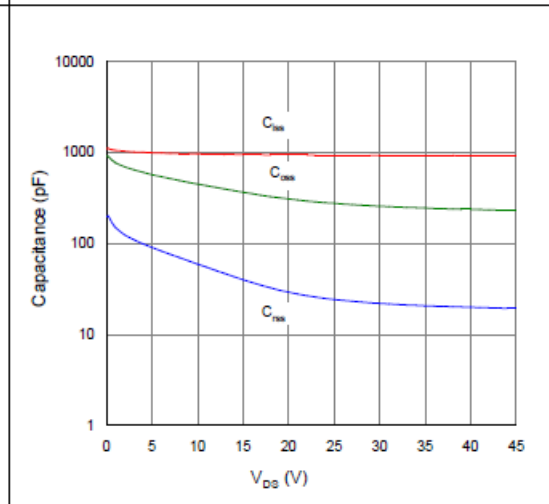


Figure 9. Maximum Safe Operating Area

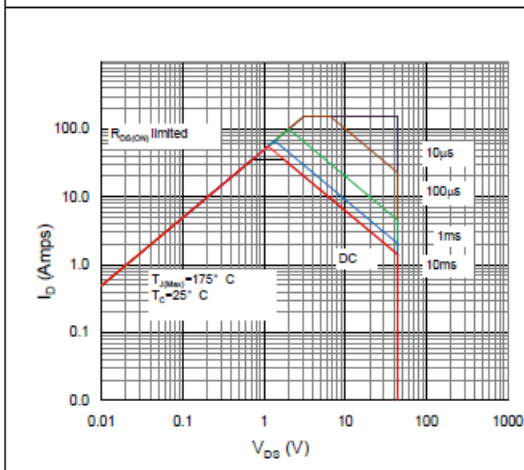


Figure 10. Maximum Drain Current vs. Case Temperature

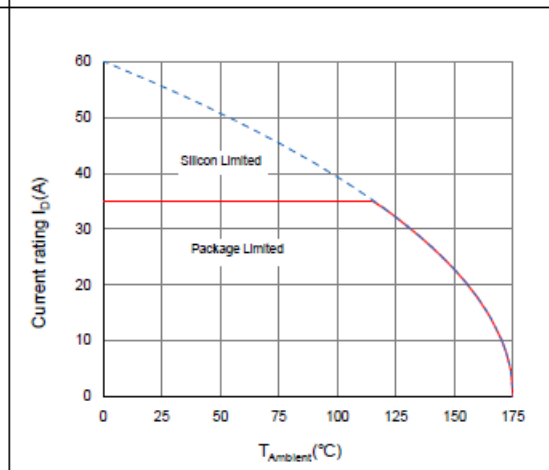
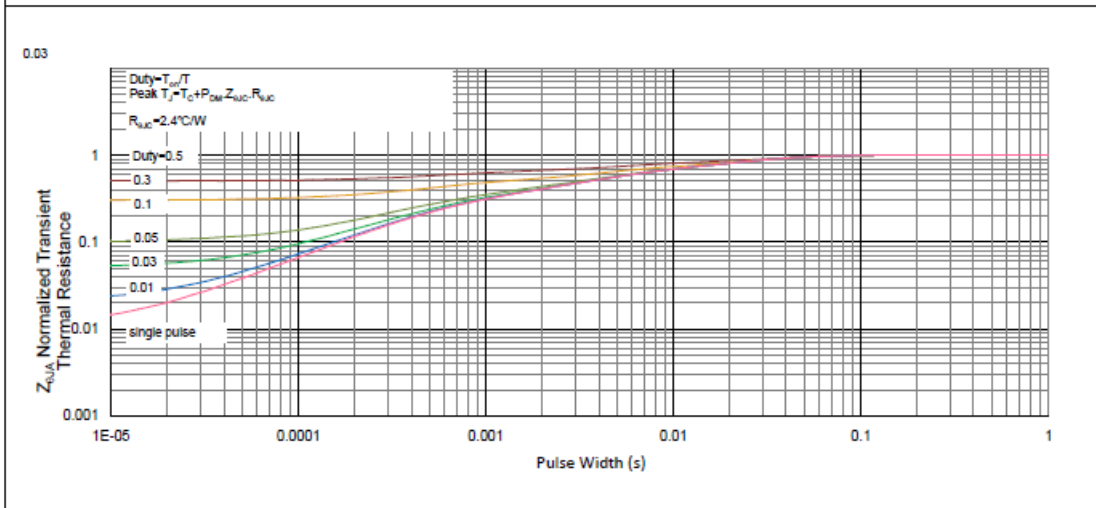


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient

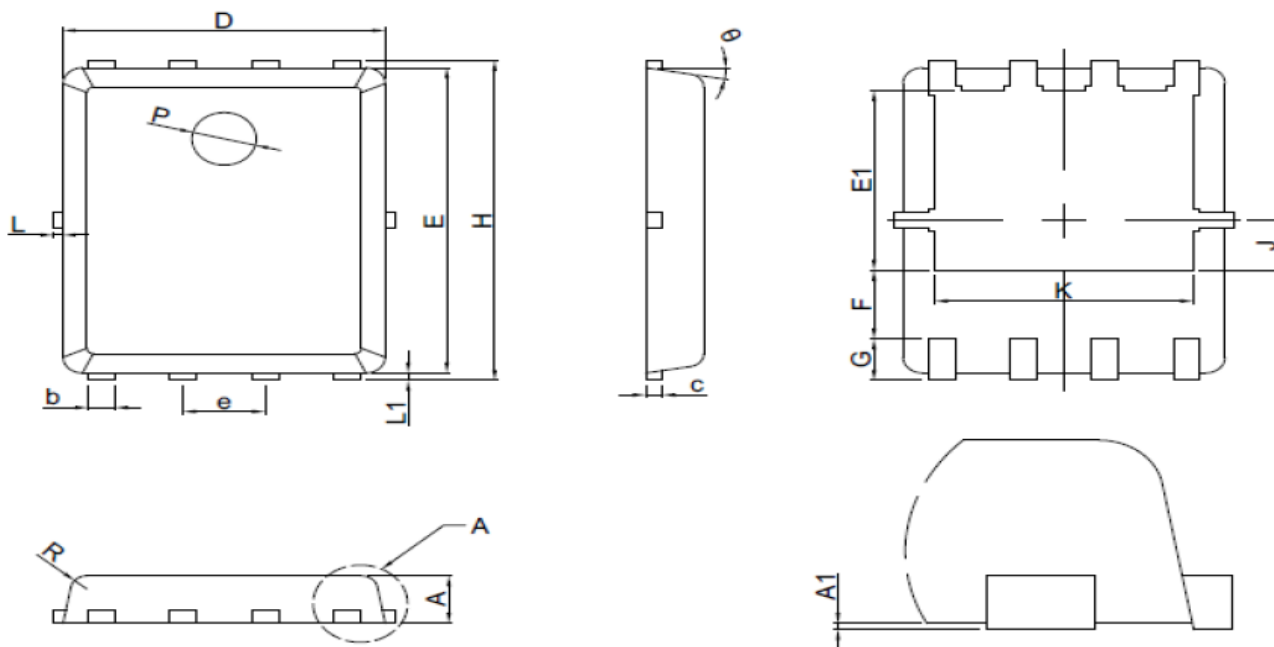




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PPAK5x6-8L PACKAGE OUTLINE



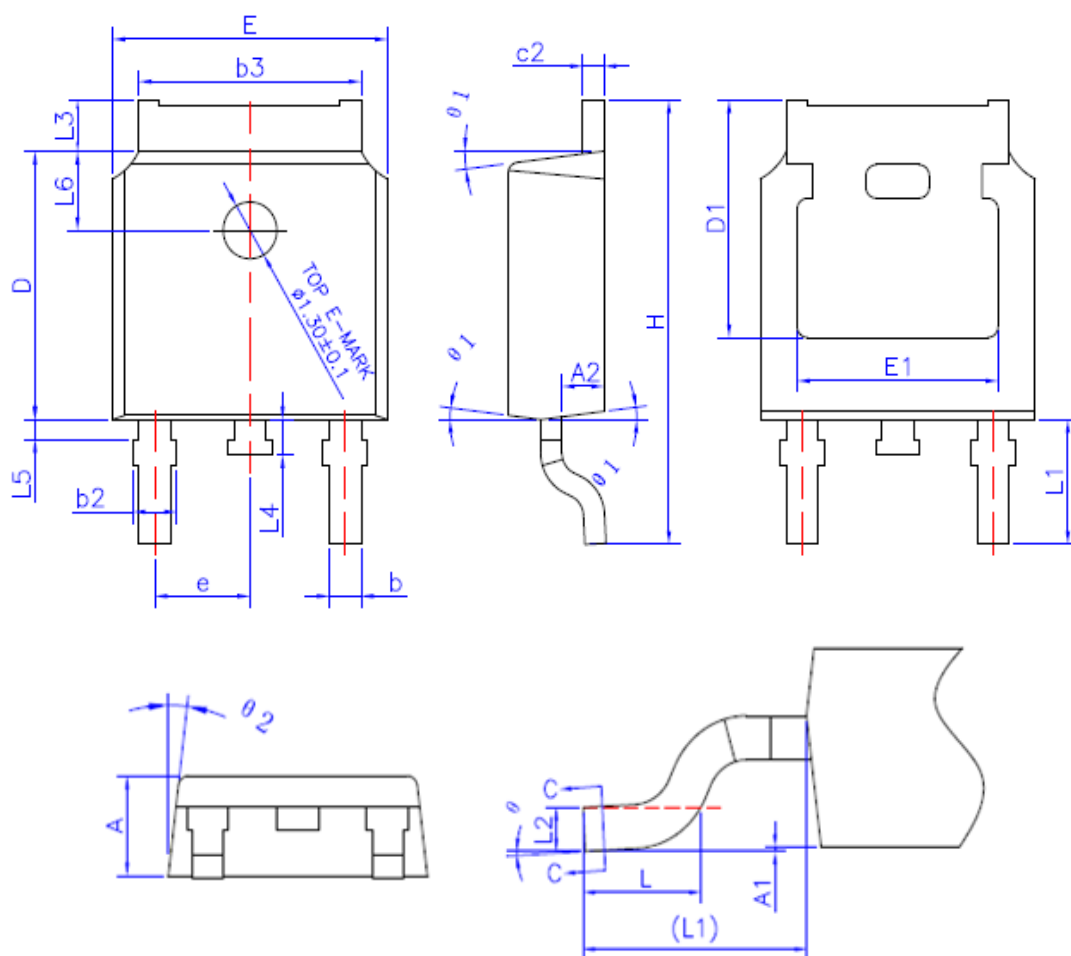
SYMBOL	MILLIMETERS		
	MIN	NOM	MAX
A	0.8	0.95	1.1
A1	0.00	0.03	0.05
b	0.33	0.41	0.51
c	0.254 REF		
D	4.80	4.95	5.10
F	1.40 REF		
E	5.70	5.80	5.90
e	1.27 BSC		
H	5.90	6.05	6.20
L1	0.06	0.13	0.20
G	0.60 REF		
J	0.95 BSC		
K	4.00 REF		
L	---	----	0.20
P	1.00 REF		
E1	3.40REF		
E2	0.95 REF		
θ	6°	10°	14°
R	0.25REF		



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TO-252-2L PACKAGE OUTLINE



SYMBOL	MIN	NOM	MAX
A	2.20	2.30	2.40
A1	0.00	--	0.15
A2	0.90	1.01	1.10
b	0.72	--	0.85
b2	0.72	--	0.90
b3	5.13	5.33	5.46
c	0.47	--	0.60
c2	0.47	--	0.60
D	6.00	6.10	6.20
D1	5.25	--	--
E	6.40	6.60	6.80
E1	4.70	--	--
e	2.3REF		
H	9.80	10.10	10.40
L	1.40	1.60	1.80
L1	2.90REF		
L2	0.508BSC		
L3	0.90	--	1.25
L4	0.60	0.80	1.00
L5	0.15	--	0.75
L6	1.80REF		
θ	0°	3°	8°
$\theta 1$	5°	7°	9°
$\theta 2$	5°	7°	9°



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SYNC Power Corporation

7F-2, No.3-1, Park Street

NanKang District (NKSP), Taipei, Taiwan 115

Phone: 886-2-2655-8178

Fax: 886-2-2655-8468

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