TPS22968x-Q1 5.5-V, 4-A, 27-mΩ On-Resistance Load Switch

1 Features

- Integrated Dual Channel Load Switch
- Qualified for Automotive Applications:
  - Device Temperature Grade 1 : –40°C to +125°C Ambient Operating Temperature Range
- Input Voltage Range: 0.8 to 5.5 V
- VBIAS Voltage Range: 2.5 to 5.5 V
- On-Resistance
  - R_{ON} = 29 mΩ at V_{IN} = 5 V (V_{BIAS} = 5 V)
  - R_{ON} = 27 mΩ at V_{IN} = 3.3 V (V_{BIAS} = 5 V)
  - R_{ON} = 26 mΩ at V_{IN} = 1.8 V (V_{BIAS} = 5 V)
- 4-A Maximum Continuous Switch Current per Channel
- Low Quiescent Current
  - 58-µA at V_{BIAS} = 5 V (Both Channels)
- Low-Control Input-Threshold Enables Use of 1.2-, 1.8-, 2.5-, 3.3- V Logic
- Configurable Rise Time With CT Pin(1)
- Quick-Output Discharge (QOD)(2) (TPS22968-Q1 Only)
- 10-Pin WSON Package With Wettable Flanks
- ESD Performance Tested per JEDEC STD
  - ±2-kV HBM and ±1-kV CDM
- Latch-Up Performance meets 100-mA per JESD 78, Class II
- GPIO Enable – Active High

(1) See *Adjustable Rise Time* for CT value versus rise time

(2) This feature discharges output of the switch to GND through a 270-Ω resistor, preventing the output from floating.

2 Applications

- Automotive Electronics
- Infotainment
- Cluster
- ADAS

3 Description

The TPS22968x-Q1 is a small, dual-channel load switch with configurable rise time. The device contains two N-channel MOSFETs that can operate over an input voltage range of 0.8 V to 5.5 V and can support a maximum continuous current of 4-A per channel. Each switch is independently controlled by an on/off input (ON1 and ON2), which is capable of interfacing directly with low-voltage control signals. The TPS22968-Q1 includes a 270 Ω on-chip resistor for quick output discharge when the switch is turned off.

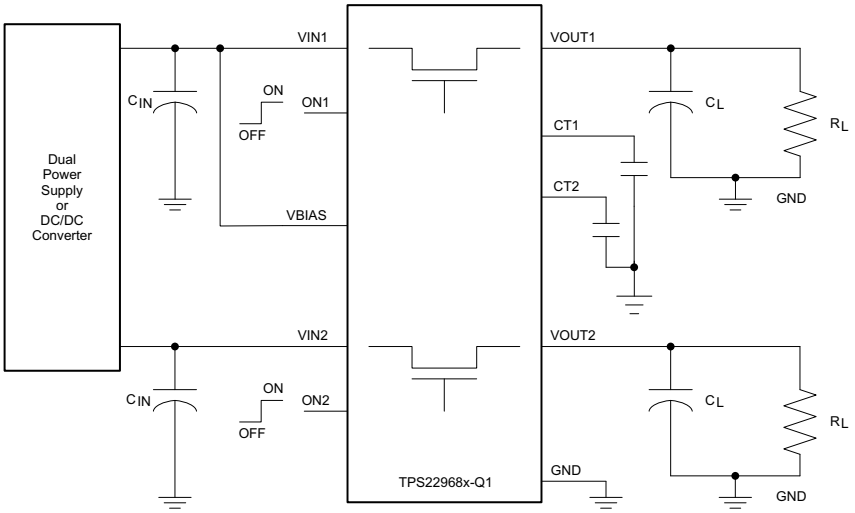
The TPS22968x-Q1 is available in a small, space-saving package (DMG) with wettable flanks and an integrated thermal pad. The wettable flanks allow for visual solder inspection. The device is characterized for operation over the free-air temperature range of –40 to +125°C.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22968-Q1 TPS22968N-Q1	WSON (10)	2.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2015) to Revision B	Page
• Added new Device TPS22968N-Q1	1

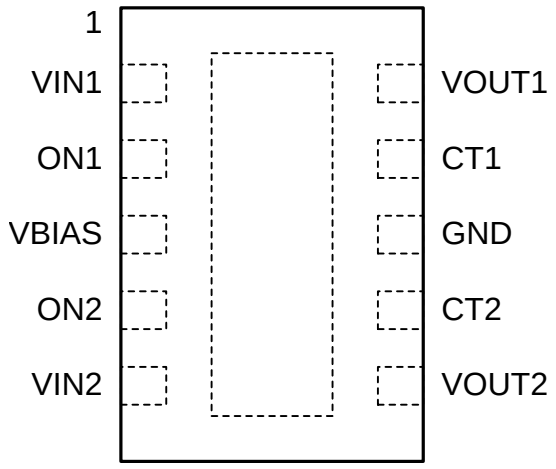
Changes from Original (November 2014) to Revision A	Page
• Changed device status from *Product Preview* to *Production Data*	1

5 Device Comparison Table

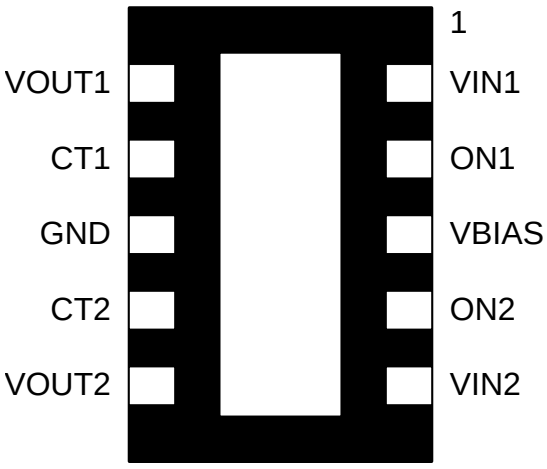
DEVICE	Ron (typ) at VIN = 3.3 V, VBIAS = 5.0 V	QUICK OUTPUT DISCHARGE	MAXIMUM OUTPUT CURRENT	ENABLE
TPS22968-Q1	27 mΩ	Yes	4 A	Active High
TPS22968N-Q1	27 mΩ	No	4 A	Active High

6 Pin Configuration and Functions

DMG Package
10-Pin WSON
Top View



DMG Package
10-Pin WSON
Bottom View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VIN1	I	Switch 1 input. Bypass this input with a ceramic capacitor to GND.
2	ON1	I	Active-high switch 1 control input. Do not leave floating.
3	VBIAS	I	Bias voltage. Power supply to the device. Recommended voltage range for this pin is 2.5 to 5.5 V. See *V_{IN} and V_{BIAS} Voltage Range* section.
4	ON2	I	Active-high switch 2 control input. Do not leave floating.
5	VIN2	I	Switch 2 input. Bypass this input with a ceramic capacitor to GND.
6	VOUT2	O	Switch 2 output
7	CT2	O	Switch 2 slew rate control. Can be left floating.
8	GND	—	Ground
9	CT1	O	Switch 1 slew rate control. Can be left floating.
10	VOUT1	O	Switch 1 output
—	Thermal Pad	—	Thermal pad (exposed center pad) to alleviate thermal stress. Tie to GND. See *Layout Guidelines* section.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
$V_{IN1,2}$	Input voltage	–0.3	6	V
V_{BIAS}	Bias voltage	–0.3	6	V
$V_{OUT1,2}$	Output voltage	–0.3	6	V
$V_{ON1,2}$	ON voltage	–0.3	6	V
I_{MAX}	Maximum continuous switch current per channel, T_A = 50 °C		4	A
I_{PLS}	Maximum pulsed switch current, pulse <300 µs, 2% duty cycle		6	A
T_J	Maximum junction temperature		150	°C
T_{LEAD}	Maximum lead temperature (10-s soldering time)		300	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
$V_{IN1,2}$	Input voltage range		0.8	V_{BIAS}	V
V_{BIAS}	Bias voltage range		2.5	5.5	V
$V_{ON1,2}$	ON voltage range		0	5.5	V
$V_{OUT1,2}$	Output voltage range			V_{IN}	V
$V_{IH,\ ON1,2}$	High-level input voltage, ON1,2	V_{BIAS} = 2.5 to 5.5 V	1.2	5.5	V
$V_{IL,\ ON1,2}$	Low-level input voltage, ON1,2	V_{BIAS} = 2.5 to 5.5 V	0	0.5	V
$C_{IN1,2}$	Input capacitor		1 (1)		µF
T_A	Operating free-air temperature (2)		–40	125	°C

(1) Refer to *Application Information*.
(2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [$T_{A(max)}$] is dependent on the maximum operating junction temperature [$T_{J(max)}$], the maximum power dissipation of the device in the application [$P_{D(max)}$], and the junction-to-ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A(max)} = T_{J(max)} - (R_{\theta JA} \times P_{D(max)})$.

7.4 Thermal Information

THERMAL METRIC (1) (2)		TPS22968x-Q1 DMG (WSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	55.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	71	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

Thermal Information (continued)

THERMAL METRIC (1) (2)		TPS22968x-Q1 DMG (WSON) 10 PINS	UNIT
ψ_{JB}	Junction-to-board characterization parameter	21.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.3	°C/W

7.5 Electrical Characteristics (V_{BIAS} = 5 V)

V_{BIAS} = 5 V. Typical values are for T_A = 25°C, unless otherwise noted

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
$I_{Q, VBIAS}$	V_{BIAS} quiescent current (both channels)	I_{OUT1} = I_{OUT2} = 0 A, $V_{IN1,2}$ = $V_{ON1,2}$ = V_{BIAS} = 5 V		–40°C to +85°C		58	70	µA
				–40°C to +125°C			70	
	V_{BIAS} quiescent current (single channel)	I_{OUT1} = I_{OUT2} = 0 A, V_{ON2} = 0 V, $V_{IN1,2}$ = V_{ON1} = V_{BIAS} = 5 V		–40°C to +85°C		58	68	µA
				–40°C to +125°C			68	
$I_{SD, VBIAS}$	V_{BIAS} shutdown current	$V_{ON1,2}$ = 0 V, $V_{OUT1,2}$ = 0 V		–40°C to +85°C		1	2	µA
				–40°C to +125°C			2	
$I_{SD, VIN1,2}$	$V_{IN1,2}$ shutdown current (per channel)	$V_{ON1,2}$ = 0 V, $V_{OUT1,2}$ = 0 V	$V_{IN1,2}$ = 5 V	–40°C to +85°C		0.5	8	µA
				–40°C to +125°C			36	
			$V_{IN1,2}$ = 3.3 V	–40°C to +85°C		0.1	3	
				–40°C to +125°C			13	
			$V_{IN1,2}$ = 1.8 V	–40°C to +85°C		0.07	2	
				–40°C to +125°C			6	
			$V_{IN1,2}$ = 1.2 V	–40°C to +85°C		0.05	1	
				–40°C to +125°C			4	
			$V_{IN1,2}$ = 0.8 V	–40°C to +85°C		0.04	1	
				–40°C to +125°C			4	
$I_{ON1,2}$	ON pin input leakage current	V_{ON} = 5.5 V		–40°C to +125°C			0.1	µA
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance	I_{OUT} = –200 mA, V_{BIAS} = 5 V	V_{IN} = 5 V	25°C		29	35	mΩ
				–40°C to +85°C			40	
				–40°C to +125°C			43	
			V_{IN} = 3.3 V	25°C		27	32	mΩ
				–40°C to +85°C			36	
				–40°C to +125°C			40	
			V_{IN} = 1.8 V	25°C		26	32	mΩ
				–40°C to +85°C			36	
				–40°C to +125°C			39	
			V_{IN} = 1.2 V	25°C		26	32	mΩ
				–40°C to +85°C			36	
				–40°C to +125°C			39	
			V_{IN} = 0.8 V	25°C		26	32	mΩ
				–40°C to +85°C			36	
				–40°C to +125°C			39	
R_{PD} (1)	Output pulldown resistance	V_{IN} = 5 V, V_{ON} = 0 V, I_{OUT} = 5 mA		–40°C to +125°C		270	320	Ω

(1) The TPS22968N-Q1 device does not feature an output pulldown resistance R_{PD}

7.6 Electrical Characteristics (V_{BIAS} = 3.3 V)

V_{BIAS} = 3.3 V. Typical values are for T_A = 25°C, unless otherwise noted

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
$I_{Q, VBIAS}$	V_{BIAS} quiescent current (both channels)	I_{OUT1} = I_{OUT2} = 0 A, $V_{IN1,2}$ = $V_{ON1,2}$ = V_{BIAS} = 3.3 V		–40°C to +85°C		27	40	µA
				–40°C to +125°C			40	
	V_{BIAS} quiescent current (single channel)	I_{OUT1} = I_{OUT2} = 0 A, V_{ON2} = 0 V, $V_{IN1,2}$ = V_{ON1} = V_{BIAS} = 3.3 V		–40°C to +85°C		27	40	µA
				–40°C to +125°C			40	
$I_{SD, VBIAS}$	V_{BIAS} shutdown current	$V_{ON1,2}$ = 0 V, $V_{OUT1,2}$ = 0 V		–40°C to +85°C		0.5	1	µA
				–40°C to +125°C			1	
$I_{SD, VIN1,2}$	$V_{IN1,2}$ shutdown current (per channel)	$V_{ON1,2}$ = 0 V, $V_{OUT1,2}$ = 0 V	$V_{IN1,2}$ = 3.3 V	–40°C to +85°C		0.1	3	µA
				–40°C to +125°C			13	
			$V_{IN1,2}$ = 1.8 V	–40°C to +85°C		0.07	2	
				–40°C to +125°C			6	
			$V_{IN1,2}$ = 1.2 V	–40°C to +85°C		0.05	1	
				–40°C to +125°C			4	
			$V_{IN1,2}$ = 0.8 V	–40°C to +85°C		0.04	1	
				–40°C to +125°C			4	
$I_{ON1,2}$	ON pin input leakage current	V_{ON} = 5.5 V		–40°C to +125°C			0.1	µA
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance	I_{OUT} = –200 mA, V_{BIAS} = 3.3 V	V_{IN} = 3.3 V	25°C		32	38	mΩ
				–40°C to +85°C			44	
				–40°C to +125°C			48	
			V_{IN} = 1.8 V	25°C		28	33	mΩ
				–40°C to +85°C			38	
				–40°C to +125°C			42	
			V_{IN} = 1.2 V	25°C		27	33	mΩ
				–40°C to +85°C			38	
				–40°C to +125°C			41	
			V_{IN} = 0.8 V	25°C		27	32	mΩ
				–40°C to +85°C			37	
				–40°C to +125°C			40	
R_{PD} (1)	Output pulldown resistance	V_{IN} = 3.3 V, V_{ON} = 0 V, I_{OUT} = 5 mA		–40°C to +125°C		270	320	Ω

(1) The TPS22968N-Q1 device does not feature an output pulldown resistance R_{PD}

7.7 Electrical Characteristics (V_{BIAS} = 2.5 V)

V_{BIAS} = 2.5 V. Typical values are for T_A = 25°C, unless otherwise noted

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
$I_{Q, VBIAS}$	V_{BIAS} quiescent current (both channels)	$I_{OUT1} = I_{OUT2} = 0$, $V_{IN1,2} = V_{ON1,2} = V_{BIAS}$ = 2.5 V		–40°C to 85°C		19	27	µA
				–40°C to 125°C			27	
	V_{BIAS} quiescent current (single channel)	$I_{OUT1} = I_{OUT2} = 0$, V_{ON2} = 0 V, $V_{IN1,2} = V_{ON1} = V_{BIAS}$ = 2.5 V		–40°C to 85°C		19	27	µA
				–40°C to 125°C			27	
$I_{SD, VBIAS}$	V_{BIAS} shutdown current	$V_{ON1,2}$ = 0 V, $V_{OUT1,2}$ = 0 V		–40°C to 85°C		0.4	1	µA
				–40°C to 125°C			1	
$I_{SD, VIN1,2}$	$V_{IN1,2}$ shutdown current (per channel)	$V_{ON1,2}$ = 0 V, $V_{OUT1,2}$ = 0 V	$V_{IN1,2}$ = 2.5 V	–40°C to 85°C		0.1	2	µA
				–40°C to 125°C			9	
			$V_{IN1,2}$ = 1.8 V	–40°C to 85°C		0.07	2	
				–40°C to 125°C			6	
			$V_{IN1,2}$ = 1.2 V	–40°C to 85°C		0.05	1	
				–40°C to 125°C			4	
			$V_{IN1,2}$ = 0.8 V	–40°C to 85°C		0.04	1	
				–40°C to 125°C			4	
$I_{ON1,2}$	ON pin input leakage current	V_{ON} = 5.5 V		–40°C to 125°C			0.1	µA
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance	I_{OUT} = –200 mA, V_{BIAS} = 2.5 V	V_{IN} = 2.5 V	25°C		39	45	mΩ
				–40°C to 85°C			52	
				–40°C to 125°C			57	
			V_{IN} = 1.8 V	25°C		34	39	mΩ
				–40°C to 85°C			46	
				–40°C to 125°C			50	
			V_{IN} = 1.2 V	25°C		31	37	mΩ
				–40°C to 85°C			42	
				–40°C to 125°C			46	
			V_{IN} = 0.8 V	25°C		30	35	mΩ
				–40°C to 85°C			41	
				–40°C to 125°C			44	
R_{PD}	Output pulldown resistance	V_{IN} = 2.5 V, V_{ON} = 0 V, I_{OUT} = 5 mA		–40°C to 125°C		270	320	Ω

7.8 Switching Characteristics

T_A = 25 °C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} = V_{ON} = V_{BIAS} = 5 V						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		1150		µs
t_{OFF}	Turn-off time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		4		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		1400		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		2		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		469		
V_{IN} = 0.8 V, V_{ON} = V_{BIAS} = 5 V						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		514		µs
t_{OFF}	Turn-off time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		31		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		271		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		2		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		382		
V_{IN} = 3.3 V, V_{ON} = 5 V, V_{BIAS} = 3.3 V						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		1455		µs
t_{OFF}	Turn-off time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		5		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		1592		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		2		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		681		
V_{IN} = 0.8 V, V_{ON} = 5 V, V_{BIAS} = 3.3 V						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		805		µs
t_{OFF}	Turn-off time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		31		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		455		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		2		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		577		
V_{IN} = 2.5 V, V_{ON} = 5 V, V_{BIAS} = 2.5 V						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		1800		µs
t_{OFF}	Turn-off time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		6		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		1830		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		2		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		909		
V_{IN} = 0.8 V, V_{ON} = 5 V, V_{BIAS} = 2.5 V						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		1140		µs
t_{OFF}	Turn-off time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		28		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		664		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		2		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, CT = 1000 pF		798		

7.9 Typical Characteristics

7.9.1 DC Characteristics

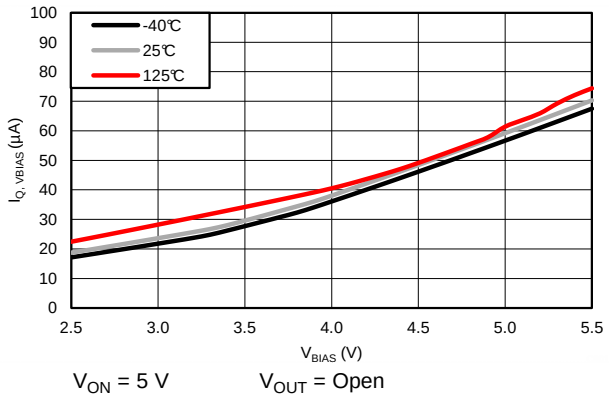


Figure 1. $I_{Q, VBIAS}$ vs V_{BIAS} (Single Channel)

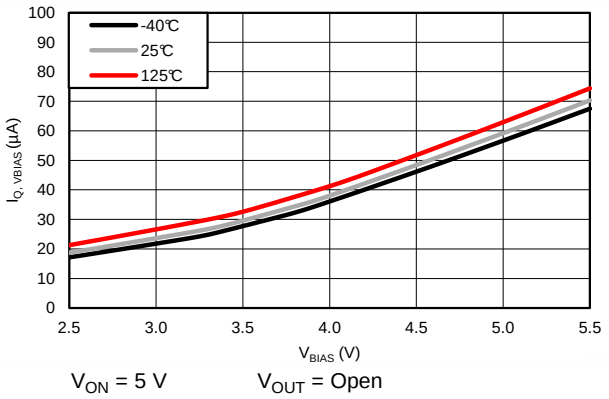


Figure 2. $I_{Q, VBIAS}$ vs V_{BIAS} (Dual Channel)

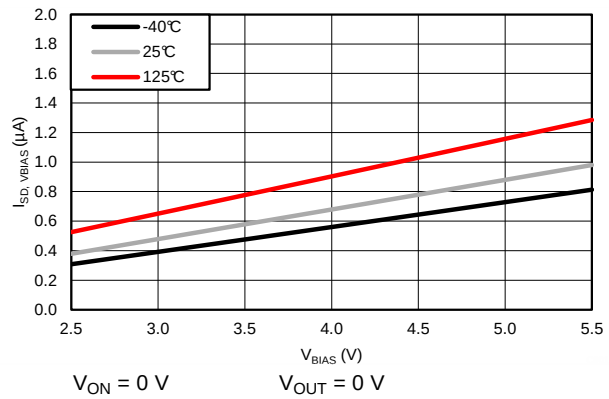


Figure 3. $I_{SD, VBIAS}$ vs V_{BIAS}

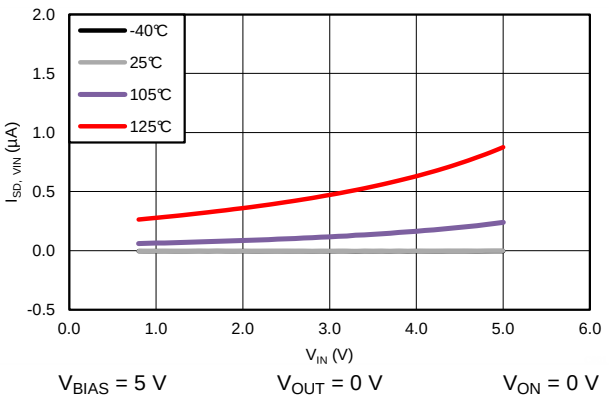


Figure 4. $I_{SD, VIN}$ vs V_{IN} (One Channel)

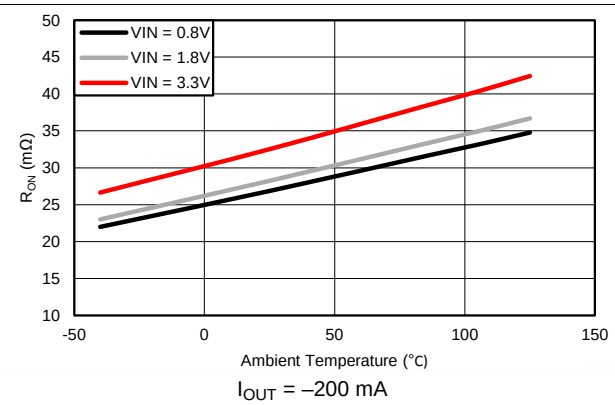


Figure 5. R_{ON} vs Ambient Temperature, V_{BIAS} = 3.3 V

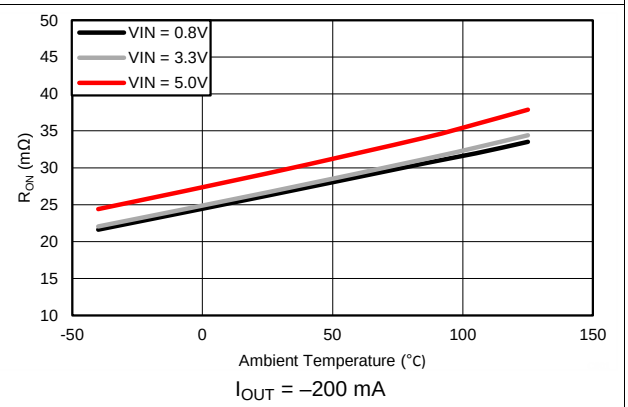


Figure 6. R_{ON} vs Ambient Temperature , V_{BIAS} = 5 V

DC Characteristics (continued)

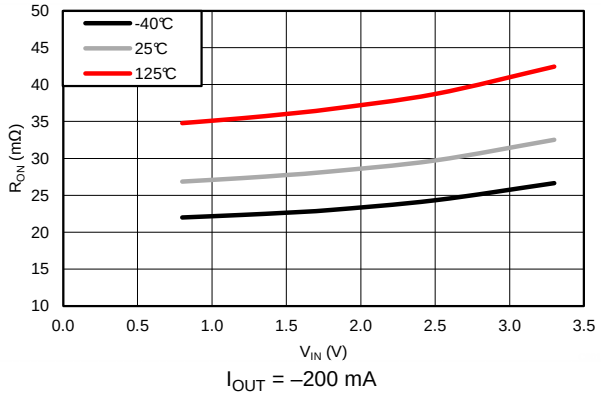


Figure 7. R_{ON} vs V_{IN}, V_{BIAS} = 3.3 V

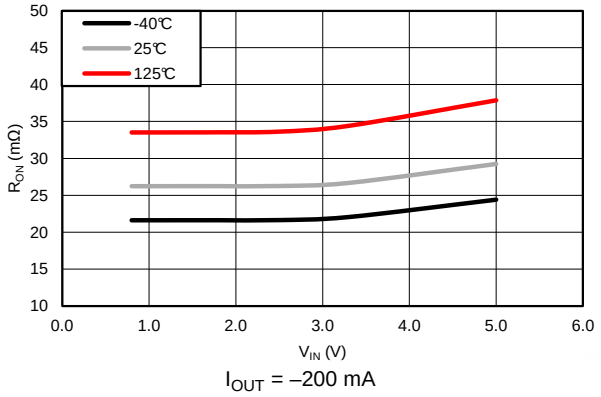


Figure 8. R_{ON} vs V_{IN}, V_{BIAS} = 5 V

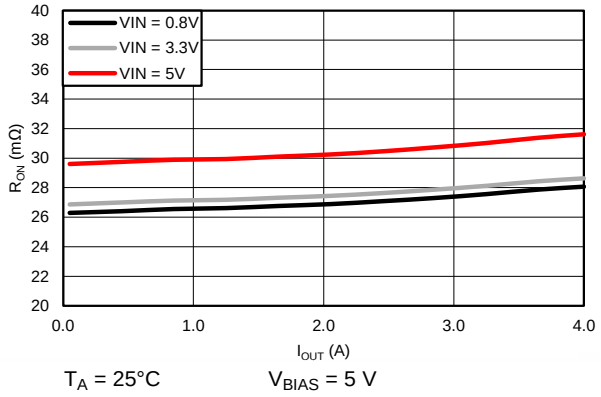


Figure 9. R_{ON} vs I_{OUT}

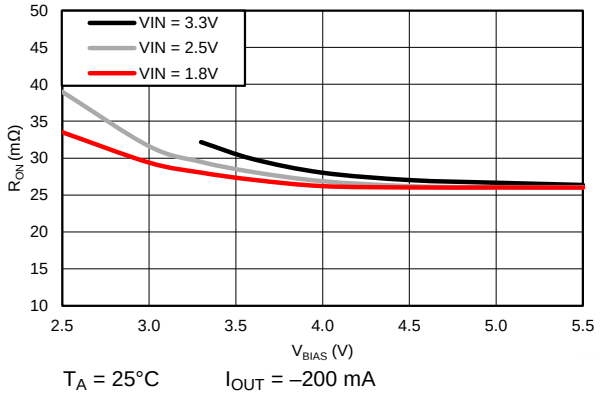


Figure 10. R_{ON} vs V_{BIAS}

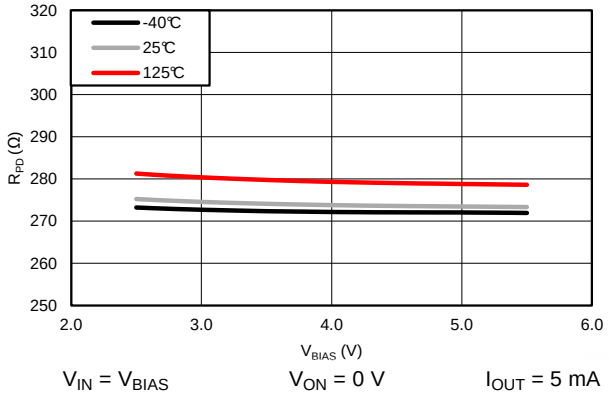


Figure 11. R_{PD} vs V_{BIAS} (TPS22968-Q1 Only)

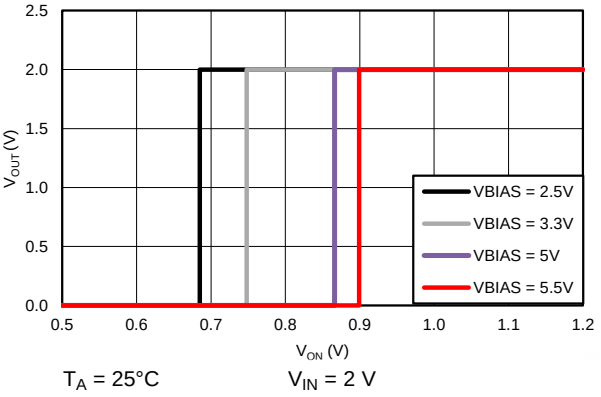


Figure 12. V_{OUT} vs V_{ON}

7.9.2 AC Characteristics

C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω, CT = 1 nF (unless otherwise specified)

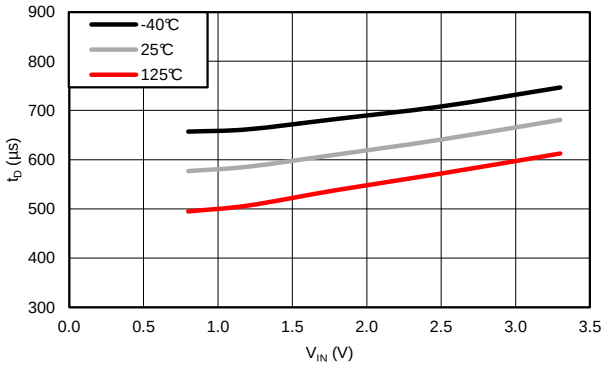


Figure 13. t_D vs V_{IN}, V_{BIAS} = 3.3 V

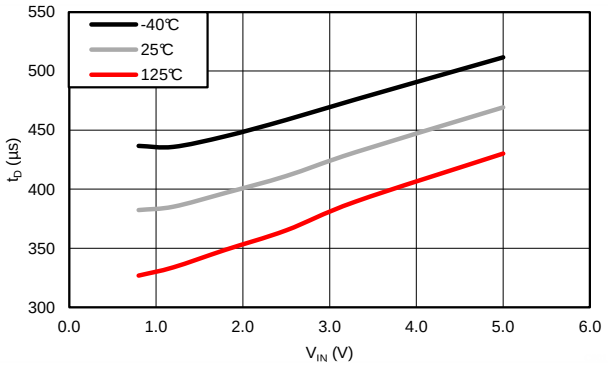


Figure 14. t_D vs V_{IN}, V_{BIAS} = 5 V

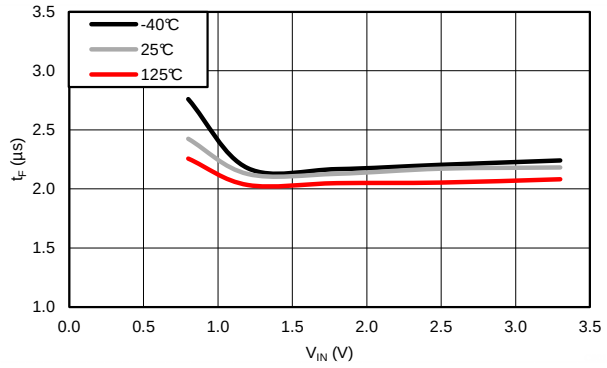


Figure 15. t_F vs V_{IN}, V_{BIAS} = 3.3 V

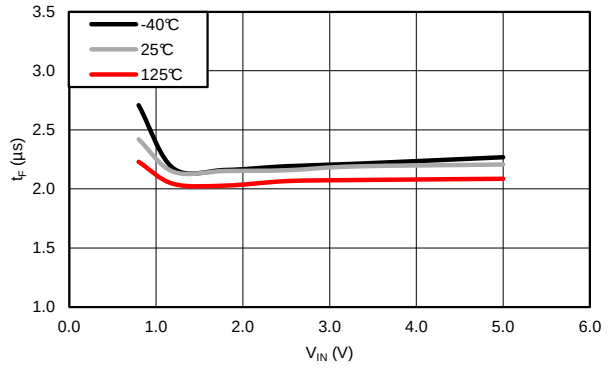


Figure 16. t_F vs V_{IN}, V_{BIAS} = 5 V

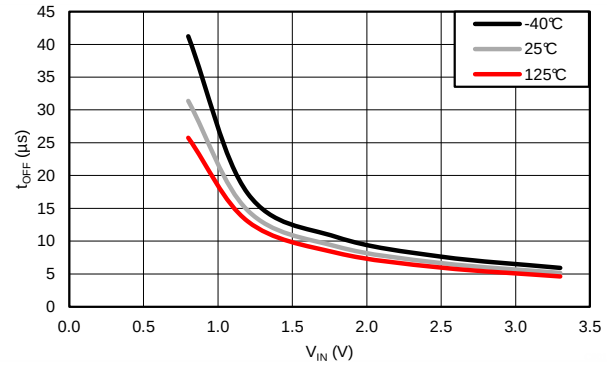


Figure 17. t_{OFF} vs V_{IN}, V_{BIAS} = 3.3 V

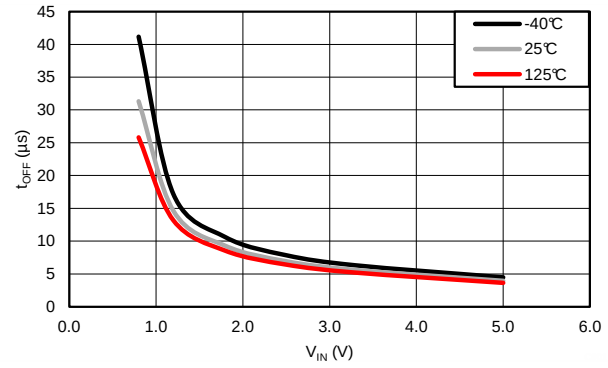


Figure 18. t_{OFF} vs V_{IN}, V_{BIAS} = 5 V

AC Characteristics (continued)

C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω, CT = 1 nF (unless otherwise specified)

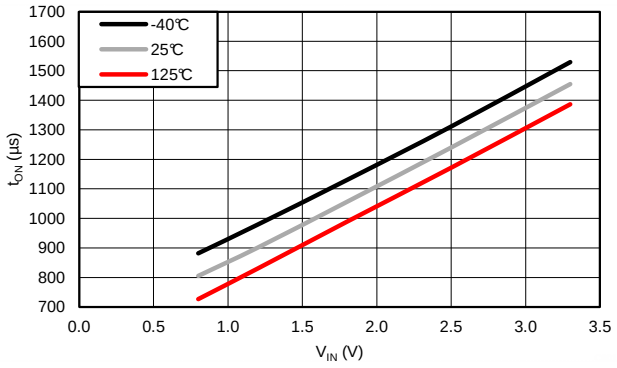


Figure 19. t_{ON} vs V_{IN}, V_{BIAS} = 3.3 V

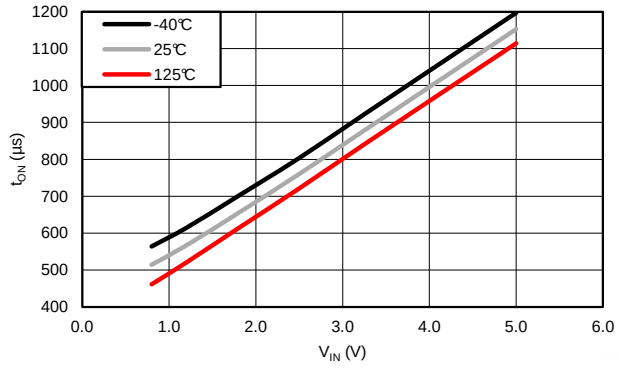


Figure 20. t_{ON} vs V_{IN}, V_{BIAS} = 5 V

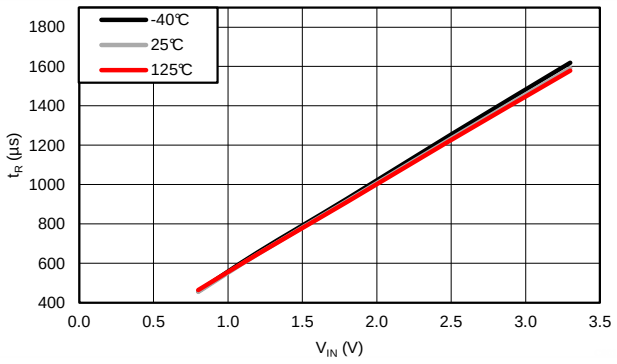


Figure 21. t_R vs V_{IN}, V_{BIAS} = 3.3 V

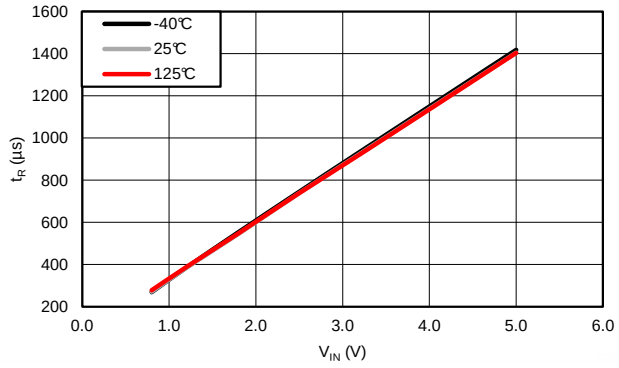


Figure 22. t_R vs V_{IN}, V_{BIAS} = 5 V

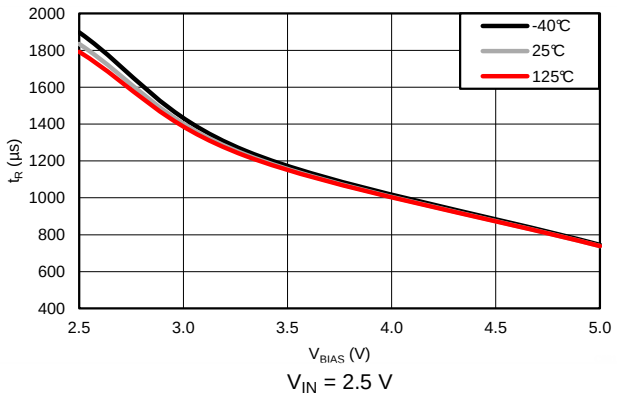


Figure 23. t_R vs V_{BIAS}

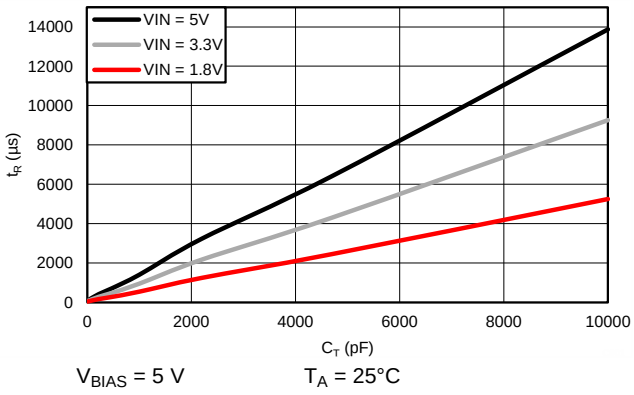


Figure 24. t_R vs CT

AC Characteristics (continued)

C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω, CT = 1 nF (unless otherwise specified)

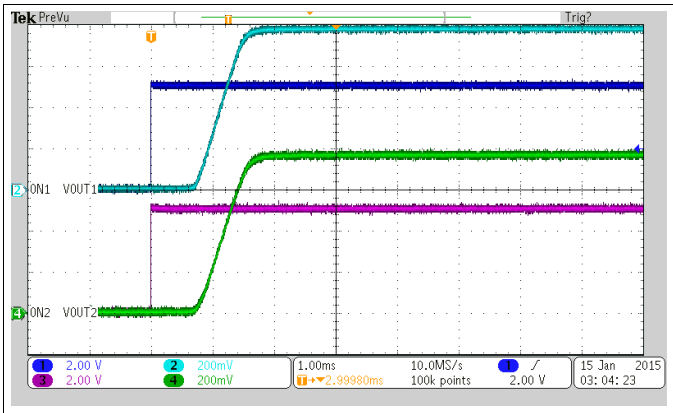


Figure 25. Turn-On Response Time (V_{IN} = 0.8 V, V_{BIAS} = 2.5 V)

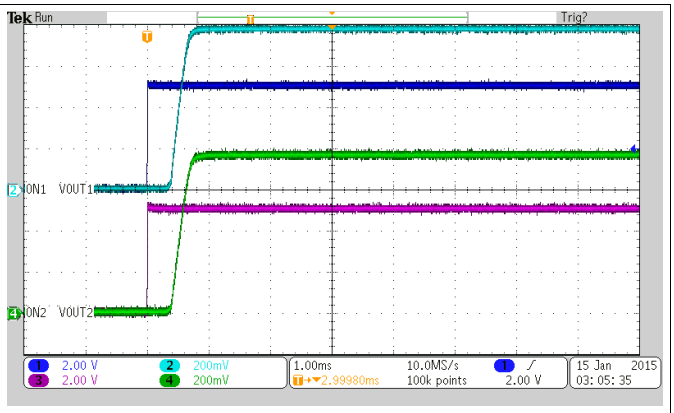


Figure 26. Turn-On Response Time (V_{IN} = 0.8 V, V_{BIAS} = 5 V)

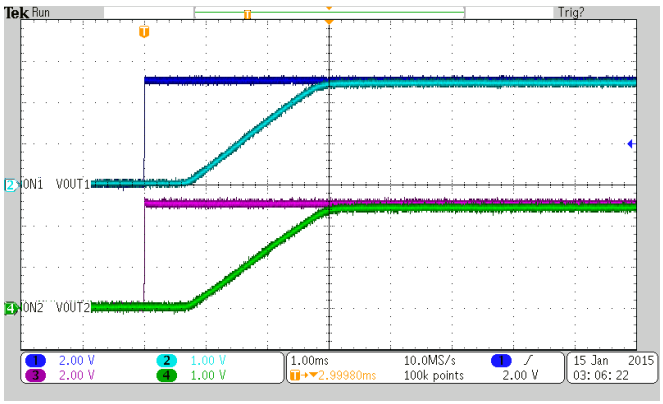


Figure 27. Turn-On Response Time (V_{IN} = 2.5 V, V_{BIAS} = 2.5 V)

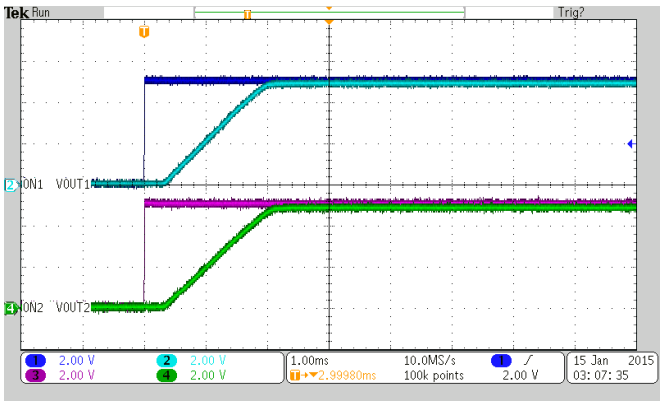


Figure 28. Turn-On Response Time (V_{IN} = 5 V, V_{BIAS} = 5 V)

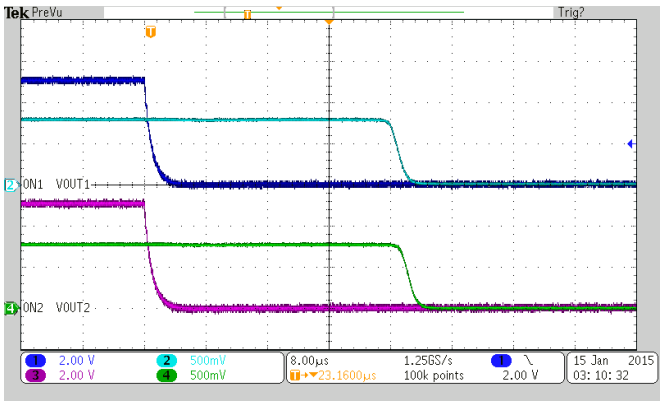


Figure 29. Turn-Off Response Time (V_{IN} = 0.8 V, V_{BIAS} = 2.5 V)

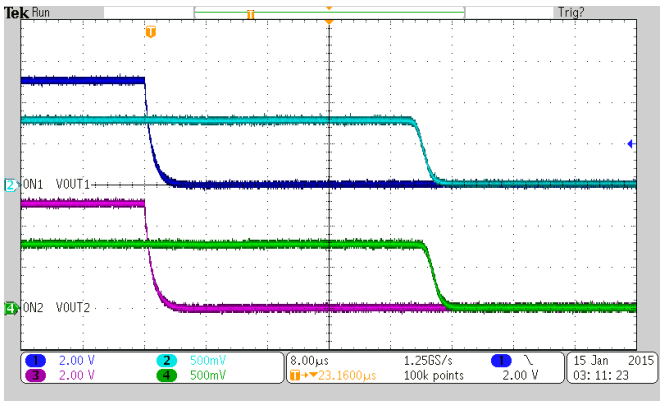


Figure 30. Turn-Off Response Time (V_{IN} = 0.8 V, V_{BIAS} = 5 V)

AC Characteristics (continued)

C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω, CT = 1 nF (unless otherwise specified)

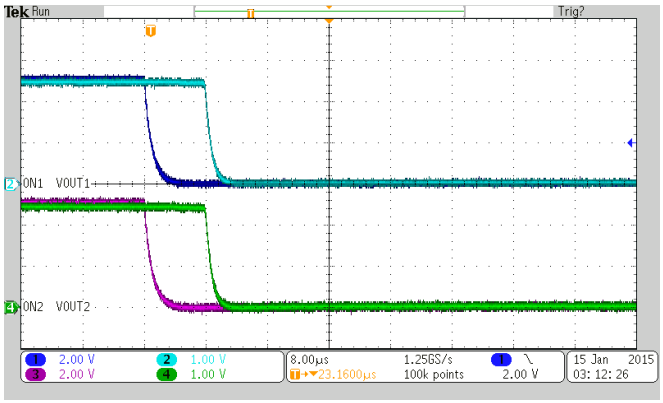


Figure 31. Turn-Off Response Time (V_{IN} = 2.5 V, V_{BIAS} = 2.5 V)

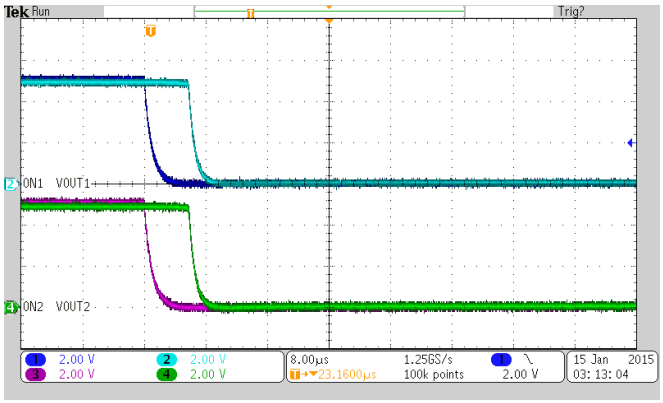


Figure 32. Turn-Off Response Time (V_{IN} = 5 V, V_{BIAS} = 5 V)

8 Parameter Measurement Information

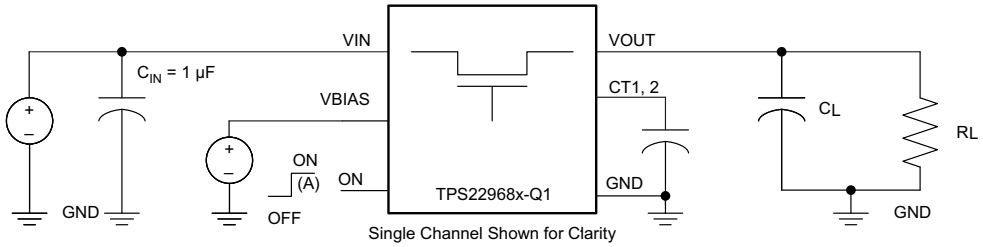
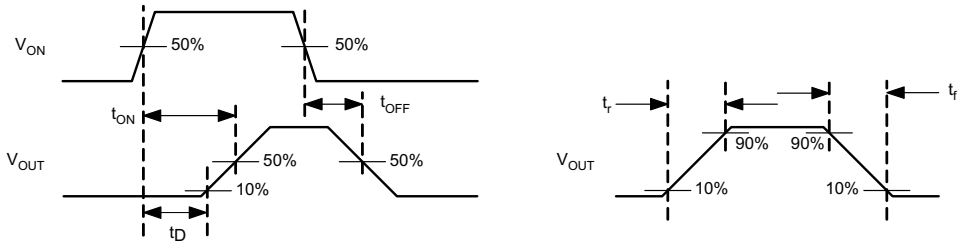


Figure 33. Test Circuit



Rise and fall times of the control signal is 100 ns.

Figure 34. Timing Waveforms

9 Detailed Description

9.1 Overview

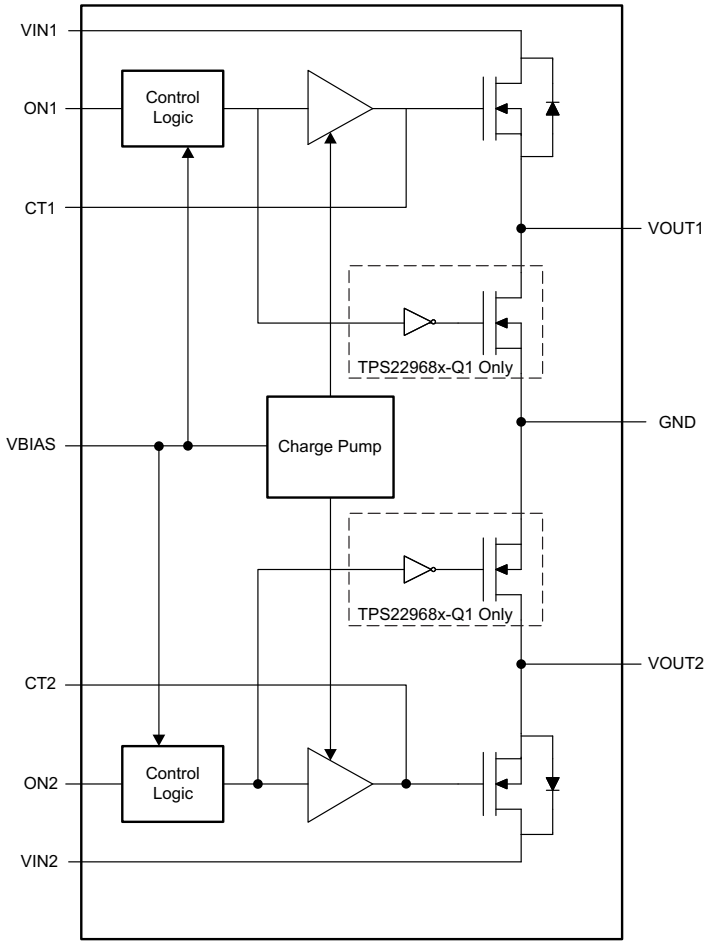
The device is a 5.5 V, 4-A, dual-channel ultra-low R_{ON} load switch with controlled turn on. The device contains two N-channel MOSFETs. Each channel can support a maximum continuous current of 4-A. Each channel is controlled by an on/off GPIO-compatible input. The ON pin must be connected and cannot be left floating. The device is designed to control the turn-on rate and therefore the inrush current. By controlling the inrush current, power supply sag can be reduced during turn-on. The slew rate for each channel is set by connecting a capacitor to GND on the CT pins.

The slew rate is proportional to the capacitor on the CT pin. Refer to *Adjustable Rise Time* to determine the correct CT value for a desired rise time.

The internal circuitry is powered by the VBIAS pin, which supports voltages from 2.5 to 5.5 V. This circuitry includes the charge pump, QOD (TPS22968-Q1 only), and control logic. For these internal blocks to function correctly, a voltage between 2.5 and 5.5 V must be supplied to VBIAS.

When a voltage is supplied to VBIAS and the ON1, 2 pin goes low, the QOD turns on. This connects VOUT1, 2 to GND through an on-chip resistor. The typical pulldown resistance (R_{PD}) is 270 Ω. Note that QOD is not applicable to TPS22968N-Q1.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 ON and OFF Control

The ON pins control the state of the switch. Asserting ON high enables the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2 V or higher GPIO voltage. This pin cannot be left floating and must be tied either high or low for proper functionality.

9.3.2 Quick Output Discharge (QOD) (TPS22968-Q1 Only)

The TPS22968-Q1 includes a QOD feature. When the switch is disabled, a discharge resistor is connected between VOUT and GND. This resistor has a typical value of 270 Ω and prevents the output from floating while the switch is disabled.

9.3.3 Adjustable Rise Time

A capacitor to GND on the CT pins sets the slew rate for each channel. The capacitor to GND on the CT pins should be rated for 25 V and above. An approximate formula for the relationship between CT and slew rate with V_{BIAS} = 5 V is shown in Equation 1:

$$SR = 0.35 \times CT + 25 \quad (1)$$

where

- SR = slew rate (in µs/V)
- CT = the capacitance value on the CT pin (in pF)
- The units for the constant 25 is in µs/V.

Rise time can be calculated by multiplying the input voltage by the slew rate. Table 1 contains rise time values measured on a typical device.

Table 1. Rise Time Table

CTx (pF)	Rise Time (µs) (1) (2)					
	V_{IN} = 5 V	V_{IN} = 3.3 V	V_{IN} = 2.5 V	V_{IN} = 1.8 V	V_{IN} = 1.2 V	V_{IN} = 0.8 V
0	84	63	52	43	35	27
220	418	285	223	168	122	88
470	711	479	372	276	196	139
1000	1405	952	738	545	385	271
2200	3236	2174	1684	1246	876	615
4700	6415	4306	3317	2454	1725	1217
10000	13872	9261	7150	5253	3694	2591

(1) 10% - 90%, C_L = 0.1 µF, C_{IN} = 1 µF, R_L = 10 Ω, V_{BIAS} = 5 V
(2) Typical values at 25°C with a 25-V X7R 10% ceramic capacitor on CT

9.4 Device Functional Modes

Table 2 lists the device function table

Table 2. Functional Table

ONx	VINx to VOUTx	VOUTx to GND
L	Off	On
H	On	Off

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

This section highlights some of the design considerations for implementing this device in various applications. A PSPICE model for this device is also available on the product page on www.ti.com for further aid. (See the *Device Support* section for more information)

10.1.1 Input Capacitor (Optional)

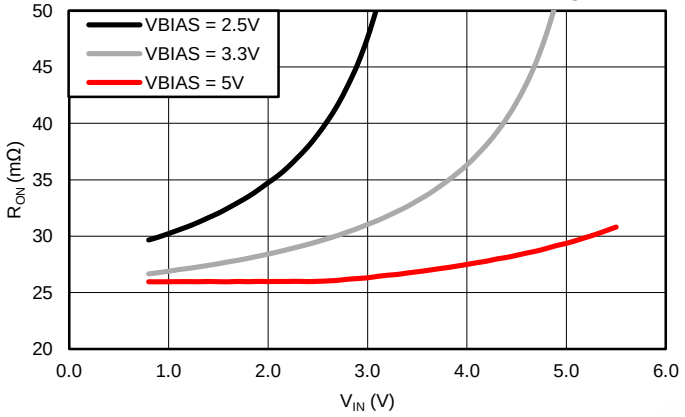
To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor, a capacitor must be placed between VIN and GND. A 1-µF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high-current applications. When switching heavy loads, TI recommends to have an input capacitor about 10× higher than the output capacitor to avoid excessive voltage drop.

10.1.2 Output Capacitor (Optional)

Due to the integrated body diode in the NMOS switch, TI highly recommends a C_{IN} greater than C_L. A C_L greater than C_{IN} can cause the voltage on VOUT to exceed VIN when the system supply is removed. This could result in current flow through the body diode from VOUT to VIN. TI recommends a C_{IN} to C_L ratio of 10 to 1 for minimizing V_{IN} dip caused by inrush currents during startup.

10.1.3 V_{IN} and V_{BIAS} Voltage Range

For optimal R_{ON} performance, make sure $V_{IN} \leq V_{BIAS}$. The device is still functional if $V_{IN} > V_{BIAS}$, but it will exhibit R_{ON} greater than what is listed in the *Electrical Characteristics (V_{BIAS} = 5 V)* and *Electrical Characteristics (V_{BIAS} = 2.5 V)* . See Figure 35 for an example of a typical device. Notice the increasing R_{ON} as V_{IN} exceeds V_{BIAS} voltage. Be sure to never exceed the maximum voltage rating for V_{IN} and V_{BIAS}.



T_A = 25°C I_{OUT} = –200 mA

Figure 35. R_{ON} vs V_{IN}

Application Information (continued)

10.1.3.1 Parallel Configuration

To increase the current capabilities and lower the R_{ON} by approximately 50%, both channels can be placed in parallel as shown in Figure 36 (parallel configuration). With this configuration, the CT1 and CT2 pins can be tied together to use one capacitor, CT, as shown in Figure 36. With a single CT capacitor, the rise time will be half of the typical rise-time value. Refer to the Table 1 for typical timing values.

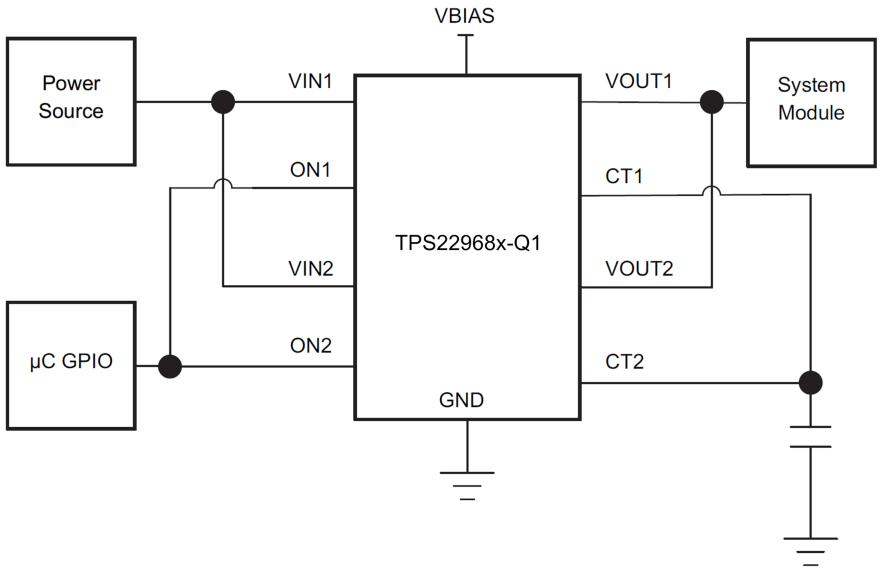


Figure 36. Parallel Configuration Schematic

10.1.3.2 Standby Power Reduction

TPS22968x-Q1 can help to reduce the standby power consumption of a module. Some loads will consume a non-trivial amount of power when turned off. If the power to the load is removed by the load switch, the standby power consumption can be significantly reduced. Figure 37 below shows the Standby Power Reduction Schematic.

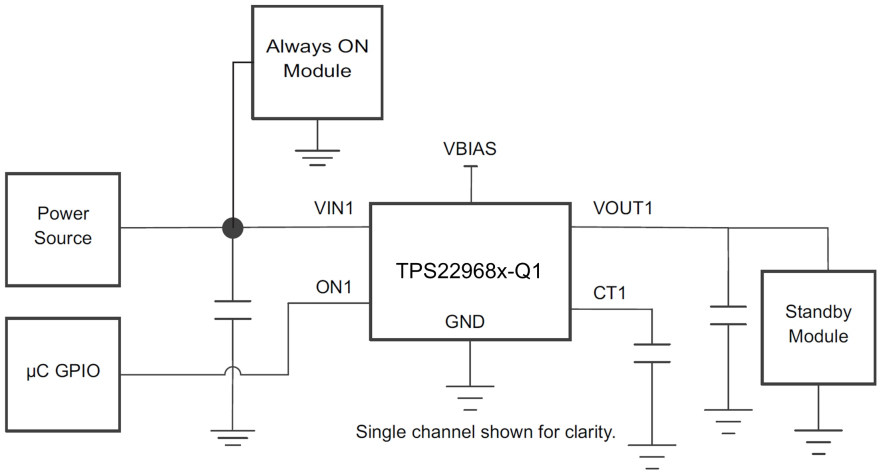
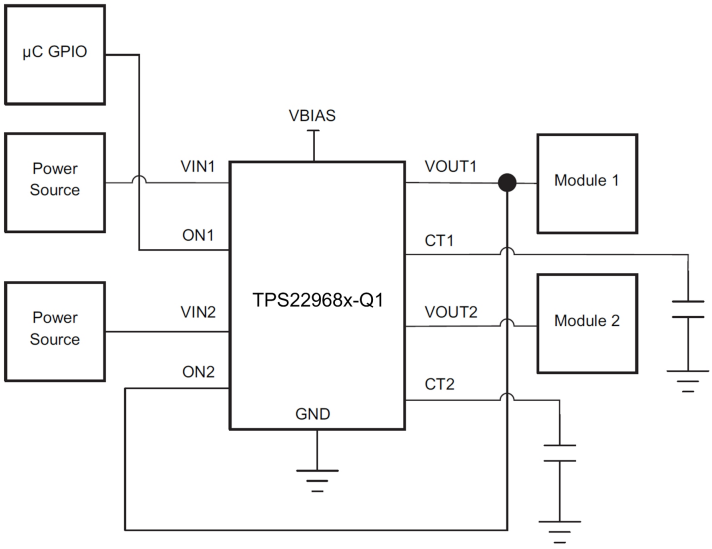


Figure 37. Standby Power Reduction Schematic

Application Information (continued)

10.1.3.3 Power Supply Sequencing Without a GPIO Input

In many end equipments, there is a need to power up various modules in a predetermined manner. TPS22968x-Q1 can solve the problem of power sequencing without adding any complexity to the overall system. See Figure 38.



VIN1 must be greater V_{IH}.

Figure 38. Power Sequencing Without a GPIO Input Schematic

10.1.3.4 Reverse Current Blocking

In certain applications, it may be desirable to have reverse current blocking. Reverse current blocking prevents current from flowing from the output to the input of the load switch when the device is disabled. With the following configuration, the TPS22968x-Q1 can be converted into a single-channel switch with reverse current blocking. In this configuration, VIN1 or VIN2 can be used as the input and VIN2 or VIN1 is the output. See Figure 39.

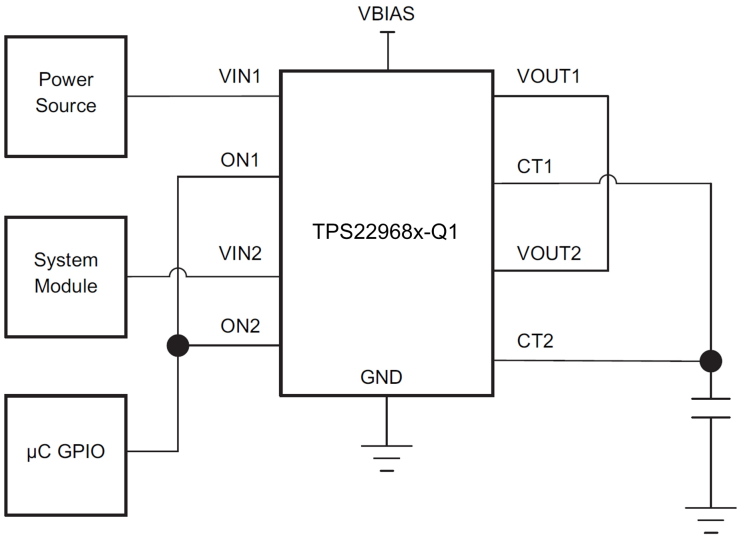


Figure 39. Reverse Current Blocking Schematic

10.2 Typical Application

This application demonstrates how the TPS22968x-Q1 can be used to power a downstream load with a large capacitance. The example in Figure 40 is powering a 22-µF capacitive output load.

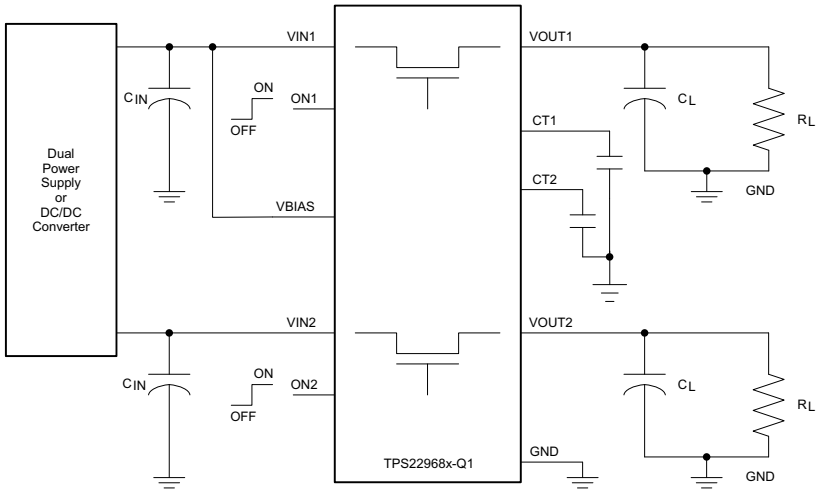


Figure 40. Typical Application Schematic for Powering a Downstream Module

10.2.1 Design Requirements

For this design example, use the values listed in Table 3 as the input parameters.

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	3.3 V
V_{BIAS}	5 V
Output capacitance (C_L)	22 µF
Allowable inrush current on VOUT	0.4 A

10.2.2 Detailed Design Procedure

To begin the design process, the designer must know the following:

- V_{IN} voltage
- V_{BIAS} voltage
- Output capacitance (C_L)
- Allowable inrush current on VOUT due to C_L capacitor

10.2.2.1 Inrush Current

To determine how much inrush current will be caused by the C_L capacitor, use Equation 2.

$$I_{INRUSH} = C_L \times \frac{dV_{OUT}}{dt}$$

where

- I_{INRUSH} = amount of inrush current caused by C_L
- C_L = capacitance on VOUT
- dt = V_{OUT} rise time
- dV_{OUT} = increase in V_{OUT} during the rise time (2)

Inrush current is proportional to rise time. The rise time is adjustable by use of the CT capacitor. The appropriate rise time can be calculated using the design requirements and the inrush current equation (Equation 2).

400 mA = 22 µF × 3.3 V / dt (3)

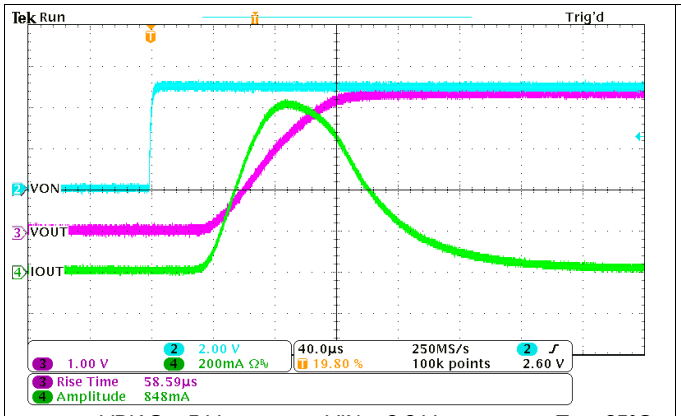
dt = 182 µs (4)

To ensure an inrush current of less than 400 mA, choose a CT capacitor value that will yield a rise time of more than 182 µs. See the oscilloscope captures in the *Application Curves* for an example of how the CT capacitor can be used to reduce inrush current. See Table 1 for correlation between rise times and CT values.

An appropriate C_L value should be placed on VOUT such that the I_{MAX} and I_{PLS} specifications of the device are not violated.

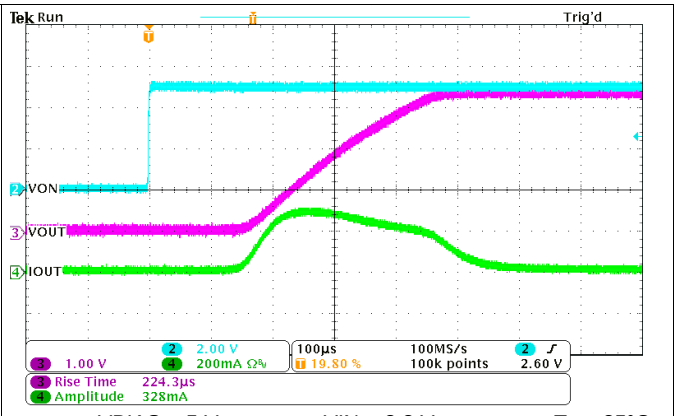
10.2.3 Application Curves

The two scope captures in Figure 41 and Figure 42 show how the CT capacitor can be used to reduce inrush current.



VBIAS = 5 V VIN = 3.3 V T_A = 25°C
CT = Open C_L = 22 µF

Figure 41. Inrush Current Without CT Capacitor



VBIAS = 5 V VIN = 3.3 V T_A = 25°C
CT = 220 pF C_L = 22 µF

Figure 42. Inrush Current With CT = 220 pF

11 Power Supply Recommendations

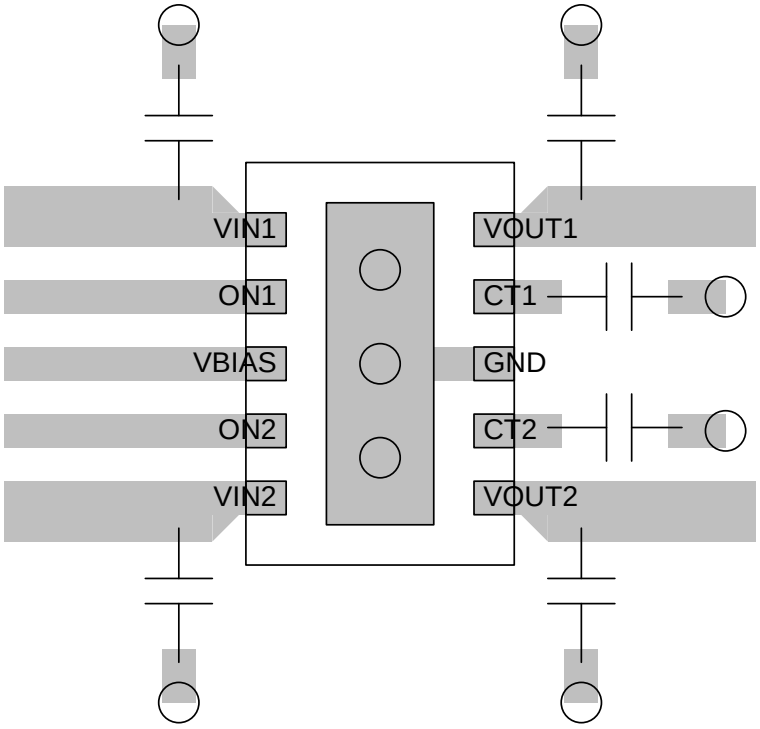
The device is designed to operate from a V_{BIAS} range of 2.5 V to 5.5 V and V_{IN} range of 0.8 V to 5.5 V. This supply must be well regulated and placed as close to the device pin as possible with the recommended 1-µF bypass capacitor. If the supply is located more than a few inches from the device pins, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 10 µF may be sufficient.

12 Layout

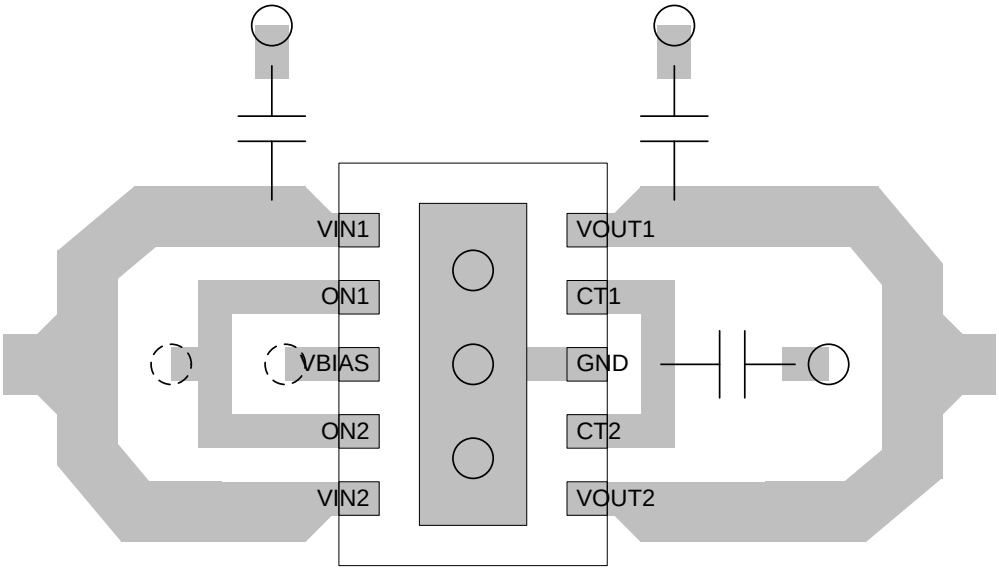
12.1 Layout Guidelines

- VIN and VOUT traces should be as short and wide as possible to accommodate for high current.
- Use vias under the exposed thermal pad for thermal relief for high current operation.
- VINx pins should be bypassed to ground with low-ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 1-µF ceramic with X5R or X7R dielectric. This capacitor should be placed as close to the device pins as possible.
- VOUTx pins should be bypassed to ground with low-ESR ceramic bypass capacitors. The typical recommended bypass capacitance is one-tenth of the VINx bypass capacitor of X5R or X7R dielectric rating. This capacitor should be placed as close to the device pins as possible.
- The VBIAS pin should be bypassed to ground with low-ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 0.1-µF ceramic with X5R or X7R dielectric.
- The CTx capacitors should be placed as close to the device pins as possible. The typical recommended CTx capacitance is a capacitor of X5R or X7R dielectric rating with a rating of 25 V or higher.

12.2 Layout Example



Dual-channel layout



Single-channel layout

Via to GND

Via to internal or bottom layer

Figure 43. Layout Schematic

12.3 Thermal Considerations

The maximum IC junction temperature should be restricted to 150°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given ambient temperature, use Equation 5.

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} \quad (5)$$

where

- $P_{D(max)}$ = maximum allowable power dissipation
- $T_{J(max)}$ = maximum allowable junction temperature (150°C for the TPS22968x-Q1)
- T_A = ambient temperature of the device
- $R_{\theta JA}$ = junction to air thermal impedance. See *Thermal Information*. This parameter is highly dependent upon board layout.

Following are two examples demonstrating how to use the above information: For V_{BIAS} = 5 V, V_{IN} = 5 V, the maximum allowable ambient temperature with a 3-A load through each channel can be determined by using the following calculations.

NOTE

When calculating power dissipation in the switch, it is important to use the correct R_{ON} value. R_{ON} is dependent on the junction temperature of the device.

$$P_D = I^2 \times R \times 2 \text{ (multiplied by 2 because there are two channels)} \quad (6)$$

$$2 \times I^2 \times R = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} \quad (7)$$

$$T_A = T_{J(MAX)} - R_{\theta JA} \times 2 \times I^2 \times R \quad (8)$$

$$T_A = 150°C - 55.6°C/W \times 2 \times (3\ A)^2 \times 45\ m\Omega = 105°C \quad (9)$$

For V_{BIAS} = 5 V, V_{IN} = 5 V, the maximum continuous current for an ambient temperature of 85°C with the same current flowing through each channel can be determined by using the following calculation:

$$2 \times I^2 \times R = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} \quad (10)$$

$$I = \sqrt{\frac{T_{J(MAX)} - T_A}{2 \times R \times R_{\theta JA}}} \quad (11)$$

$$I = \sqrt{\frac{150°C - 85°C}{2 \times 45\ m\Omega \times 55.6°C/W}} = 3.6\ A \quad (12)$$

13 Device and Documentation Support

13.1 Device Support

13.1.1 Developmental Support

For the TPS22968N and TPS22968N-Q1 PSpice Transient Model, see SLVMBA9.

For the TPS22968 and TPS22968-Q1 PSpice Transient Model, see SLVMA29.

13.2 Documentation Support

13.2.1 Related Documentation

For related documentation see the following:

- *Basics of Load Switches*, SLVA652
- *Managing Inrush Current*, SLVA670A
- *TPS22968EVM-007 Dual 4A Load Switch*, SLVUA30
- *Load Switch Thermal Considerations*, SLVUA74
- *TPS22968Q1EVM Dual 4 A Load Switch*, SLVUAE2A

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

E2E is a trademark of Texas Instruments.
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13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22968NQDMGRQ1	ACTIVE	WSON	DMG	10	3000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	11C	Samples
TPS22968NQDMGTQ1	ACTIVE	WSON	DMG	10	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	11C	Samples
TPS22968QDMGRQ1	ACTIVE	WSON	DMG	10	3000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	SIV	Samples
TPS22968QDMGTQ1	ACTIVE	WSON	DMG	10	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	SIV	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS22968-Q1 :

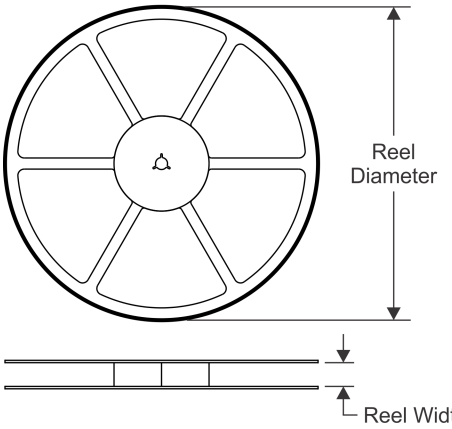
- Catalog: TPS22968

NOTE: Qualified Version Definitions:

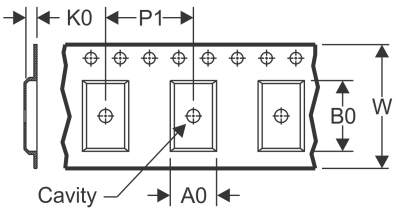
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

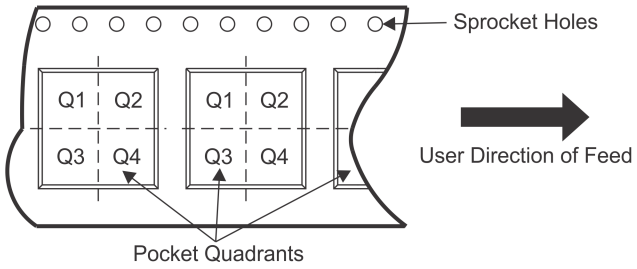


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

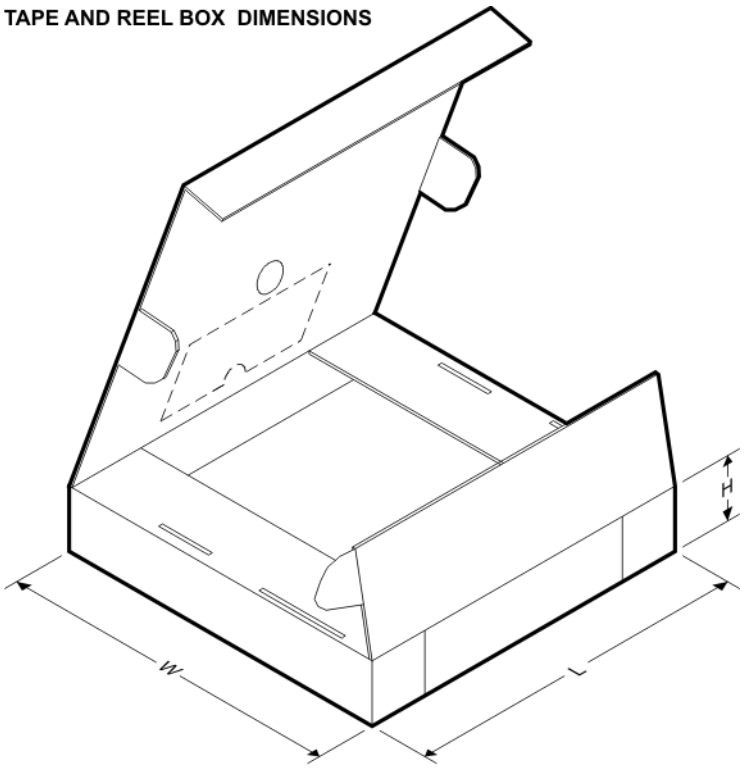
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22968NQDMGRQ1	WSON	DMG	10	3000	179.0	8.4	2.3	3.2	1.0	4.0	8.0	Q1
TPS22968NQDMGTQ1	WSON	DMG	10	250	179.0	8.4	2.3	3.2	1.0	4.0	8.0	Q1
TPS22968QDMGRQ1	WSON	DMG	10	3000	179.0	8.4	2.3	3.2	1.0	4.0	8.0	Q1
TPS22968QDMGTQ1	WSON	DMG	10	250	179.0	8.4	2.3	3.2	1.0	4.0	8.0	Q1

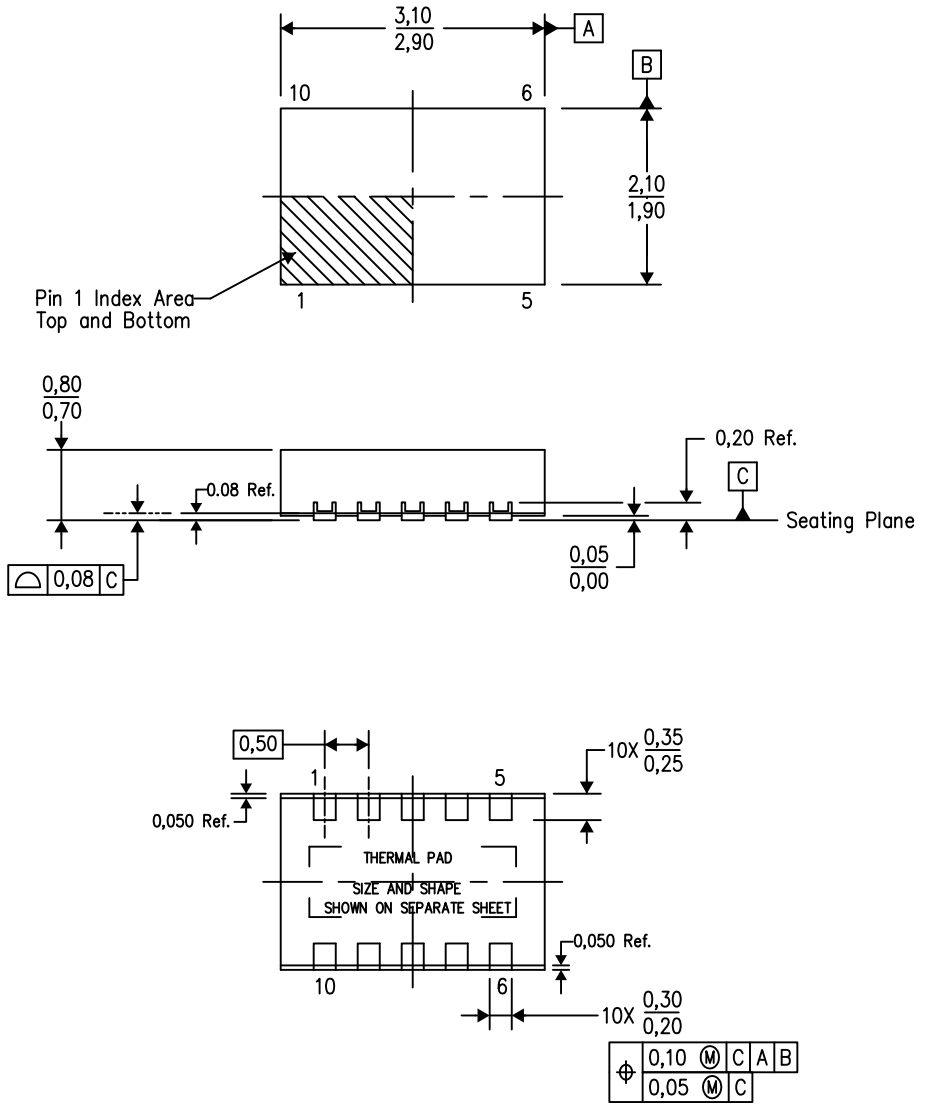
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22968NQDMGRQ1	WSON	DMG	10	3000	195.0	200.0	45.0
TPS22968NQDMGTQ1	WSON	DMG	10	250	195.0	200.0	45.0
TPS22968QDMGRQ1	WSON	DMG	10	3000	195.0	200.0	45.0
TPS22968QDMGTQ1	WSON	DMG	10	250	195.0	200.0	45.0

DMG (R–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



4221635/B 07/14

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Side Lead Plating Process–1, matte tin only.

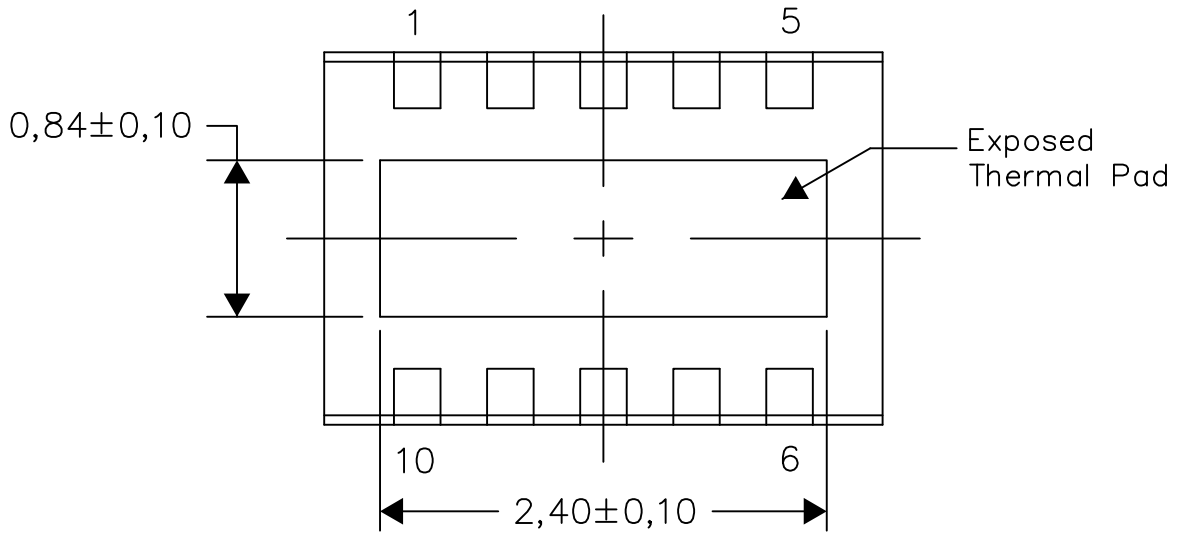
DMG (R–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4221653/A 07/14

NOTES: All linear dimensions are in millimeters

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