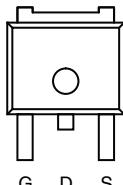


# Automotive N-Channel 150 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY	
$V_{DS}$ (V)	150
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = 10$ V	0.052
$I_D$ (A)	25
Configuration	Single

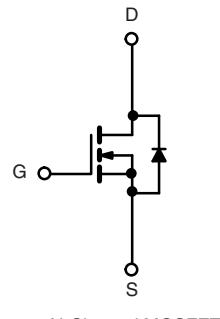


**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

**TO-252**


Drain Connected to Tab

Top View



N-Channel MOSFET

## FEATURES

- TrenchFET® Power MOSFET
- Package with Low Thermal Resistance
- 100 %  $R_g$  and UIS Tested
- AEC-Q101 Qualified
- Material categorization:  
For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

## ORDERING INFORMATION

Package	TO-252
Lead (Pb)-free and Halogen-free	SQD25N15-52-GE3

## ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	150	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current	$I_D$	25	A
		16	
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	50	A
Pulsed Drain Current <sup>b</sup>	$I_{DM}$	63	
Single Pulse Avalanche Current	$I_{AS}$	30	mJ
Single Pulse Avalanche Energy	$E_{AS}$	45	
Maximum Power Dissipation <sup>b</sup>	$P_D$	107	W
		35	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 175	°C

## THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient	$R_{thJA}$	50	°C/W
Junction-to-Case (Drain)	$R_{thJC}$	1.4	

### Notes

- Package limited.
- Pulse test; pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2$  %.
- When mounted on 1" square PCB (FR-4 material).

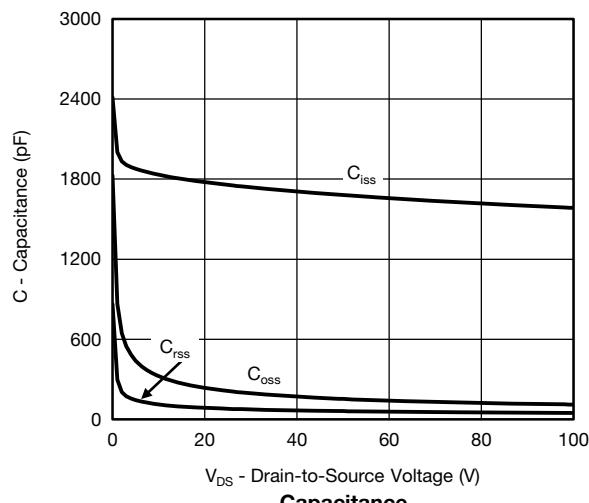
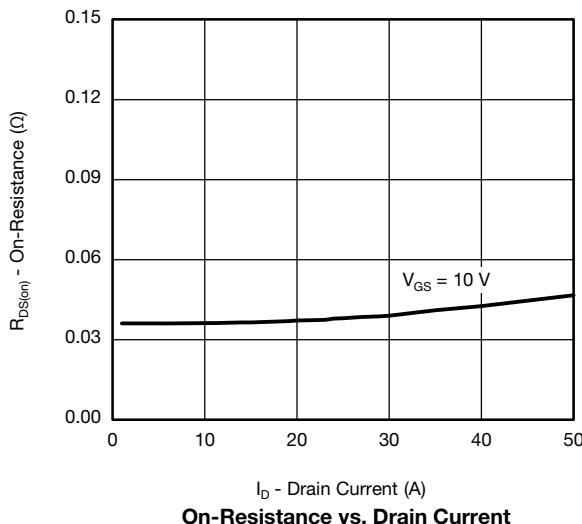
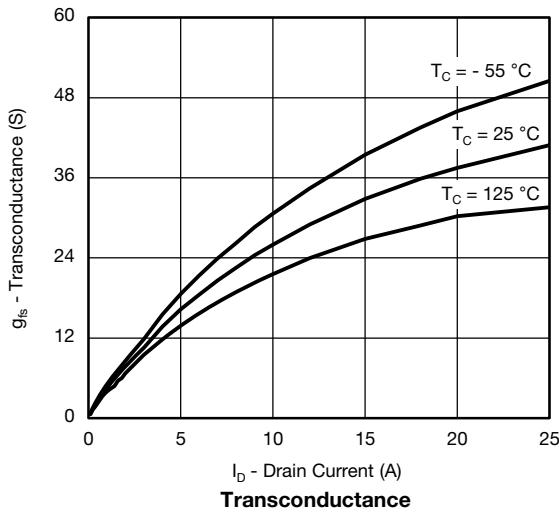
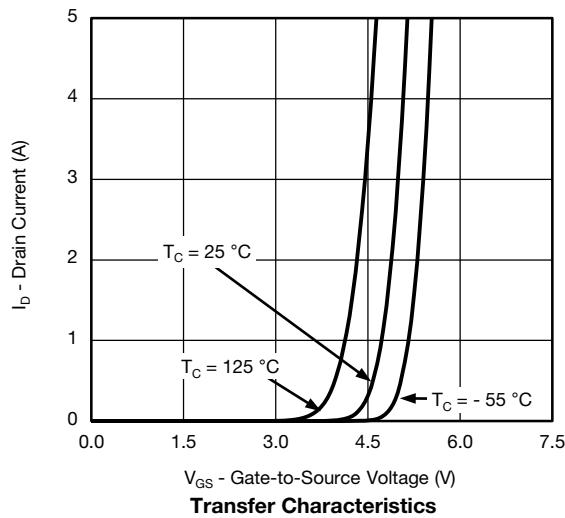
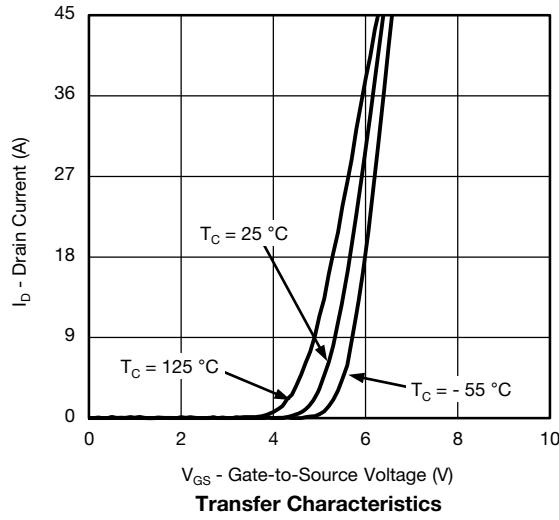
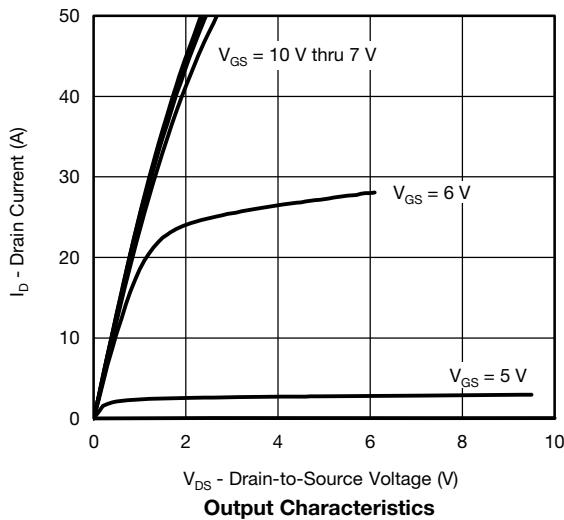
**SPECIFICATIONS** ( $T_C = 25^\circ\text{C}$ , unless otherwise noted)

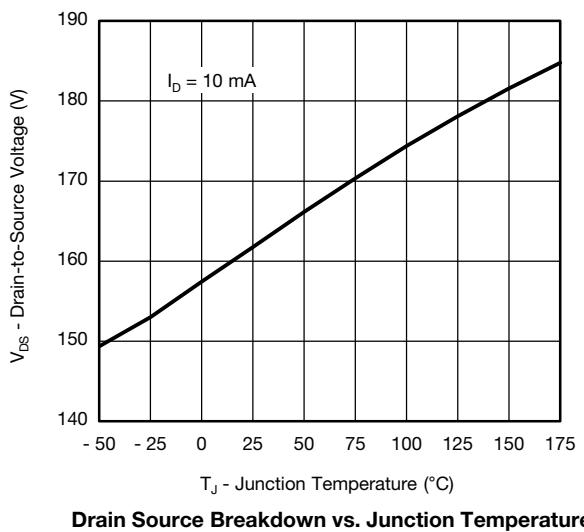
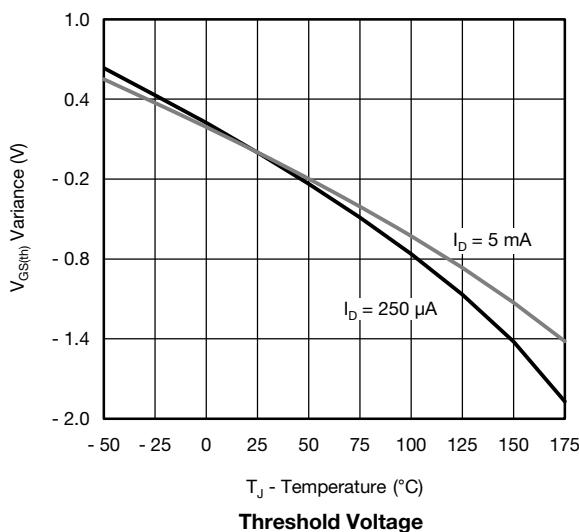
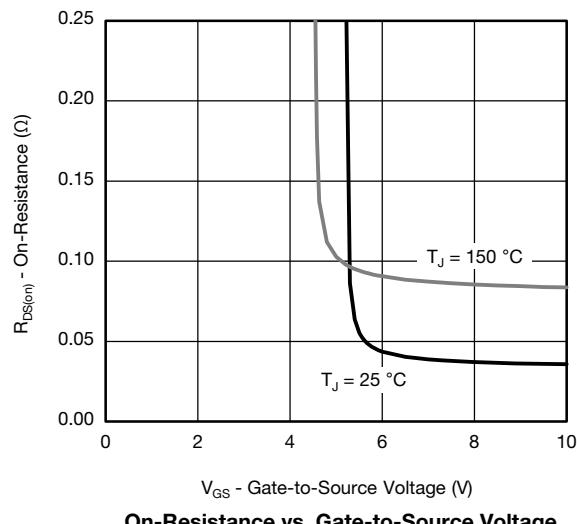
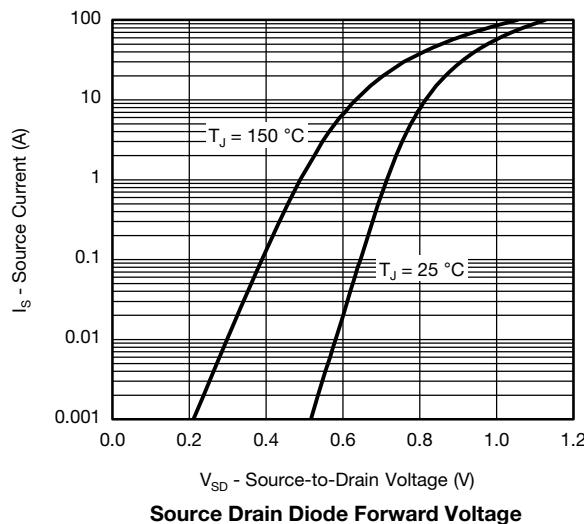
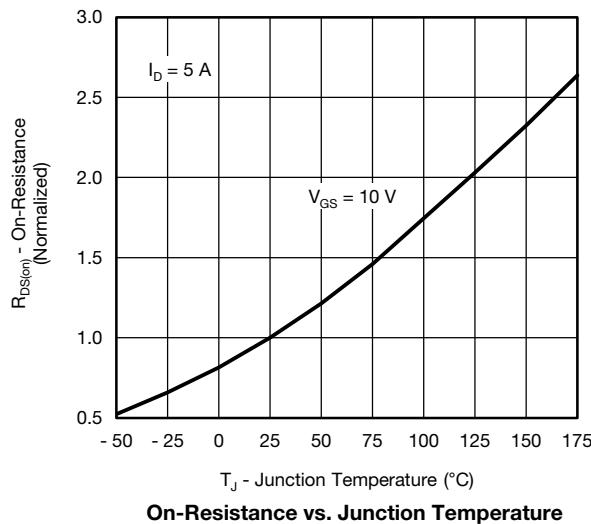
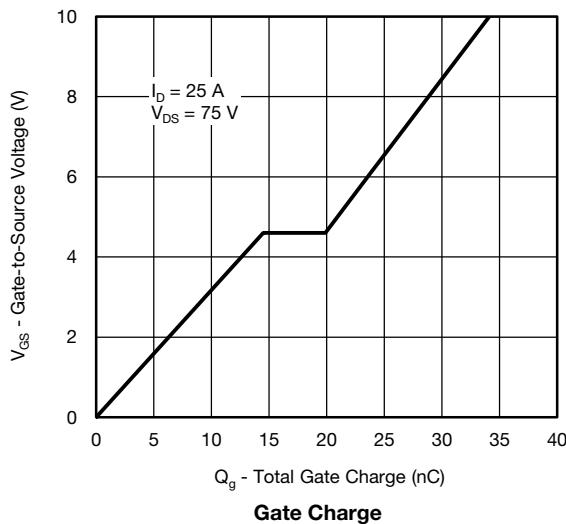
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
<b>Static</b>								
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$	$I_D = 250\text{ }\mu\text{A}$	150	-	-	V	
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$	$I_D = 250\text{ }\mu\text{A}$	2.5	3	4		
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}$	$V_{GS} = \pm 20\text{ V}$	-	-	$\pm 100$	nA	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 150\text{ V}$	-	-	1	$\mu\text{A}$	
		$V_{GS} = 0\text{ V}$	$V_{DS} = 150\text{ V}$ , $T_J = 125^\circ\text{C}$	-	-	50		
		$V_{GS} = 0\text{ V}$	$V_{DS} = 150\text{ V}$ , $T_J = 175^\circ\text{C}$	-	-	250		
On-State Drain Current <sup>a</sup>	$I_{D(\text{on})}$	$V_{GS} = 10\text{ V}$	$V_{DS} \geq 5\text{ V}$	30	-	-	A	
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(\text{on})}$	$V_{GS} = 10\text{ V}$	$I_D = 15\text{ A}$	-	0.038	0.052	$\Omega$	
		$V_{GS} = 10\text{ V}$	$I_D = 15\text{ A}$ , $T_J = 125^\circ\text{C}$	-	-	0.104		
		$V_{GS} = 10\text{ V}$	$I_D = 15\text{ A}$ , $T_J = 175^\circ\text{C}$	-	-	0.136		
Forward Transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}$ , $I_D = 15\text{ A}$		-	33	-	S	
<b>Dynamic<sup>b</sup></b>								
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$	-	1760	2200	pF	
Output Capacitance	$C_{oss}$			-	215	270		
Reverse Transfer Capacitance	$C_{rss}$			-	80	100		
Total Gate Charge <sup>c</sup>	$Q_g$	$V_{GS} = 10\text{ V}$	$V_{DS} = 75\text{ V}$ , $I_D = 25\text{ A}$	-	34	51	nC	
Gate-Source Charge <sup>c</sup>	$Q_{gs}$			-	14.5	-		
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			-	5.4	-		
Gate Resistance	$R_g$	$f = 1\text{ MHz}$		1	1.8	2.6	$\Omega$	
Turn-On Delay Time <sup>c</sup>	$t_{d(\text{on})}$	$V_{DD} = 75\text{ V}$ , $R_L = 3\Omega$ $I_D \geq 25\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\Omega$		-	11	17	ns	
Rise Time <sup>c</sup>	$t_r$			-	11	17		
Turn-Off Delay Time <sup>c</sup>	$t_{d(\text{off})}$			-	20	30		
Fall Time <sup>c</sup>	$t_f$			-	6	9		
<b>Source-Drain Diode Ratings and Characteristics<sup>b</sup></b>								
Pulsed Current <sup>a</sup>	$I_{SM}$			-	-	63	A	
Forward Voltage	$V_{SD}$	$I_F = 20\text{ A}$ , $V_{GS} = 0\text{ V}$		-	0.87	1.5	V	

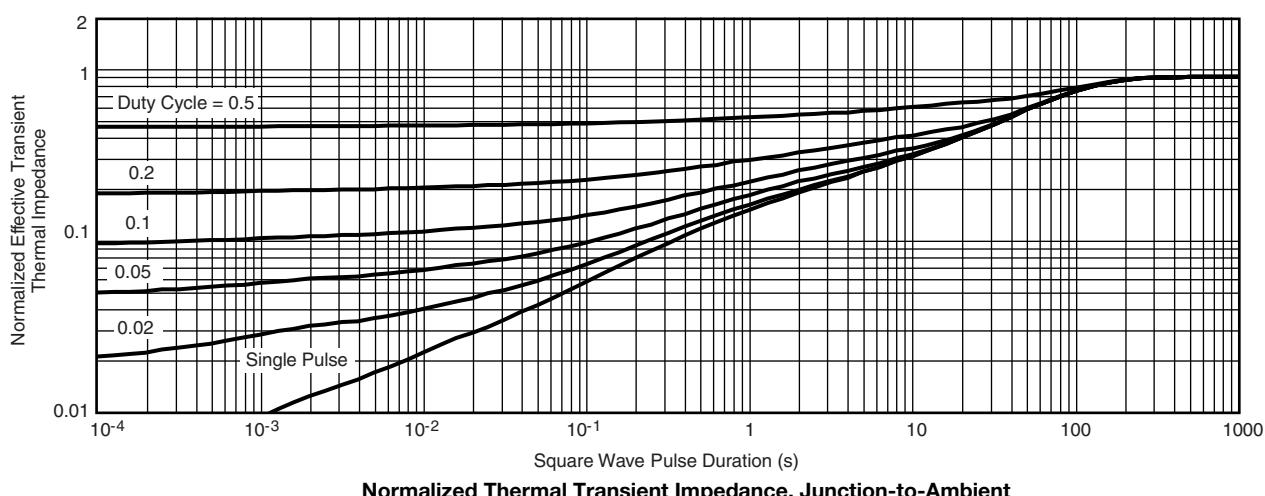
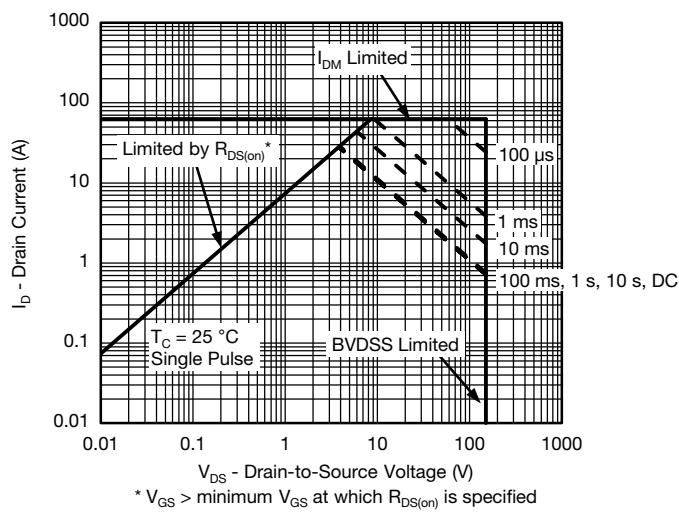
**Notes**

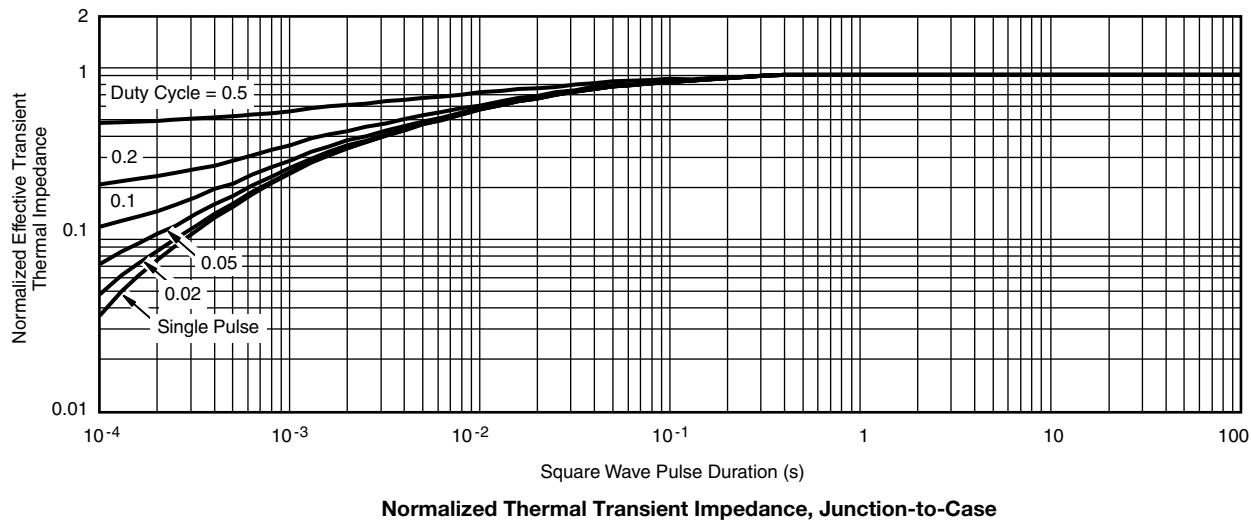
- Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\text{ \%}$ .
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)


**TYPICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)


**THERMAL RATINGS** ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)


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**Note**

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to- Ambient ( $25^\circ\text{C}$ )
  - Normalized Transient Thermal Impedance Junction-to-Case ( $25^\circ\text{C}$ )

are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?268604](http://www.vishay.com/ppg?268604).

## DPAK / TO-252 and Reverse DPAK

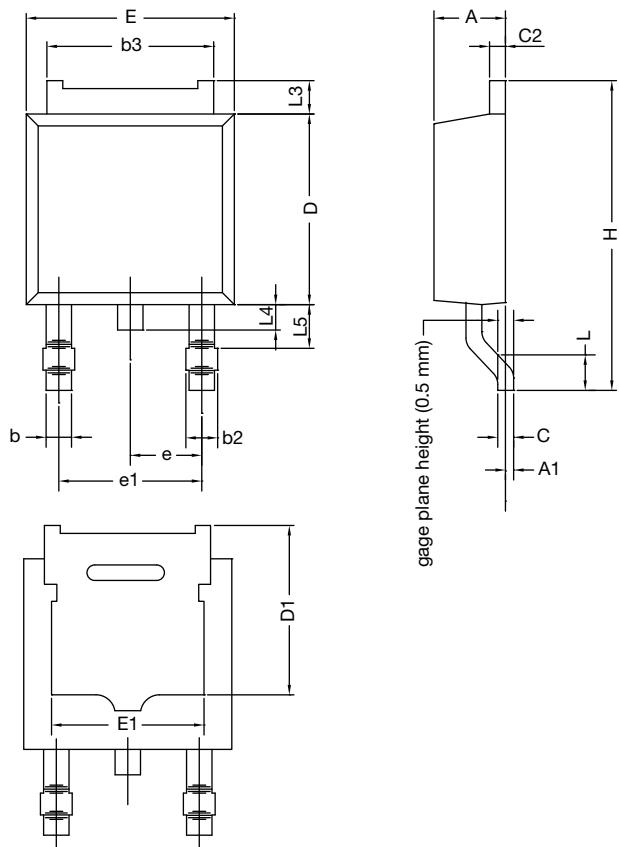
Ordering codes for the SQ rugged series power MOSFETs in the DPAK / TO-252 and Reverse DPAK packages:

DATASHEET PART NUMBER	OLD ORDERING CODE <sup>a</sup>	NEW ORDERING CODE
SQD07N25-350H	SQD07N25-350H-GE3	<b>SQD07N25-350H_GE3</b>
SQD100N03-3m2L	SQD100N03-3M2L-GE3	<b>SQD100N03-3M2L_GE3</b>
SQD100N03-3m4	SQD100N03-3M4-GE3	<b>SQD100N03-3M4_GE3</b>
SQD100N04-3m6	SQD100N04-3M6-GE3	<b>SQD100N04-3M6_GE3</b>
SQD100N04-3m6L	SQD100N04-3M6L-GE3	<b>SQD100N04-3M6L_GE3</b>
SQD10N30-330H	SQD10N30-330H-GE3	<b>SQD10N30-330H_GE3</b>
SQD15N06-42L	SQD15N06-42L-GE3	<b>SQD15N06-42L_GE3</b>
SQD19P06-60L	SQD19P06-60L-GE3	<b>SQD19P06-60L_GE3</b>
SQD23N06-31L	SQD23N06-31L-GE3	<b>SQD23N06-31L_GE3</b>
SQD25N06-22L	SQD25N06-22L-GE3	<b>SQD25N06-22L_GE3</b>
SQD25N15-52	SQD25N15-52-GE3	<b>SQD25N15-52_GE3</b>
SQD30N05-20L	SQD30N05-20L-GE3	<b>SQD30N05-20L_GE3</b>
SQD40N06-14L	SQD40N06-14L-GE3	<b>SQD40N06-14L_GE3</b>
SQD40N10-25	SQD40N10-25-GE3	<b>SQD40N10-25_GE3</b>
SQD40P10-40L	SQD40P10-40L-GE3	<b>SQD40P10-40L_GE3</b>
SQD45P03-12	SQD45P03-12-GE3	<b>SQD45P03-12_GE3</b>
SQD50N04-5m6	SQD50N04-5M6-GE3	<b>SQD50N04-5M6_GE3</b>
SQD50N05-11L	SQD50N05-11L-GE3	<b>SQD50N05-11L_GE3</b>
SQD50N06-09L	SQD50N06-09L-GE3	<b>SQD50N06-09L_GE3</b>
SQD50N10-8m9L	SQD50N10-8M9L-GE3	<b>SQD50N10-8M9L_GE3</b>
SQD50P03-07	SQD50P03-07-GE3	<b>SQD50P03-07_GE3</b>
SQD50P04-13L	SQD50P04-13L-GE3	<b>SQD50P04-13L_GE3</b>
SQD50P04-09L	SQD50P04-09L-GE3	<b>SQD50P04-09L_GE3</b>
SQD50P06-15L	SQD50P06-15L-GE3	<b>SQD50P06-15L_GE3</b>
SQD50P08-25L	SQD50P08-25L-GE3	<b>SQD50P08-25L_GE3</b>
SQD50P08-28	SQD50P08-28-GE3	<b>SQD50P08-28_GE3</b>
SQD90P04-9m4L	SQD90P04-9M4L-GE3	<b>SQD90P04-9M4L_GE3</b>
SQD97N06-6m3L	SQD97N06-6M3L-GE3	<b>SQD97N06-6M3L_GE3</b>
SQR40N10-25	SQR40N10-25-GE3	<b>SQR40N10-25_GE3</b>
SQR50N04-3m8	SQR50N04-3M8-GE3	<b>SQR50N04-3M8_GE3</b>

**Note**

a. Old ordering code is obsolete and no longer valid for new orders

### TO-252AA Case Outline



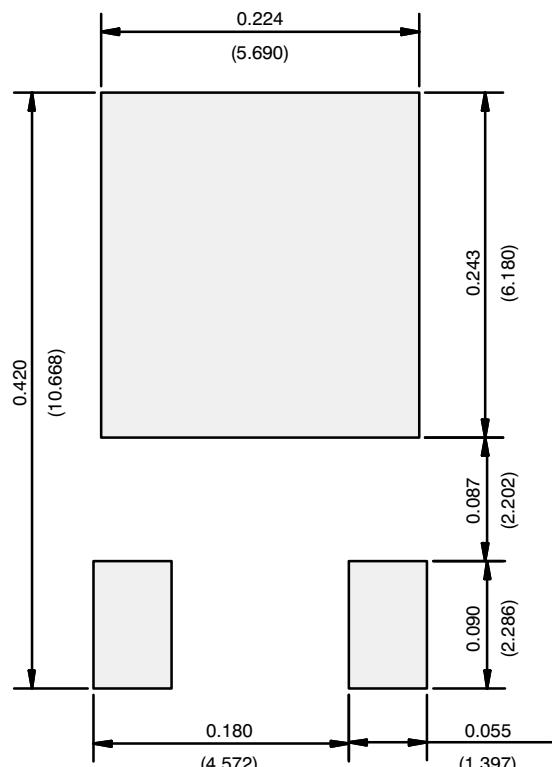
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060

ECN: T13-0592-Rev. A, 02-Sep-13  
DWG: 6019

#### Note

- Dimension L3 is for reference only.

## RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



[Return to Index](#)

APPLICATION NOTE

## Disclaimer

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