

Automotive P-Channel 30 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	- 30
$R_{DS(on)}$ (Ω) at $V_{GS} = - 10$ V	0.007
$R_{DS(on)}$ (Ω) at $V_{GS} = - 4.5$ V	0.011
I_D (A)	- 50
Configuration	Single

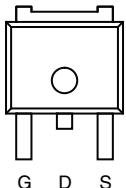
FEATURES

- TrenchFET® Power MOSFET
- AEC-Q101 Qualified^d
- 100 % R_g and UIS Tested
- Material categorization:
For definitions of compliance please see www.vishay.com/doc?99912



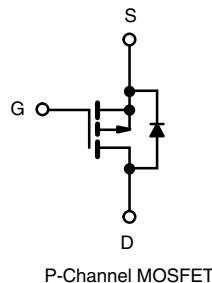
RoHS
COMPLIANT
HALOGEN
FREE

TO-252



Drain Connected to Tab

Top View



P-Channel MOSFET

ORDERING INFORMATION

Package	TO-252
Lead (Pb)-free and Halogen-free	SQD50P03-07-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	- 30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ^a	I_D	- 50	
		- 50	
Continuous Source Current (Diode Conduction) ^a	I_S	- 50	A
Pulsed Drain Current ^b	I_{DM}	- 200	
Single Pulse Avalanche Current	I_{AS}	- 50	mJ
Single Pulse Avalanche Energy	E_{AS}	125	
Maximum Power Dissipation ^b	P_D	136	W
		45	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 175	°C

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient	R_{thJA}	50	°C/W
Junction-to-Case (Drain)	R_{thJC}	1.1	

Notes

- Package limited.
- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %.
- When mounted on 1" square PCB (FR-4 material).
- Parametric verification ongoing.

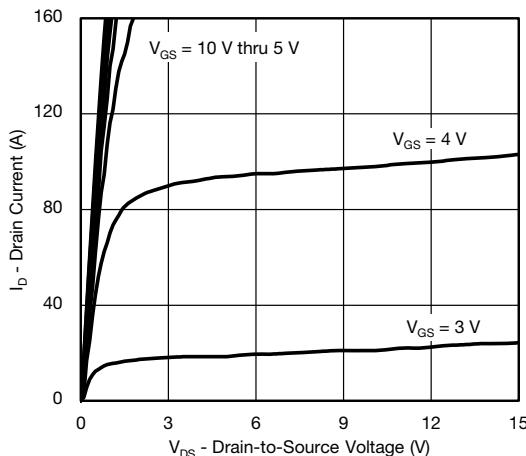
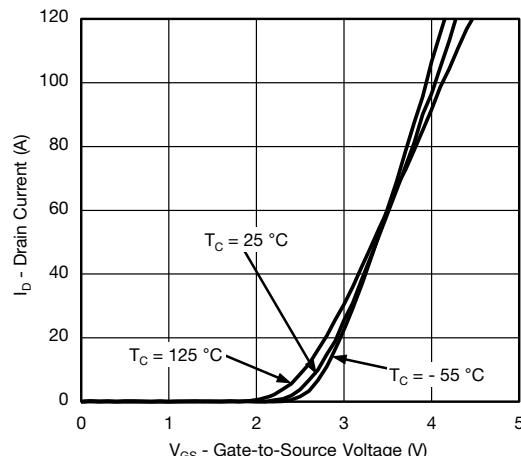
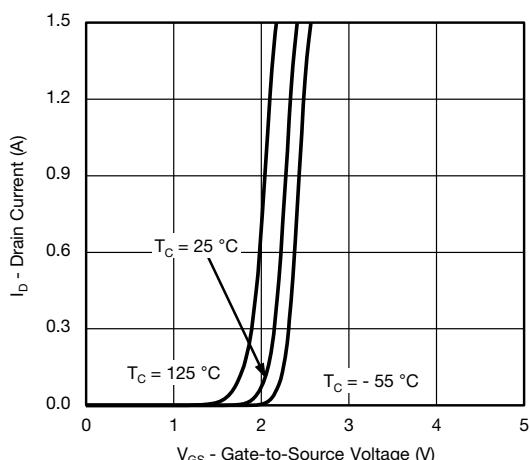
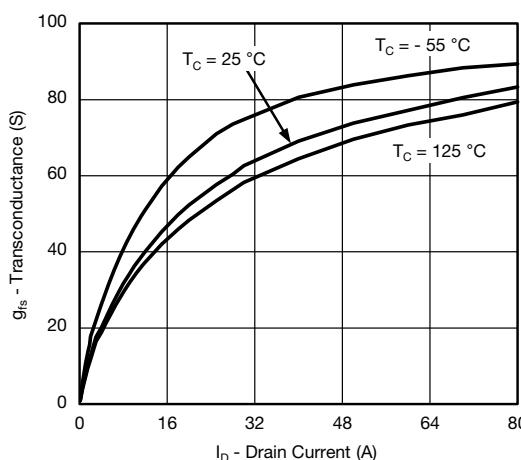
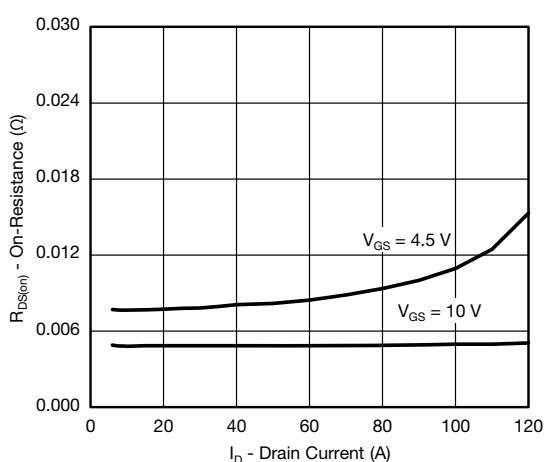
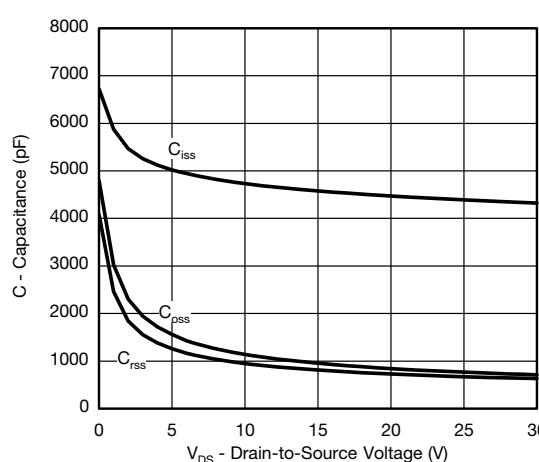
SPECIFICATIONS ($T_C = 25^\circ\text{C}$, unless otherwise noted)

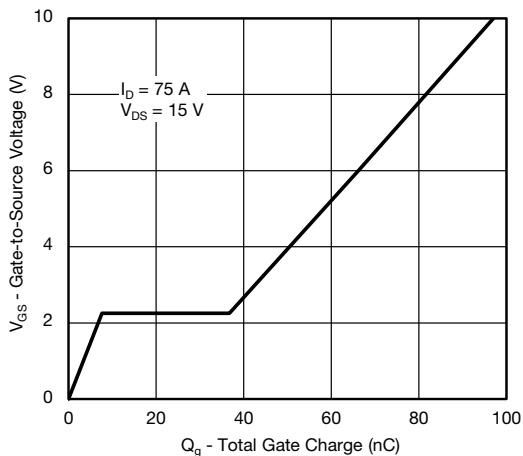
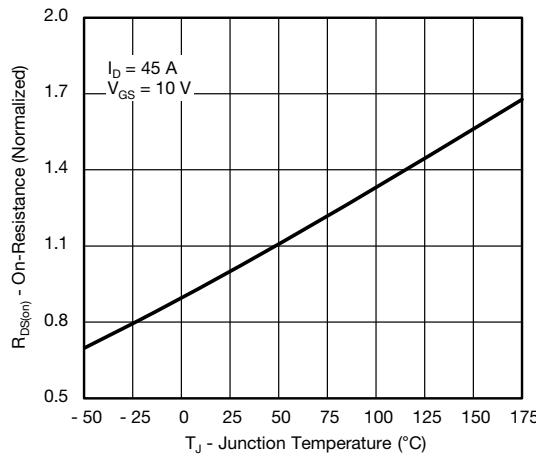
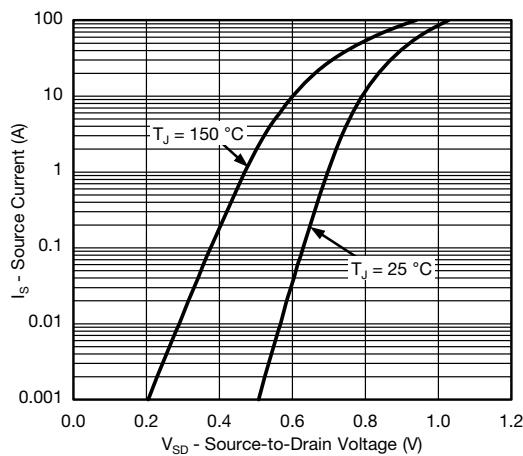
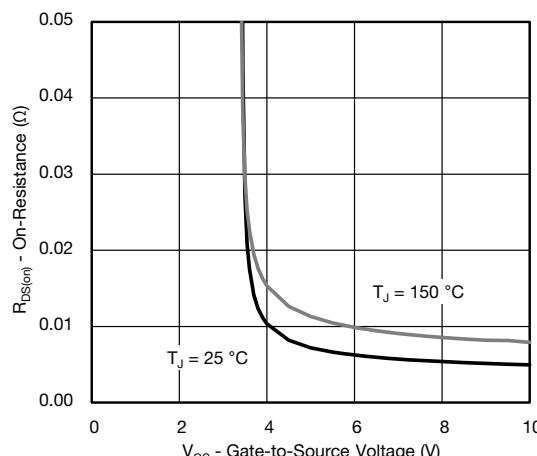
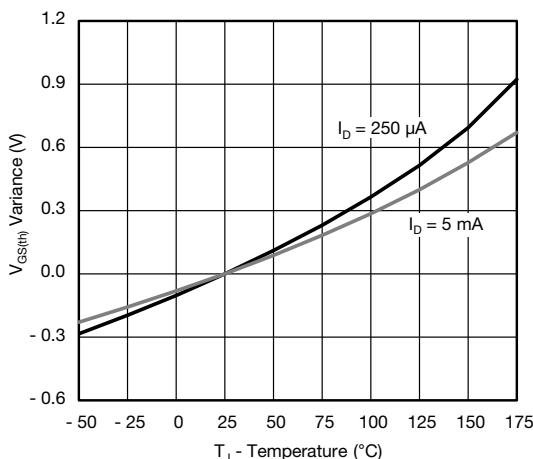
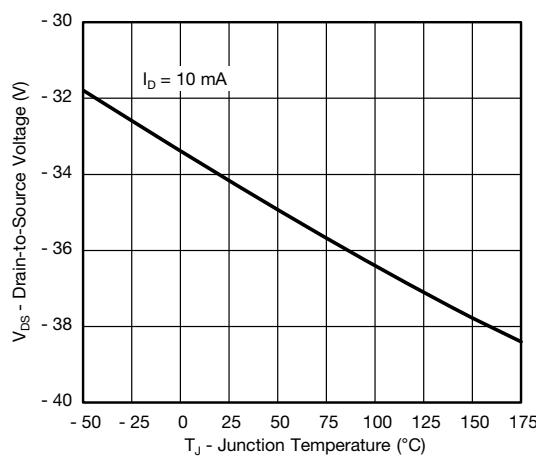
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static								
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0$, $I_D = -250 \mu\text{A}$		- 30	-	-	V	
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = -250 \mu\text{A}$		- 1.5	- 2.0	- 2.5		
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}$, $V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0 \text{ V}$	$V_{DS} = -30 \text{ V}$	-	-	- 1	μA	
		$V_{GS} = 0 \text{ V}$	$V_{DS} = -30 \text{ V}$, $T_J = 125^\circ\text{C}$	-	-	- 50		
		$V_{GS} = 0 \text{ V}$	$V_{DS} = -30 \text{ V}$, $T_J = 175^\circ\text{C}$	-	-	- 250		
On-State Drain Current ^a	$I_{D(\text{on})}$	$V_{GS} = -10 \text{ V}$	$V_{DS} \leq -5 \text{ V}$	- 50	-	-	A	
Drain-Source On-State Resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = -10 \text{ V}$	$I_D = -20 \text{ A}$	-	0.005	0.007	Ω	
		$V_{GS} = -10 \text{ V}$	$I_D = -20 \text{ A}$, $T_J = 125^\circ\text{C}$	-	-	0.011		
		$V_{GS} = -10 \text{ V}$	$I_D = -20 \text{ A}$, $T_J = 175^\circ\text{C}$	-	-	0.012		
		$V_{GS} = -4.5 \text{ V}$	$I_D = -15 \text{ A}$	-	0.008	0.011		
Forward Transconductance ^b	g_{fs}	$V_{DS} = -15 \text{ V}$, $I_D = -20 \text{ A}$		-	52	-	S	
Dynamic^b								
Input Capacitance	C_{iss}	$V_{GS} = 0 \text{ V}$	$V_{DS} = -25 \text{ V}$, $f = 1 \text{ MHz}$	-	4390	5490	pF	
Output Capacitance	C_{oss}			-	766	960		
Reverse Transfer Capacitance	C_{rss}			-	672	840		
Total Gate Charge ^c	Q_g	$V_{GS} = -10 \text{ V}$	$V_{DS} = -15 \text{ V}$, $I_D = -75 \text{ A}$	-	97	146	nC	
Gate-Source Charge ^c	Q_{gs}			-	7.6	-		
Gate-Drain Charge ^c	Q_{gd}			-	29.1	-		
Gate Resistance	R_g	$f = 1 \text{ MHz}$		1.40	2.85	4.50	Ω	
Turn-On Delay Time ^c	$t_{d(\text{on})}$	$V_{DD} = -15 \text{ V}$, $R_L = 0.2 \Omega$ $I_D \approx -75 \text{ A}$, $V_{GEN} = -10 \text{ V}$, $R_g = 1 \Omega$		-	11	17	ns	
Rise Time ^c	t_r			-	12	18		
Turn-Off Delay Time ^c	$t_{d(\text{off})}$			-	63	95		
Fall Time ^c	t_f			-	28	42		
Source-Drain Diode Ratings and Characteristics^b								
Pulsed Current ^a	I_{SM}			-	-	- 200	A	
Forward Voltage	V_{SD}	$I_F = -30 \text{ A}$, $V_{GS} = 0$		-	- 0.85	- 1.5	V	

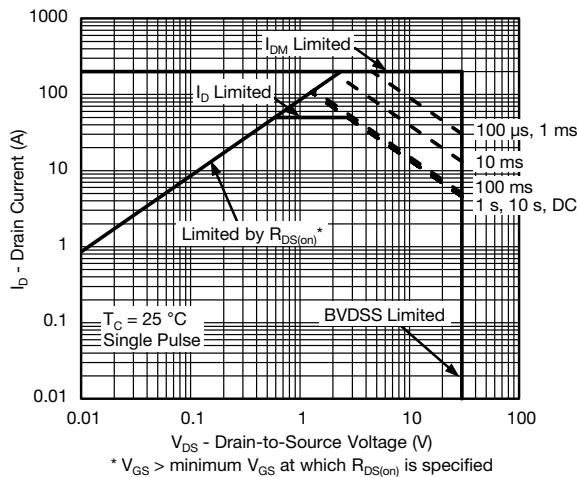
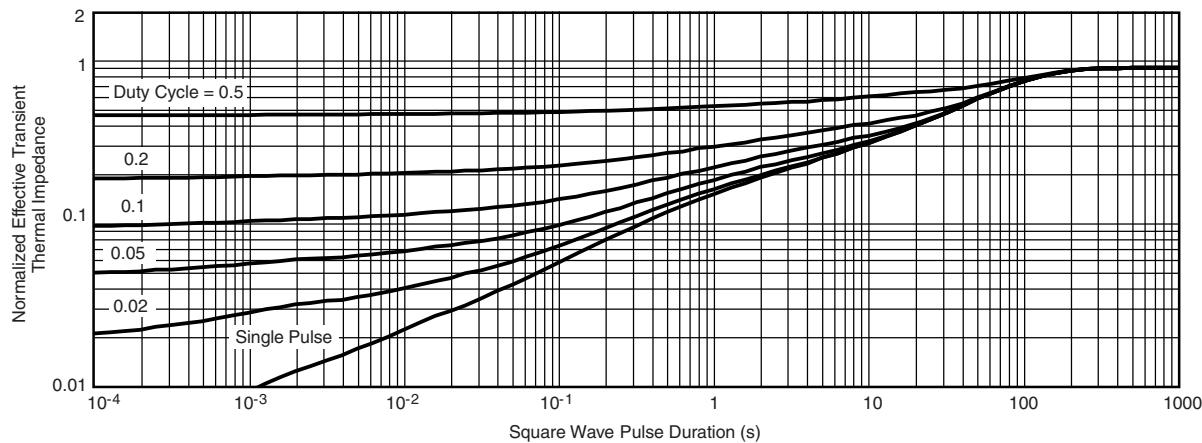
Notes

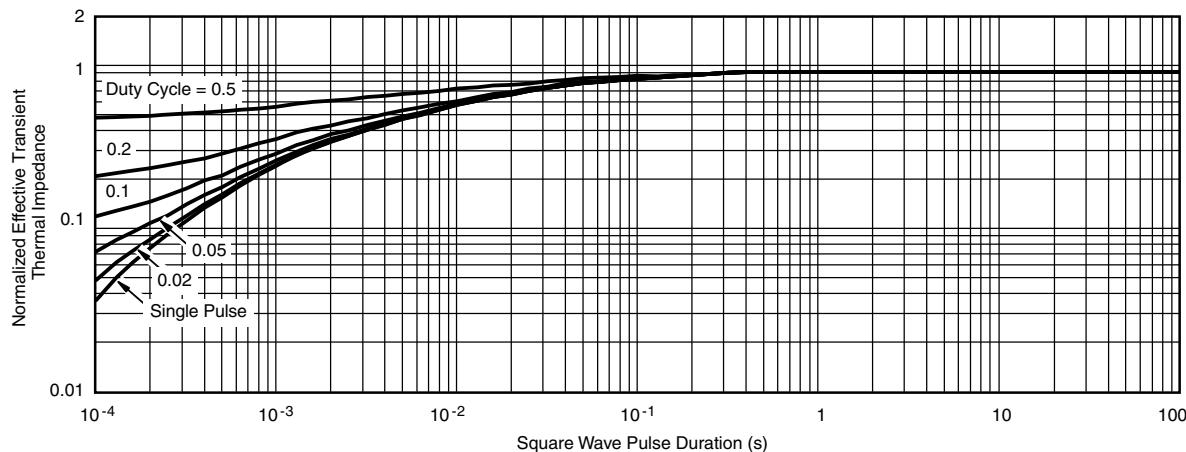
- Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Output Characteristics

Transfer Characteristics

Transfer Characteristics

Transconductance

On-Resistance vs. Drain Current

Capacitance

TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Gate Charge

On-Resistance vs. Junction Temperature

Source Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Drain Source Breakdown vs. Junction Temperature

THERMAL RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Safe Operating Area

Normalized Thermal Transient Impedance, Junction-to-Ambient

THERMAL RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Case
Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25°C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25°C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67014.

DPAK / TO-252 and Reverse DPAK

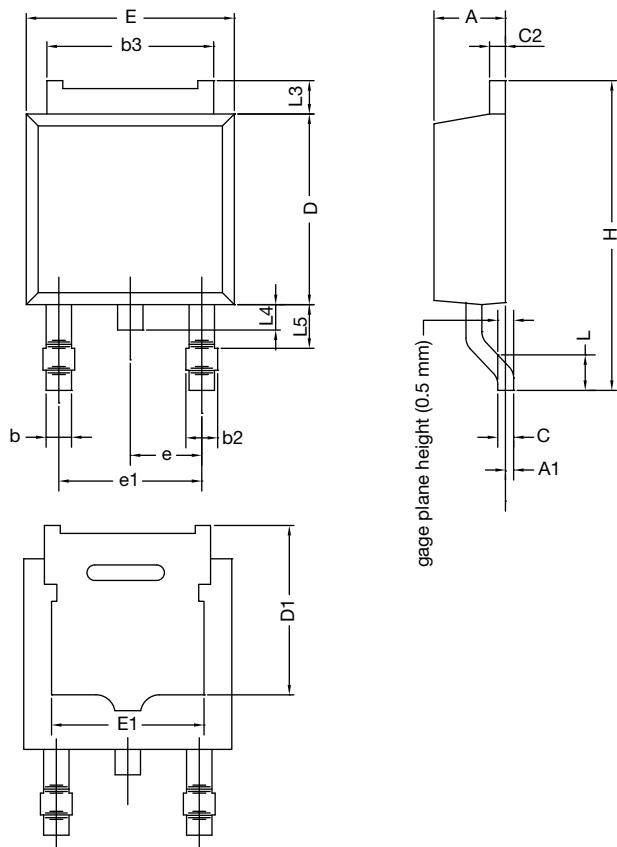
Ordering codes for the SQ rugged series power MOSFETs in the DPAK / TO-252 and Reverse DPAK packages:

DATASHEET PART NUMBER	OLD ORDERING CODE ^a	NEW ORDERING CODE
SQD07N25-350H	SQD07N25-350H-GE3	SQD07N25-350H_GE3
SQD100N02-3m5L	-	SQD100N02-3m5L_GE3
SQD100N03-3m2L	SQD100N03-3M2L-GE3	SQD100N03-3M2L_GE3
SQD100N03-3m4	SQD100N03-3M4-GE3	SQD100N03-3M4_GE3
SQD100N04-3m6	SQD100N04-3M6-GE3	SQD100N04-3M6_GE3
SQD100N04-3m6L	SQD100N04-3M6L-GE3	SQD100N04-3M6L_GE3
SQD10N30-330H	SQD10N30-330H-GE3	SQD10N30-330H_GE3
SQD15N06-42L	SQD15N06-42L-GE3	SQD15N06-42L_GE3
SQD19P06-60L	SQD19P06-60L-GE3	SQD19P06-60L_GE3
SQD23N06-31L	SQD23N06-31L-GE3	SQD23N06-31L_GE3
SQD25N06-22L	SQD25N06-22L-GE3	SQD25N06-22L_GE3
SQD25N15-52	SQD25N15-52-GE3	SQD25N15-52_GE3
SQD30N05-20L	SQD30N05-20L-GE3	SQD30N05-20L_GE3
SQD40N06-14L	SQD40N06-14L-GE3	SQD40N06-14L_GE3
SQD40N10-25	SQD40N10-25-GE3	SQD40N10-25_GE3
SQD40P10-40L	SQD40P10-40L-GE3	SQD40P10-40L_GE3
SQD45P03-12	SQD45P03-12-GE3	SQD45P03-12_GE3
SQD50N04-5m6	SQD50N04-5M6-GE3	SQD50N04-5M6_GE3
SQD50N04-5m6L	-	SQD50N04-5m6L_GE3
SQD50N05-11L	SQD50N05-11L-GE3	SQD50N05-11L_GE3
SQD50N06-09L	SQD50N06-09L-GE3	SQD50N06-09L_GE3
SQD50N10-8m9L	SQD50N10-8M9L-GE3	SQD50N10-8M9L_GE3
SQD50P03-07	SQD50P03-07-GE3	SQD50P03-07_GE3
SQD50P04-13L	SQD50P04-13L-GE3	SQD50P04-13L_GE3
SQD50P04-09L	SQD50P04-09L-GE3	SQD50P04-09L_GE3
SQD50P06-15L	SQD50P06-15L-GE3	SQD50P06-15L_GE3
SQD50P08-25L	SQD50P08-25L-GE3	SQD50P08-25L_GE3
SQD50P08-28	SQD50P08-28-GE3	SQD50P08-28_GE3
SQD70140EL	-	SQD70140EL_GE3
SQD90P04-9m4L	SQD90P04-9M4L-GE3	SQD90P04-9M4L_GE3
SQD97N06-6m3L	SQD97N06-6M3L-GE3	SQD97N06-6M3L_GE3
SQR40N10-25	SQR40N10-25-GE3	SQR40N10-25_GE3
SQR50N04-3m8	SQR50N04-3M8-GE3	SQR50N04-3M8_GE3

Note

a. Old ordering code is obsolete and no longer valid for new orders

TO-252AA Case Outline



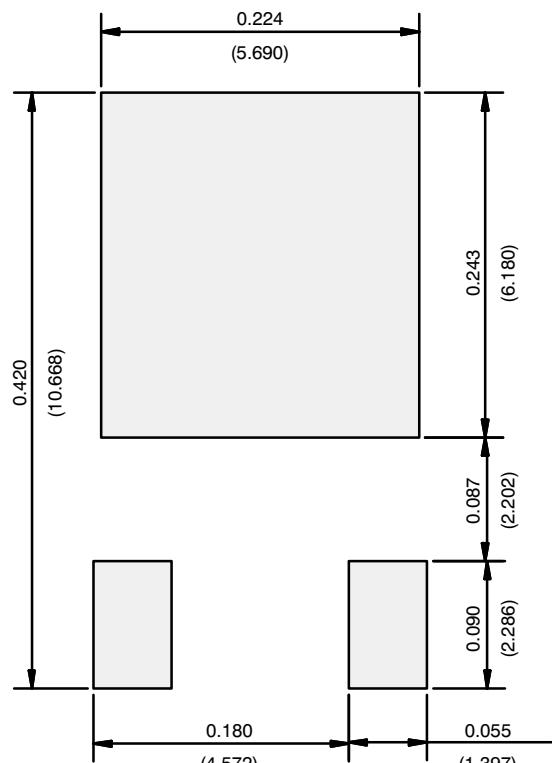
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060

ECN: T13-0592-Rev. A, 02-Sep-13
DWG: 6019

Note

- Dimension L3 is for reference only.

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



**Recommended Minimum Pads
Dimensions in Inches/(mm)**

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