

# Automotive N-Channel 40 V (D-S) 175 °C MOSFET

## PRODUCT SUMMARY

$V_{DS}$ (V)	40
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = 10$ V	0.0018
$I_D$ (A)	200
Configuration	Single
Package	TO-263-7L

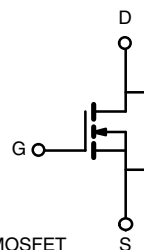
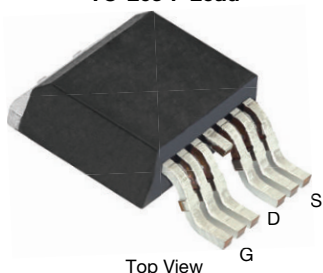
## FEATURES

- TrenchFET® power MOSFET
- Package with low thermal resistance
- 100 %  $R_g$  and UIS tested
- AEC-Q101 qualified <sup>d</sup>
- Material categorization:  
for definitions of compliance please see  
[www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

TO-263 7-Lead



N-Channel MOSFET

## ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current	$I_D$	$T_C = 25$ °C <sup>a</sup>	200
		$T_C = 125$ °C	192
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	200	A
Pulsed Drain Current <sup>b</sup>	$I_{DM}$	600	
Single Pulse Avalanche Current	$I_{AS}$	85	
Single Pulse Avalanche Energy	$E_{AS}$	361	mJ
Maximum Power Dissipation <sup>b</sup>	$P_D$	$T_C = 25$ °C	375
		$T_C = 125$ °C	125
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +175	°C

## THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient	$R_{thJA}$	40	°C/W
Junction-to-Case (Drain)	$R_{thJC}$	0.4	

### Notes

- Package limited.
- Pulse test; pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2$  %.
- When mounted on 1" square PCB (FR4 material).
- Parametric verification ongoing.



SPECIFICATIONS (T <sub>C</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		40	-	-	V
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.5	3.0	3.5	
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 40 V	-	-	1	μA
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 40 V, T <sub>J</sub> = 125 °C	-	-	50	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 40 V, T <sub>J</sub> = 175 °C	-	-	250	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> ≥ 5 V	200	-	-	A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 30 A	-	0.0015	0.0018	Ω
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 30 A, T <sub>J</sub> = 125 °C	-	-	0.0028	
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 30 A, T <sub>J</sub> = 175 °C	-	-	0.0034	
Forward Transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 30 A		-	198	-	S
Dynamic <sup>b</sup>							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 25 V, f = 1 MHz	-	13 880	17 350	pF
Output Capacitance	C <sub>oss</sub>			-	1414	1770	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	840	1050	
Total Gate Charge <sup>c</sup>	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> = 20 V, I <sub>D</sub> = 120 A	-	206	310	nC
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>			-	50	-	
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			-	44	-	
Gate Resistance	R <sub>g</sub>	f = 1 MHz		0.25	0.8	1.8	Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 20 V, R <sub>L</sub> = 0.17 Ω I <sub>D</sub> ≅ 120 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω		-	26	39	ns
Rise Time <sup>c</sup>	t <sub>r</sub>			-	21	32	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			-	68	102	
Fall Time <sup>c</sup>	t <sub>f</sub>			-	12	18	
Source-Drain Diode Ratings and Characteristics <sup>b</sup>							
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	600	A
Forward Voltage	V <sub>SD</sub>	I <sub>F</sub> = 80 A, V <sub>GS</sub> = 0 V		-	0.86	1.5	V

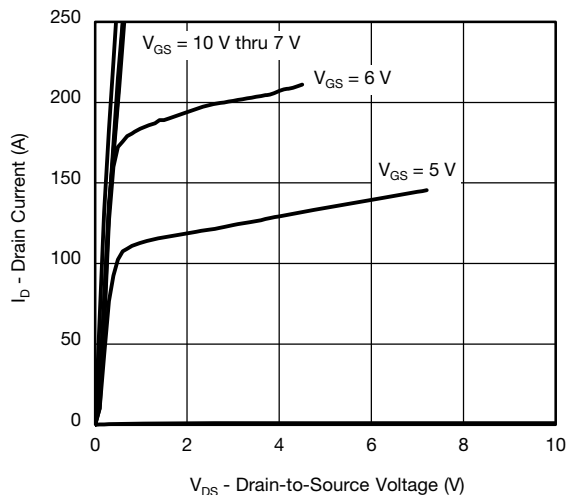
**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
b. Guaranteed by design, not subject to production testing.  
c. Independent of operating temperature.

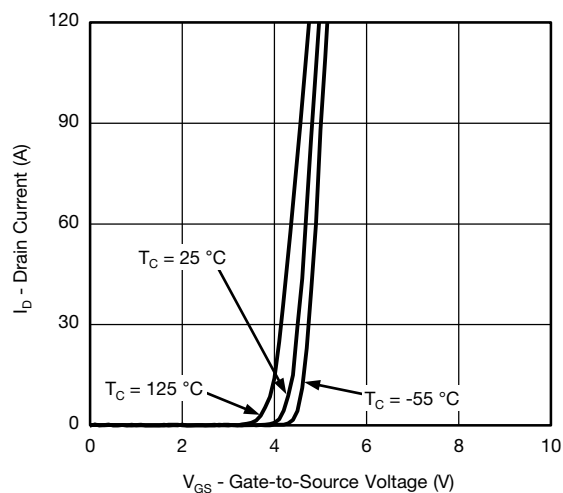
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



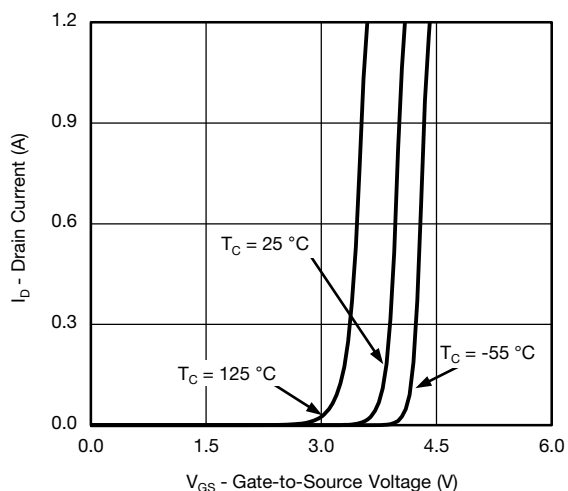
**TYPICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)



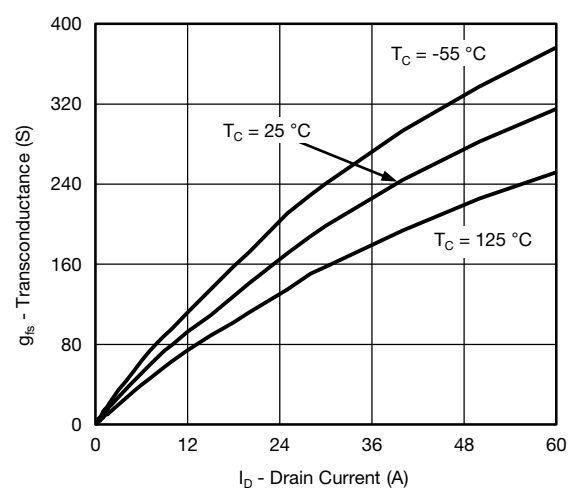
**Output Characteristics**



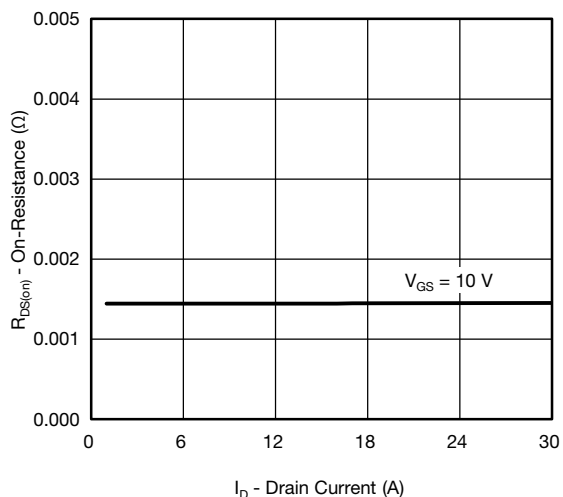
**Transfer Characteristics**



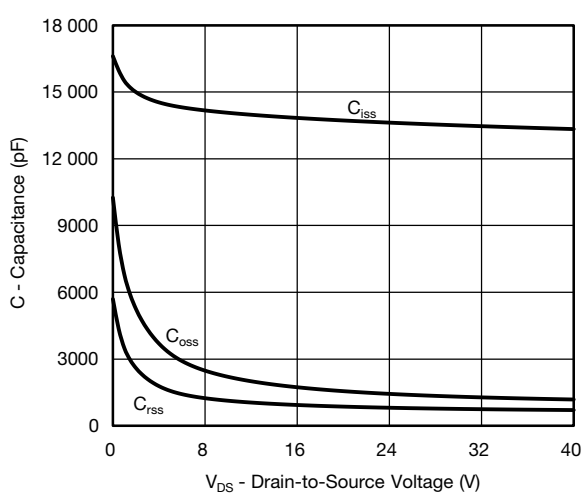
**Transfer Characteristics**



**Transconductance**



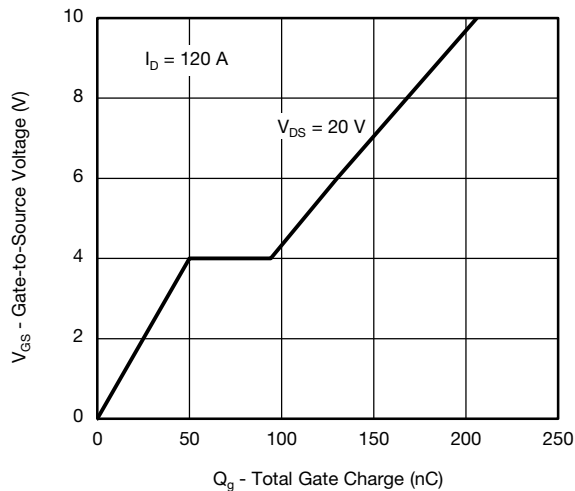
**On-Resistance vs. Drain Current**



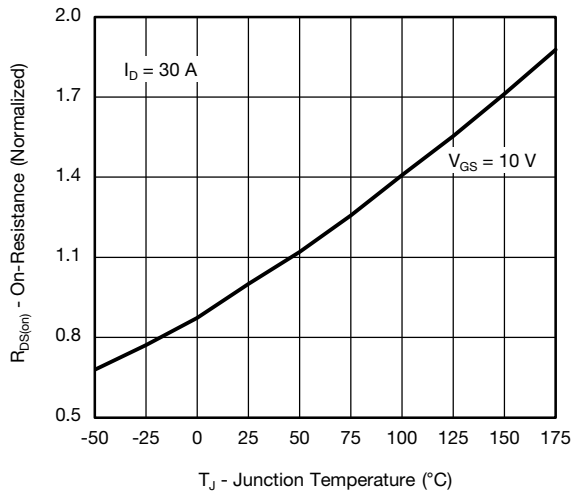
**Capacitance**



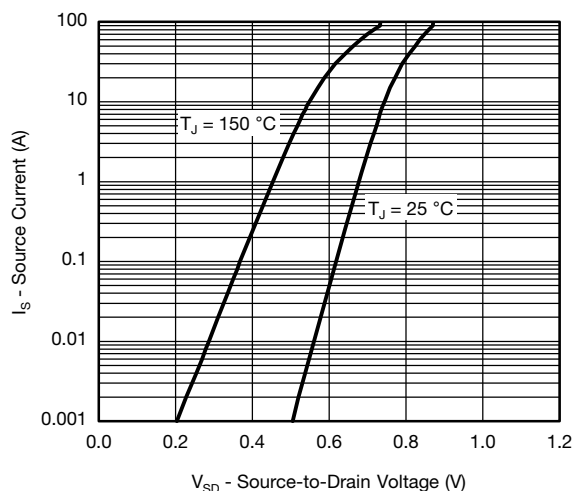
**TYPICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)



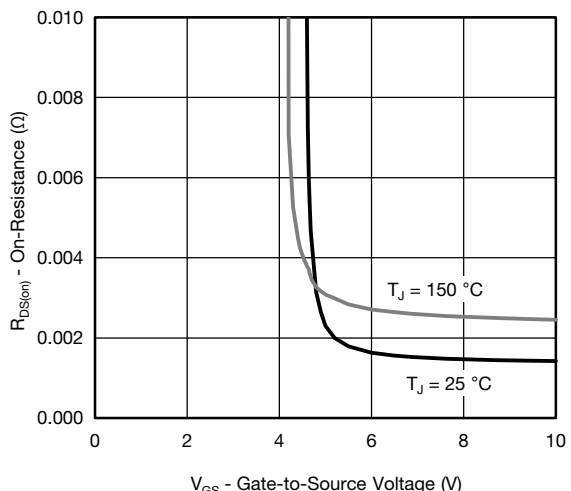
**Gate Charge**



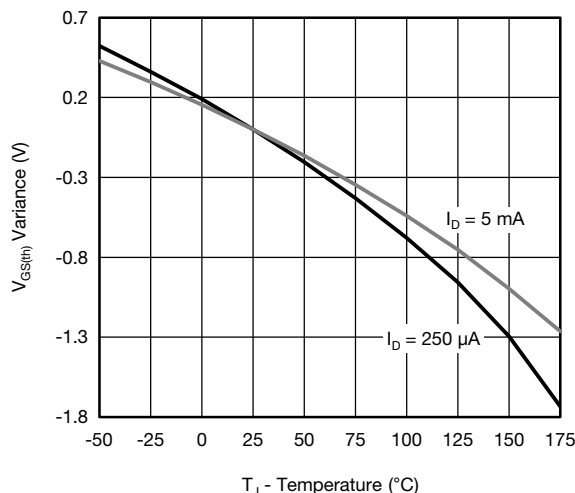
**On-Resistance vs. Junction Temperature**



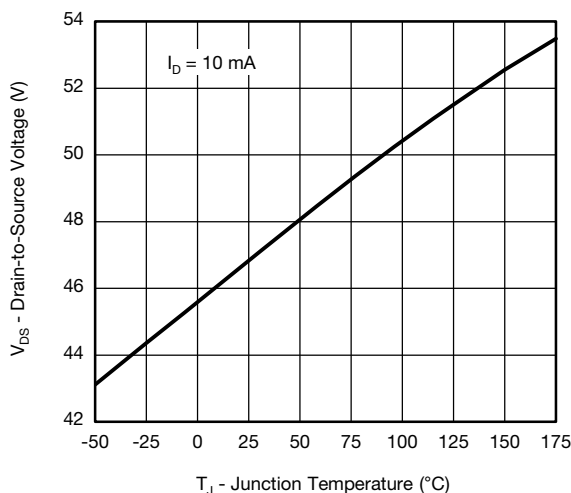
**Source Drain Diode Forward Voltage**



**On-Resistance vs. Gate-to-Source Voltage**



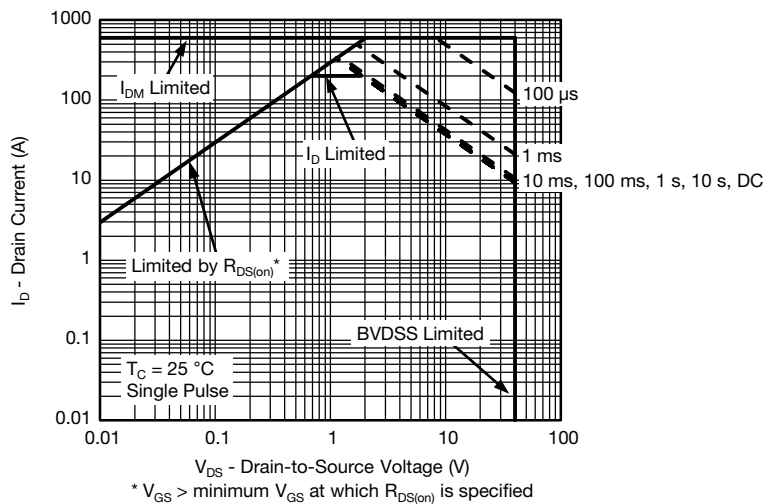
**Threshold Voltage**



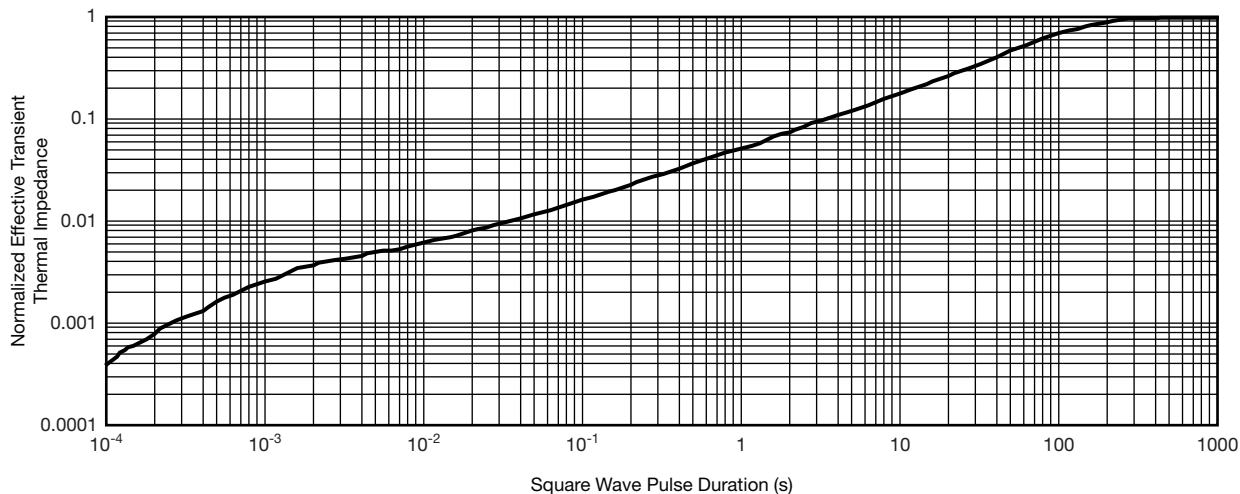
**Drain Source Breakdown vs. Junction Temperature**



**THERMAL RATINGS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



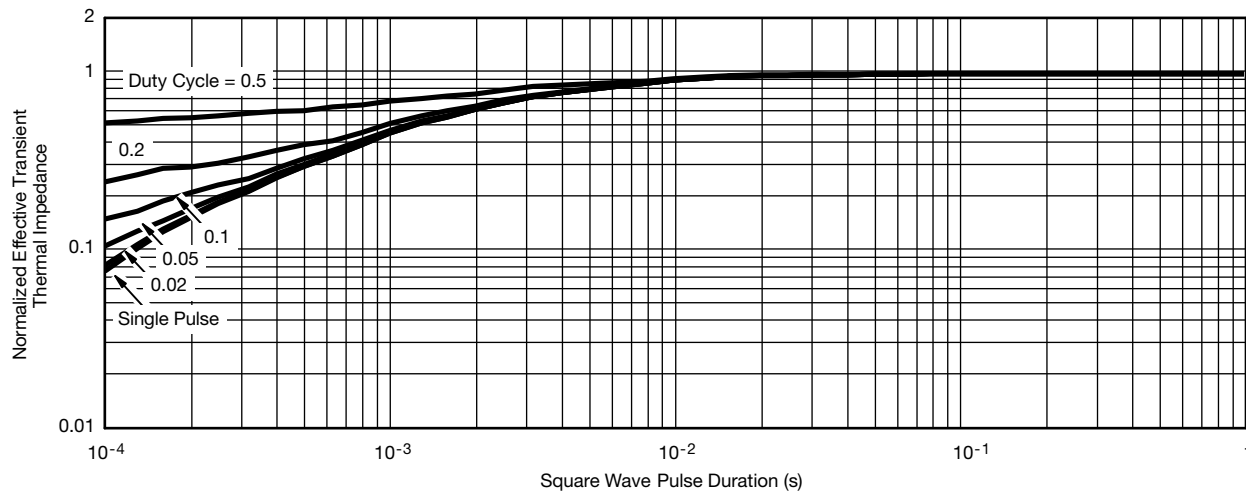
**Safe Operating Area**



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**THERMAL RATINGS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Case**

**Note**

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient ( $25\text{ }^{\circ}\text{C}$ )
  - Normalized Transient Thermal Impedance Junction-to-Case ( $25\text{ }^{\circ}\text{C}$ )are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

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REVISION HISTORY <sup>a</sup>		
REVISION	DATE	DESCRIPTION OF CHANGE
B	04-Aug-15	• Revised $R_g$ minimum limit

**Note**

a. As of April 2014

**D<sup>2</sup>PAK / TO-263 and TO-262**

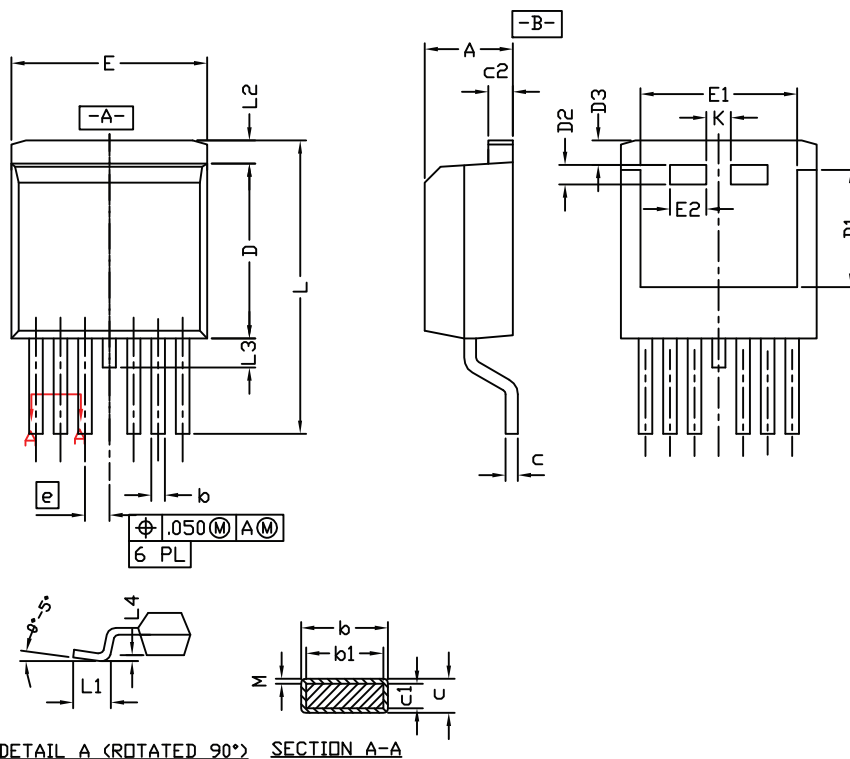
Ordering codes for the SQ rugged series power MOSFETs in the D<sup>2</sup>PAK / TO-263 and TO-262 packages:

DATASHEET PART NUMBER	OLD ORDERING CODE <sup>a</sup>	NEW ORDERING CODE
SQM100N04-2m7	SQM100N04-2M7-GE3	<b>SQM100N04-2M7_GE3</b>
SQM100N10-10	SQM100N10-10-GE3	<b>SQM100N10-10_GE3</b>
SQM110N05-06L	SQM110N05-06L-GE3	<b>SQM110N05-06L_GE3</b>
SQM110P06-8m9L	SQM110P06-8M9L-GE3	<b>SQM110P06-8M9L_GE3</b>
SQM120N02-1m3L	SQM120N02-1M3L-GE3	<b>SQM120N02-1M3L_GE3</b>
SQM120N03-1m5L	SQM120N03-1M5L-GE3	<b>SQM120N03-1M5L_GE3</b>
SQM120N04-1m7	SQM120N04-1M7-GE3	<b>SQM120N04-1M7_GE3</b>
SQM120N04-1m7L	SQM120N04-1M7L-GE3	<b>SQM120N04-1M7L_GE3</b>
SQM120N04-1m9	SQM120N04-1M9-GE3	<b>SQM120N04-1M9_GE3</b>
SQM120N06-06	SQM120N06-06-GE3	<b>SQM120N06-06_GE3</b>
SQM120N06-3m5L	SQM120N06-3M5L-GE3	<b>SQM120N06-3M5L_GE3</b>
SQM120N10-09	SQM120N10-09-GE3	<b>SQM120N10-09_GE3</b>
SQM120N10-3m8	SQM120N10-3M8-GE3	<b>SQM120N10-3M8_GE3</b>
SQM120P04-04L	SQM120P04-04L-GE3	<b>SQM120P04-04L_GE3</b>
SQM120P06-07L	SQM120P06-07L-GE3	<b>SQM120P06-07L_GE3</b>
SQM120P10-10m1L	-	<b>SQM120P10_10m1LGE3</b>
SQM200N04-1m1L	SQM200N04-1M1L-GE3	<b>SQM200N04-1M1L_GE3</b>
SQM200N04-1m7L	SQM200N04-1M7L-GE3	<b>SQM200N04-1M7L_GE3</b>
SQM200N04-1m8	SQM200N04-1M8-GE3	<b>SQM200N04-1M8_GE3</b>
SQM25N15-52	SQM25N15-52-GE3	<b>SQM25N15-52_GE3</b>
SQM35N30-97	SQM35N30-97-GE3	<b>SQM35N30-97_GE3</b>
SQM40010EL	-	<b>SQM40010EL_GE3</b>
SQM40N10-30	SQM40N10-30-GE3	<b>SQM40N10-30_GE3</b>
SQM40N15-38	SQM40N15-38-GE3	<b>SQM40N15-38_GE3</b>
SQM40P10-40L	SQM40P10-40L-GE3	<b>SQM40P10-40L_GE3</b>
SQM47N10-24L	SQM47N10-24L-GE3	<b>SQM47N10-24L_GE3</b>
SQM50020EL	-	<b>SQM50020EL_GE3</b>
SQM50N04-4m0L	SQM50N04-4M0L-GE3	<b>SQM50N04-4M0L_GE3</b>
SQM50N04-4m1	SQM50N04-4M1-GE3	<b>SQM50N04-4M1_GE3</b>
SQM50P03-07	SQM50P03-07-GE3	<b>SQM50P03-07_GE3</b>
SQM50P04-09L	SQM50P04-09L-GE3	<b>SQM50P04-09L_GE3</b>
SQM50P06-15L	SQM50P06-15L-GE3	<b>SQM50P06-15L_GE3</b>
SQM50P08-25L	SQM50P08-25L-GE3	<b>SQM50P08-25L_GE3</b>
SQM60030E	-	<b>SQM60030E_GE3</b>
SQM60N06-15	SQM60N06-15-GE3	<b>SQM60N06-15_GE3</b>
SQM60N20-35	SQM60N20-35-GE3	<b>SQM60N20-35_GE3</b>
SQM70060EL	-	<b>SQM70060EL_GE3</b>
SQM85N15-19	SQM85N15-19-GE3	<b>SQM85N15-19_GE3</b>
SQV120N10-3m8	SQV120N10-3m8-GE3	<b>SQV120N10-3m8_GE3</b>
SQV120N06-4m7L	-	<b>SQV120N06-4m7L_GE3</b>

**Note**

a. Old ordering code is obsolete and no longer valid for new orders

## D<sup>2</sup>PAK (TO-263-7L) Case Outline



### Notes

1. Plane B includes maximum features of heat sink tab and plastic.
2. No more than 25 % of L1 can fall above seating plane by max. 8 mils.
3. Pin to pin coplanarity max. 4 mils.
4. Lead thickness 25 mils.
5. For SUM part numbers lead thickness is 24 mils to 29 mils.
6. For reference only.
7. Use inches as the primary measurement.
8. This feature is only for SUM.

DIM.	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.064	4.826
b	0.020	0.039	0.508	0.990
b1	0.020	0.035	0.508	0.889
b2	0.045	0.055	1.143	1.397
c* SUB	0.012	0.018	0.305	0.457
c* SUM	0.022	0.028	0.559	0.711
c1	0.018	0.025	0.457	0.635
c2	0.045	0.055	1.143	1.397
D	0.340	0.380	8.636	9.652
D1	0.220	0.240	5.588	6.096
D2	0.038	0.042	0.965	1.067
D3	0.045	0.055	1.143	1.397
E	0.380	0.410	9.652	10.414
E1	0.245	-	6.223	-
E2	0.072	0.078	1.829	1.981
<b>[e]</b>	0.050 BSC		1.27 BSC	
K	0.045	0.055	1.143	1.397
L	0.575	0.625	14.605	15.875
L1	0.090	0.110	2.286	2.794
L2	0.040	0.055	1.016	1.397
L3	0.050	0.070	1.270	1.778
L4	0.010 BSC		0.254 BSC	
M	-	0.002	-	0.050
ECN: T13-0709-Rev. B, 30-Sep-13				
DWG: 6006				



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