SSD5000, SSD5001, SSD5002

N-CHANNEL ENHANCEMENT-MODE QUAD D-MOS FET ANALOG SWITCH ARRAYS

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

PARAMETER	SD5000	SD5001	SD5002	UNITS
V_{DS}	+20	+10	+15	Vdc
V_{SD}	+20	+10	+15	Vdc
V_{DB}	+25	+15	+22.5	Vdc
V_{SB}	+25	+15	+22.5	Vdc
V_{GS}	−25	−15	−22.5	Vdc
	+30	+25	+30	Vdc
V_{GB}	−0.3	−0.3	−0.3	Vdc
	+30	+25	+30	Vdc
V_{GD}	−25	−15	−22.5	Vdc
	+30	+25	+30	Vdc

I_D Continuous Drain Current 50mA

P_D Total Package Power Dissipation (at or below T_A = +25°C) 640mW

Linear Derating Factor ..... 10.67mW/°C

P_D Single Device Power Dissipation (at or below T_A = +25°C) 300mW

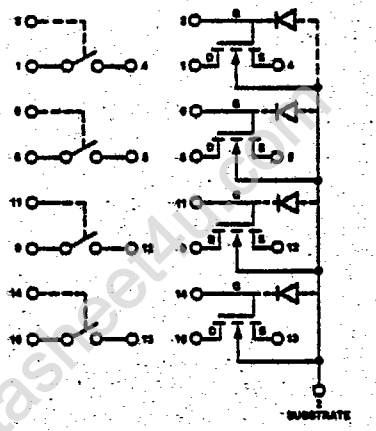
T_J Operating Junction Temperature Range ..... −55 to +85°C

T_S Storage Temperature Range .. −55 to +150°C

ORDERING INFORMATION

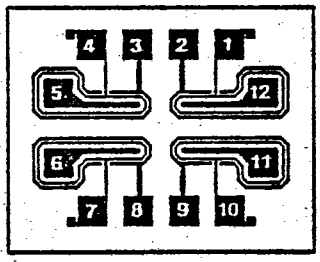
Sorted Chips in Carriers	XSD5000	XSD5001	XSD5002
Ceramic Side-Brazed DIP Pkg.	SSD5000I	SSD5001I	SSD5002I
Plastic DIP Package	SSD5000N	SSD5001N	SSD5002N

SCHEMATIC DIAGRAM



Note: Pin numbers correspond to Package Pin-out

CHIP CONFIGURATION

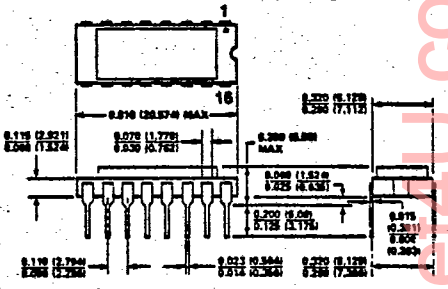


PAD NO.	PAD FUNCTION	PAD NO.	PAD FUNCTION
1	Gate No. 1	7	Gate No. 3
2	Source No. 1	8	Source No. 3
3	Source No. 2	9	Source No. 4
4	Gate No. 2	10	Gate No. 4
5	Drain No. 2	11	Drain No. 4
6	Drain No. 3	12	Drain No. 1

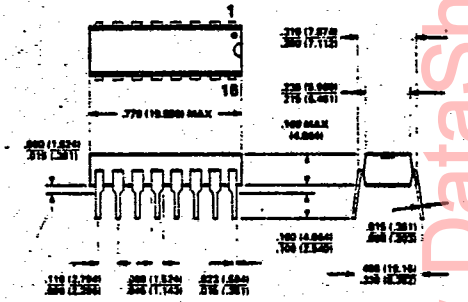
Dimensions: .040 x .032 x .010 inches

PACKAGE DIMENSIONS

Ceramic Side-Brazed "I" Package



Plastic "N" Package



All dimensions in inches and (millimeters)

SSD5000, SSD5001
SSD5002

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

#		PARAMETER		SSD5000			SSD5001			SSD5002			UNIT	TEST CONDITIONS	
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
1	STATIC	BV_{DS}	Drain-Source Breakdown Voltage	20	25		10	25		15	25		V	I_D = 10nA V_{GS} = V_{BS} = −5V	
2		BV_{SD}	Source-Drain Breakdown Voltage	20			10			15			V	I_S = 10nA V_{GD} = V_{BD} = −5V	
3		BV_{DB}	Drain-Substrate Breakdown Voltage	25			15			22.5			V	I_D = 10nA, V_{GS} = 0 Source Open	
4		BV_{SB}	Source-Substrate Breakdown Voltage	25			15			22.5			V	I_S = 10μA, V_{GB} = 0 Drain Open	
5		$I_{D(off)}$	Drain-Source Off Current						10				nA	V_{DS} = 10V	V_{GS} = V_{BS} = −5V
6												10	nA	V_{DS} = 15V	
7						10							nA	V_{DS} = 20V	
8		$I_{S(off)}$	Source-Drain OFF Current						10				nA	V_{SD} = 10V	V_{GD} = V_{BD} = −5V
9												10	nA	V_{SD} = 15V	
10						10							nA	V_{SD} = 20V	
11		I_{GBS}	Gate-Body Leakage Current					1.0					μA	V_{GB} = 25V	V_{DB} = V_{SB} = 0
12						1.0						1.0	μA	V_{GB} = 30V	
13		$V_{GS(th)}$	Gate Threshold Voltage	0.1	1.0	2.0	0.1	1.0	2.0	0.1	1.0	2.0	V	V_{DS} = V_{GS}, I_D = 1μA V_{SB} = 0	
14		$r_{DS(on)}$	Drain-Source ON Resistance		50	70		50	70		50	70	ohms	V_{GS} = 5V	I_D = 1mA V_{SB} = 0
15					30			30		30			ohms	V_{GS} = 10V	
16					23			23			23		ohms	V_{GS} = 15V	
17					19			19			19		ohms	V_{GS} = 20V	
18		r_{DSM}	ON Resistance Match		1.0	5.0		1.0	5.0		1.0	5.0	ohms	V_{GS} = 5V	
19	DYNAMIC	g_{fs}	Common-Source Forward Transcond.	10	12		10	12		10	12		mmhos	V_{DS} = 10V, I_D = 20mA f = 1KHz, VSB = 0	
20		$c_{(gs+gd+gb)}$	Gate Node Capacitance		2.4	3.5		2.4	3.5		2.4	3.5	pF	V_{DS} = 10V V_{GS} = V_{BS} = −15V f = 1MHz	
21		$c_{(gs+db)}$	Drain Node Capacitance		1.3	1.5		1.3	1.5		1.3	1.5	pF		
22		$c_{(gs+gd)}$	Source Node Capacitance		3.5	4.0		3.5	4.0		3.5	4.0	pF		
23		$c_{(dg)}$	Reverse Transfer Capacitance		0.3	0.5		0.3	0.5		0.3	0.5	pF		
24		C_T	Cross Talk		−107			−107			−107		dB		

SSD5100, SSD5101

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

#		CHARACTERISTIC		SSD5100			SSD5101			UNIT	TEST CONDITIONS
				MIN	TYP	MAX	MIN	TYP	MAX		
1	STATIC	BV_{DS}	Drain-Source Breakdown Voltage	30	35		15	30		V	I_D = 1.0μA, V_{GS} = 0
2	STATIC	BV_{SD}	Source-Drain Breakdown Voltage	0.5			0.5			V	I_S = 10nA, V_{GD} = V_{BD} = 0
3	STATIC	BV_{DB}	Drain-Substrate Breakdown Voltage	30			15			V	I_D = 1.0μA, V_{GB} = 0 Source Open
4	STATIC	BV_{SB}	Source-Substrate Breakdown Voltage	0.5			0.5			V	I_S = 100nA, V_{GB} = 0 Drain Open
5	STATIC	$I_{D(off)}$	Drain-Source OFF Current		1.0	10		1.0	10	nA	V_{DS} = 10V, V_{GS} = V_{BS} = 0
6	STATIC	I_{GBS}	Gate-Substrate Leakage Current			10			10	μA	V_{GS} = 20V, V_{DB} = V_{SB} = 0
7	STATIC	$V_{GS(th)}$	Gate-Source Threshold Voltage	0.5	1.0	2.0	0.5	1.0	2.0	V	I_D = 1.0μA, V_{DS} = V_{GS}, V_{SB} = 0
8	STATIC	$r_{DS(on)}$	Drain-Source ON Resistance		50	70		50	70	ohms	V_{GS} = 5V; I_D = 1mA, V_{SB} = 0
9	STATIC	$r_{DS(on)}$	Drain-Source ON Resistance		30	45		30	45	ohms	V_{GS} = 10V; I_D = 1mA, V_{SB} = 0
10	STATIC	$r_{DS(on)}$	Drain-Source ON Resistance		23			23		ohms	V_{GS} = 15V; I_D = 1mA, V_{SB} = 0
11	STATIC	$r_{DS(on)}$	Drain-Source ON Resistance		19			19		ohms	V_{GS} = 20V; I_D = 1mA, V_{SB} = 0
12	STATIC	r_{DSM}	ON Resistance Match		1.0	5.0		1.0	5.0	ohms	V_{GS} = 5V; I_D = 1mA, V_{SB} = 0
13	DYNAMIC	g_{fs}	Common-Source Forward Transcond	10	15		10	15		mmhos	V_{DS} = 10V, I_D = 20mA, f = 1KHz, V_{SB} = 0
14	DYNAMIC	$c_{(gs+gd+gb)}$	Gate Node Capacitance		2.4	3.5		2.4	3.5	pF	V_{DS} = 10V, V_{GS} = V_{BS} = −5V, f = 1MHZ
15	DYNAMIC	$c_{(gd+db)}$	Drain Node Capacitance		1.3	1.5		1.3	1.5	pF	V_{DS} = 10V, V_{GS} = V_{BS} = −5V, f = 1MHZ
16	DYNAMIC	c_{dg}	Reverse Transfer Capacitance		0.3	0.5		0.3	0.5	pF	V_{DS} = 10V, V_{GS} = V_{BS} = −5V, f = 1MHZ
17	DYNAMIC	C_T	Cross Talk		−107			−107		dB	f = 3KHz