

TOSHIBA Field-Effect Transistor Silicon P-Channel MOS Type

SSM3J117TU

DC-DC converter Applications

High-Speed Switching Applications

- 4 V drive
- Low ON-resistance: $R_{DS(ON)} = 225 \text{ m}\Omega$ (max) (@ $V_{GS} = -4 \text{ V}$)
 $R_{DS(ON)} = 117 \text{ m}\Omega$ (max) (@ $V_{GS} = -10 \text{ V}$)

Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

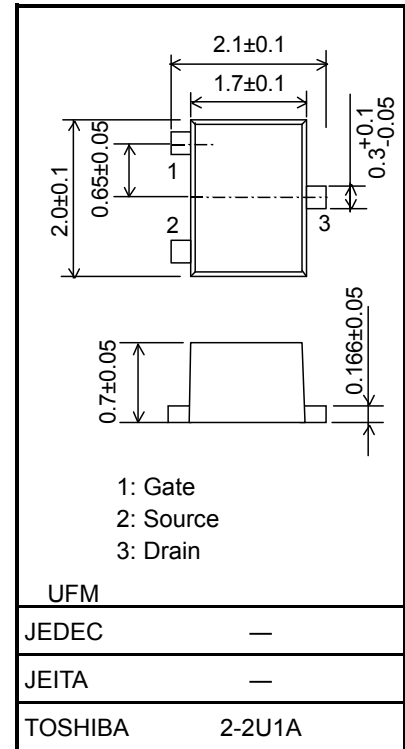
Characteristic	Symbol	Rating	Unit
Drain-source voltage	V_{DS}	-30	V
Gate-source voltage	V_{GSS}	± 20	V
Drain current	DC	I_D	A
	Pulse	I_{DP}	
Power dissipation	P_D (Note 1)	800	mW
	P_D (Note 2)	500	
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature range	T_{stg}	-55 to 150	$^\circ\text{C}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on a ceramic board.
(25.4 mm × 25.4 mm × 0.8 t, Cu Pad: 645 mm²)

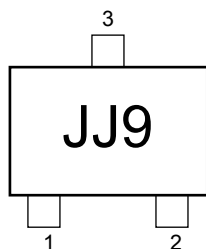
Note 2: Mounted on an FR4 board.
(25.4 mm × 25.4 mm × 1.6 t, Cu Pad: 645 mm²)

Unit: mm

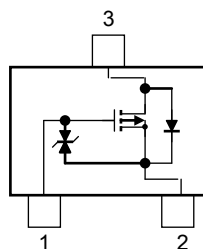


Weight: 6.6 mg (typ.)

Marking



Equivalent Circuit (top view)



Handling Precaution

When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

Start of commercial production
2005-12

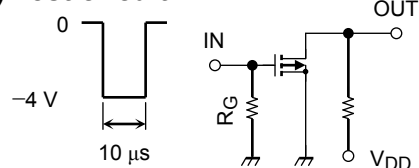
Electrical Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = -1 \text{ mA}$, $V_{GS} = 0 \text{ V}$	-30	—	—	V
	$V_{(BR)DSX}$	$I_D = -1 \text{ mA}$, $V_{GS} = +20 \text{ V}$	-15	—	—	
Drain cutoff current	I_{DSS}	$V_{DS} = -30 \text{ V}$, $V_{GS} = 0 \text{ V}$	—	—	-1	μA
Gate leakage current	I_{GSS}	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0 \text{ V}$	—	—	± 1	μA
Gate threshold voltage	V_{th}	$V_{DS} = -5 \text{ V}$, $I_D = -1 \text{ mA}$	-1.2	—	-2.6	V
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = -5 \text{ V}$, $I_D = 1 \text{ A}$ (Note 3)	1.6	3.1	—	S
Drain-source ON-resistance	$R_{DS(ON)}$	$I_D = -1 \text{ A}$, $V_{GS} = -10 \text{ V}$ (Note 3)	—	80	117	$\text{m}\Omega$
		$I_D = -0.5 \text{ A}$, $V_{GS} = -4 \text{ V}$ (Note 3)	—	160	225	
Input capacitance	C_{iss}	$V_{DS} = -15 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$	—	280	—	pF
Output capacitance	C_{oss}	$V_{DS} = -15 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$	—	80	—	pF
Reverse transfer capacitance	C_{rss}	$V_{DS} = -15 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$	—	45	—	pF
Switching time	Turn-on time	$V_{DD} = -15 \text{ V}$, $I_D = -1 \text{ A}$, $V_{GS} = 0 \text{ to } -4 \text{ V}$, $R_G = 10 \Omega$	—	16	—	ns
	Turn-off time		—	35	—	
Drain-source forward voltage	V_{DSF}	$I_D = 2 \text{ A}$, $V_{GS} = 0 \text{ V}$ (Note 3)	—	0.8	1.2	V

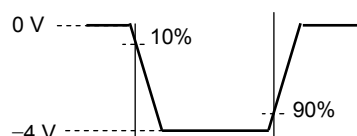
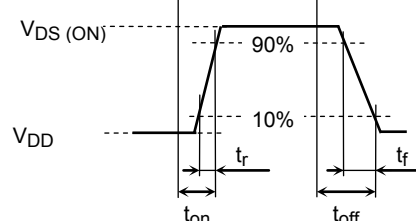
Note 3: Pulse test

Switching Time Test Circuit

(a) Test circuit



$V_{DD} = -15 \text{ V}$
 $R_G = 10 \Omega$
Duty $\leq 1 \%$
 V_{IN} : t_r , $t_f < 5 \text{ ns}$
Common Source
 $T_a = 25^\circ\text{C}$

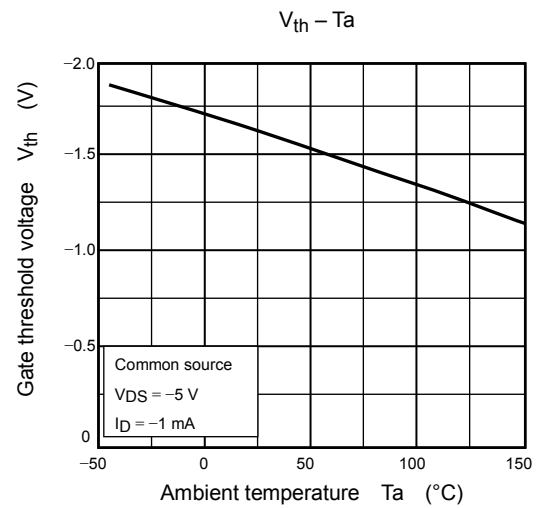
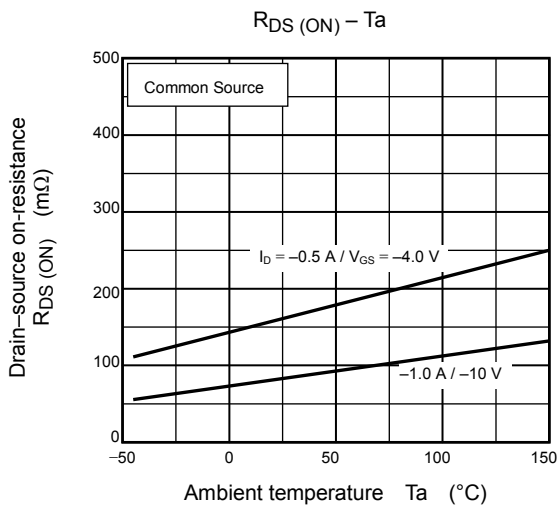
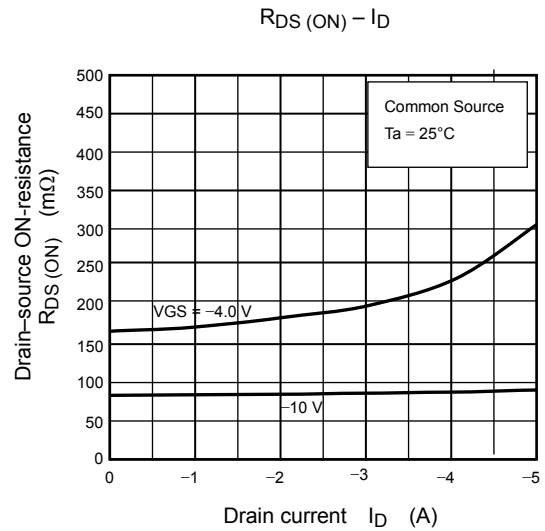
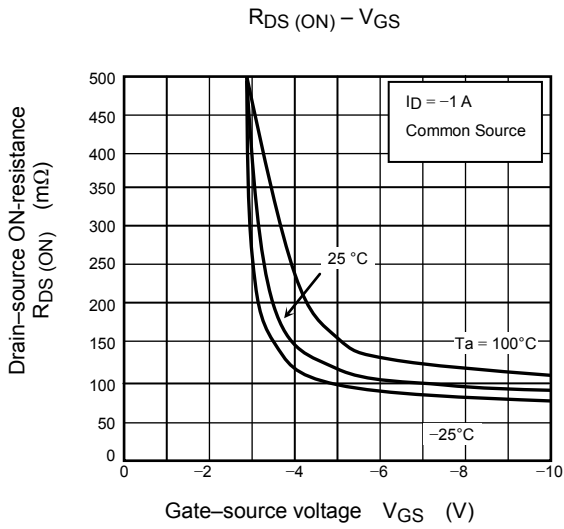
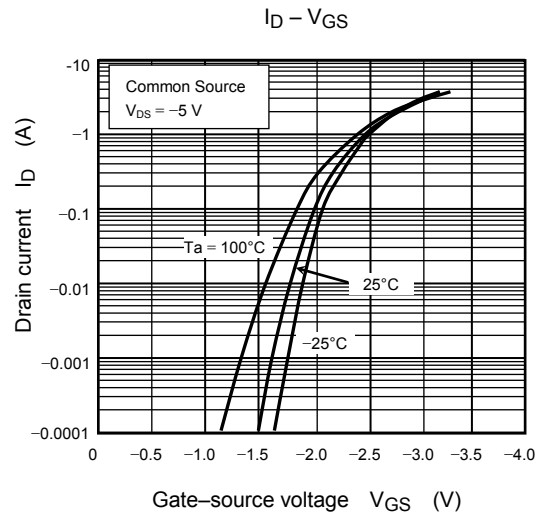
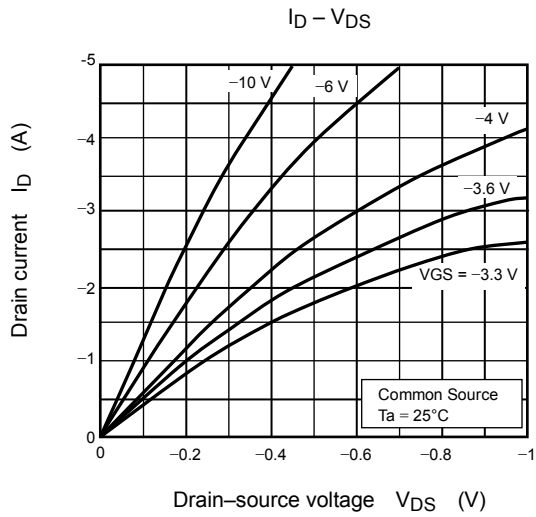
(b) V_{IN} (c) V_{OUT} 

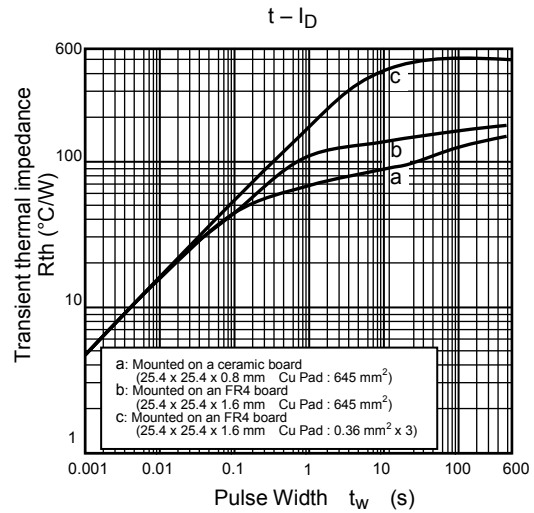
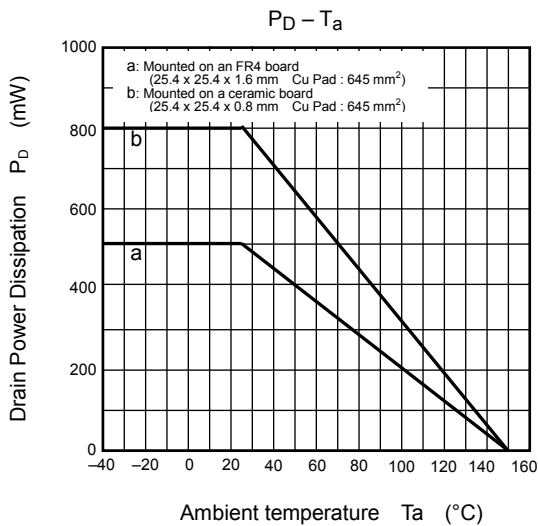
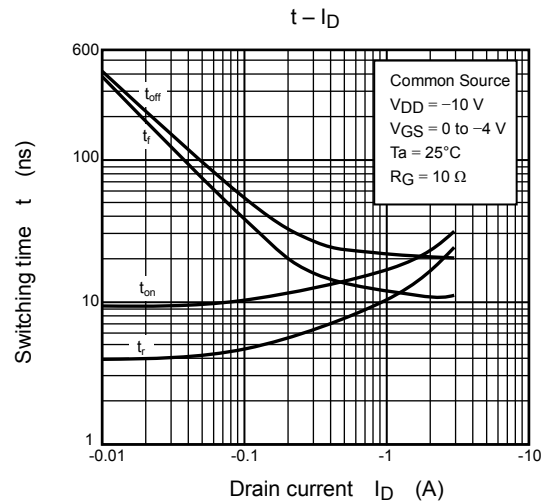
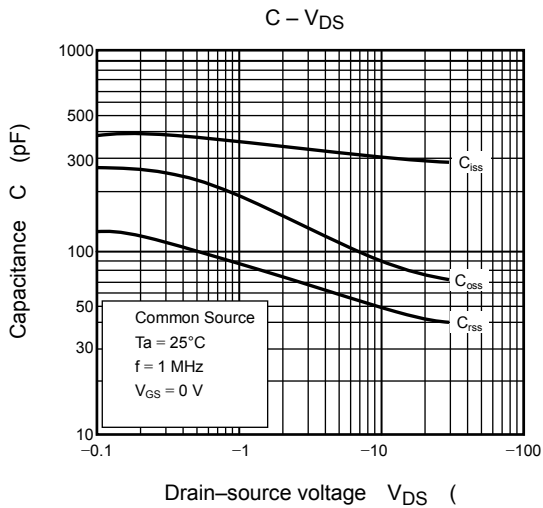
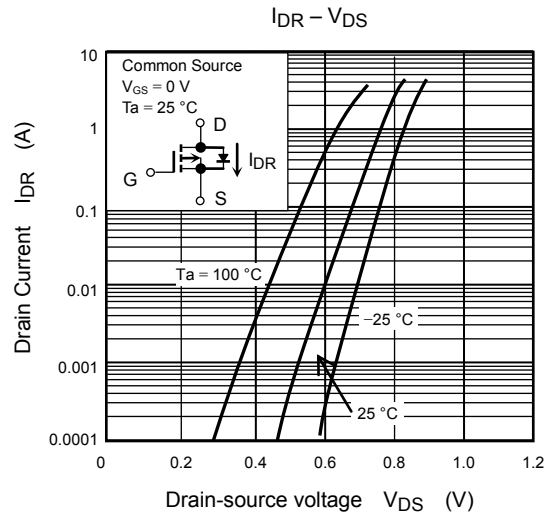
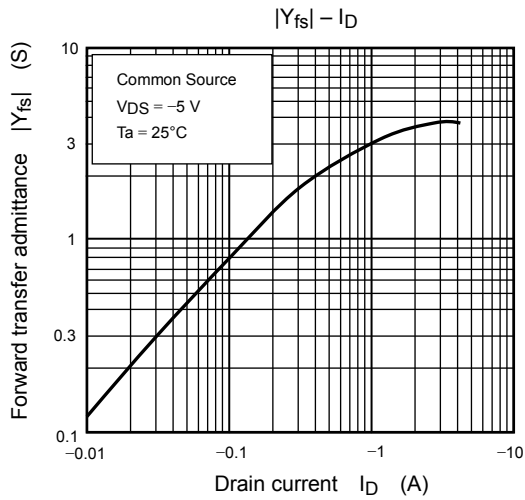
Precaution

V_{th} can be expressed as the voltage between gate and source when the low operating current value is $I_D = -1 \text{ mA}$ for this product. For normal switching operation, $V_{GS(ON)}$ requires a higher voltage than V_{th} and $V_{GS(OFF)}$ requires a lower voltage than V_{th} .

(The relationship can be established as follows: $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$.)

Take this into consideration when using the device.





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