



STP200NF04 STB200NF04 - STB200NF04-1

N-CHANNEL 40V - 120 A - 3.3 mΩ TO-220/D²PAK/I²PAK
STripFET™II MOSFET

Table 1: General Features

Type	V _{DSS}	R _{DS(on)}	I _D	P _w
STB200NF04	40 V	< 0.0037 Ω	120 A	310 W
STB200NF04-1	40 V	< 0.0037 Ω	120 A	310 W
STP200NF04	40 V	< 0.0037 Ω	120 A	310 W

- STANDARD THRESHOLD DRIVE
- 100% AVALANCHE TESTED

DESCRIPTION

This MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

- HIGH CURRENT, HIGH SWITCHING SPEED
- AUTOMOTIVE

Figure 1: Package

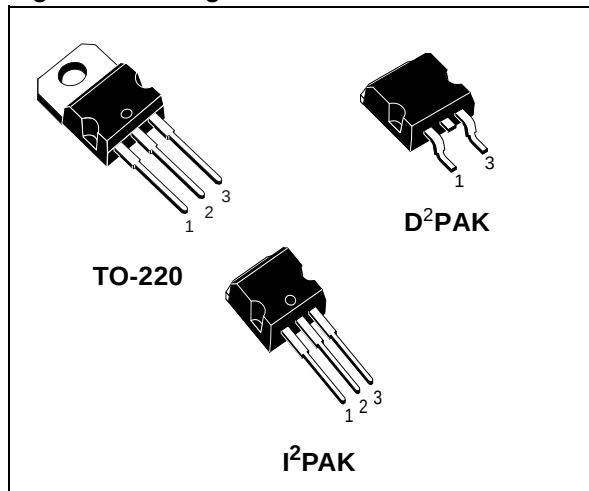


Figure 2: Internal Schematic Diagram

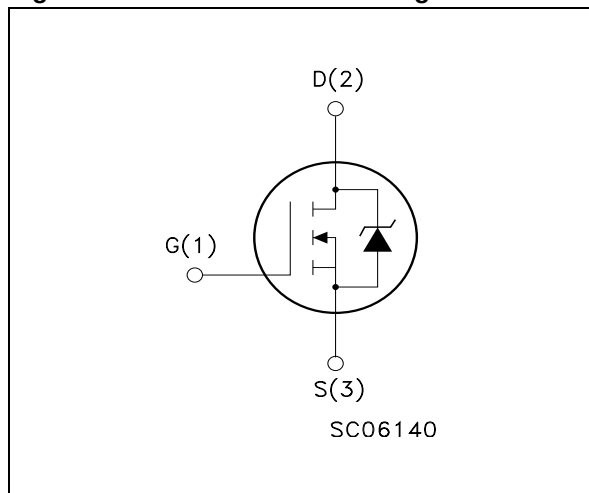


Table 2: Order Codes

SALES TYPE	MARKING	PACKAGE	PACKAGING
STB200NF04T4	B200NF04	D ² PAK	TAPE & REEL
STB200NF04-1	B200NF04	I ² PAK	TUBE
STP200NF04	P200NF04	TO-220	TUBE

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage ($V_{GS} = 0$)	40	V
V_{DGR}	Drain-gate Voltage ($R_{GS} = 20\text{ k}\Omega$)	40	V
V_{GS}	Gate- source Voltage	± 20	V
I_D (#)	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	120	A
I_D (#)	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	120	A
I_{DM} (•)	Drain Current (pulsed)	480	A
P_{TOT}	Total Dissipation at $T_C = 25^\circ\text{C}$	310	W
	Derating Factor	2.07	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	1.5	V/ns
E_{AS} (2)	Single Pulse Avalanche Energy	1.3	J
T_j T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 175	°C

(•) Pulse width limited by safe operating area

(1) $I_{SD} \leq 120\text{A}$, $di/dt \leq 500\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.(2) Starting $T_j = 25^\circ\text{C}$, $I_d = 60\text{A}$, $V_{DD} = 30\text{V}$

#) Current Limited by Package

Table 4: Thermal Data

		TO-220 / I ² PAK / D ² PAK	
Rthj-case	Thermal Resistance Junction-case Max	0.48	°C/W
Rthj-pcb	Thermal Resistance Junction-pcb Max	(see Figure 17)	°C/W
Rthj-amb	Thermal Resistance Junction-ambient (Free air) Max	62.5	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300	°C

ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^\circ\text{C}$ UNLESS OTHERWISE SPECIFIED)**Table 5: On/Off**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0$	40			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$, $T_C = 125^\circ\text{C}$			1 10	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{V}$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2		4	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{V}$, $I_D = 90\text{ A}$		3.3	3.7	m Ω

ELECTRICAL CHARACTERISTICS (CONTINUED)**Table 6: Dynamic**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	$V_{DS} = 15\text{ V}$, $I_D = 90\text{ A}$		150		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$		5100 1600 600		pF pF pF

Table 7: Switching On/Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	$V_{DD} = 20\text{ V}$, $I_D = 90\text{ A}$ $R_G = 4.7\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 20)		30 320 140 120		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 20\text{ V}$, $I_D = 120\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 23)		170 30 62	210	nC nC nC

Table 8: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				120 480	A A
V_{SD} (1)	Forward On Voltage	$I_{SD} = 120\text{ A}$, $V_{GS} = 0$			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 120\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 30\text{ V}$, $T_j = 150^\circ\text{C}$ (see Figure 21)		85 190 4.5		ns nC A

(1) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

(2) Pulse width limited by safe operating area.

Figure 3: Safe Operating Area

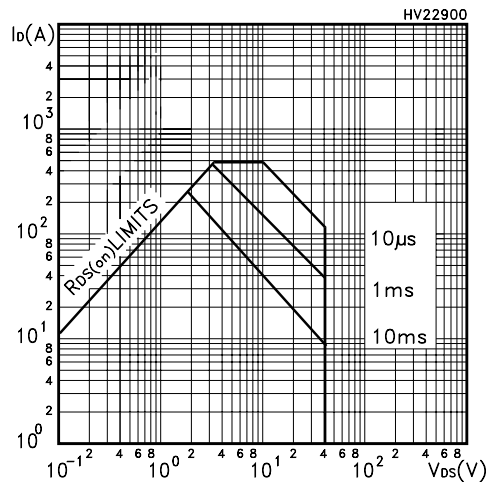


Figure 4: Output Characteristics

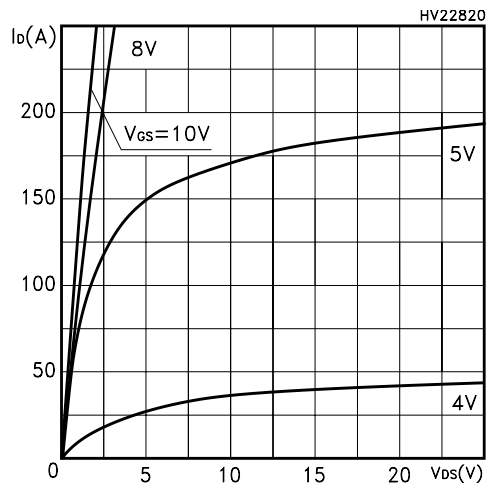


Figure 5: Transconductance

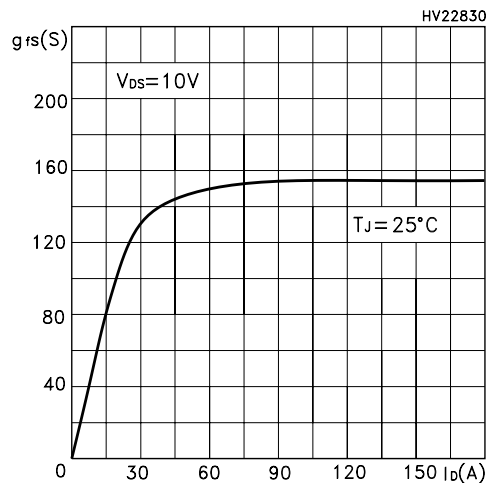


Figure 6: Thermal Impedance

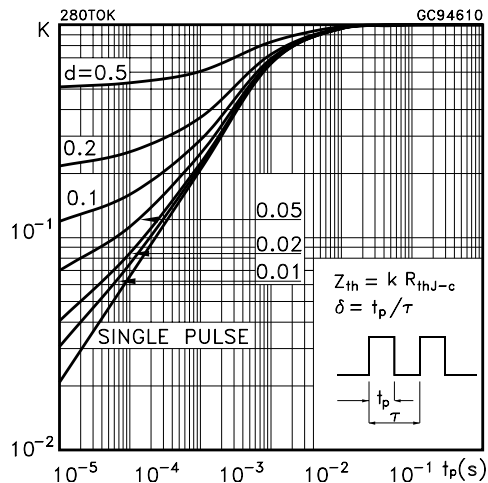


Figure 7: Transfer Characteristics

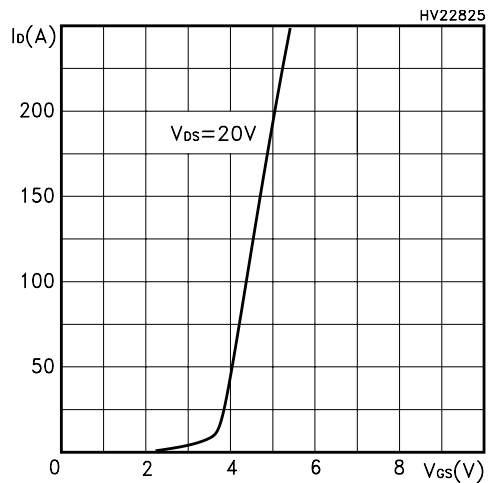


Figure 8: Static Drain-source On Resistance

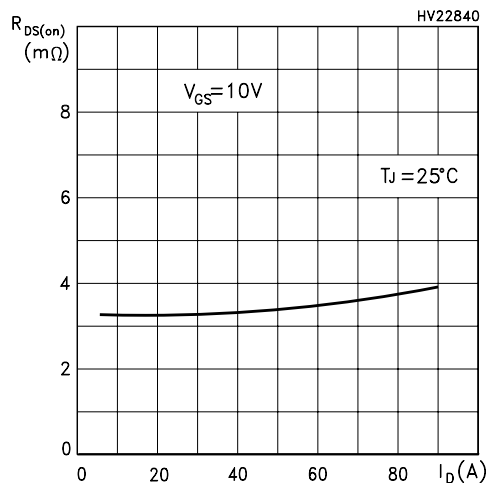


Figure 9: Gate Charge vs Gate-source Voltage

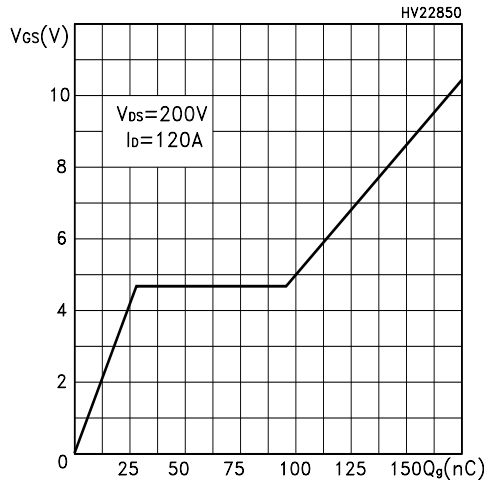


Figure 10: Normalized Gate Threshold Voltage vs Temperature

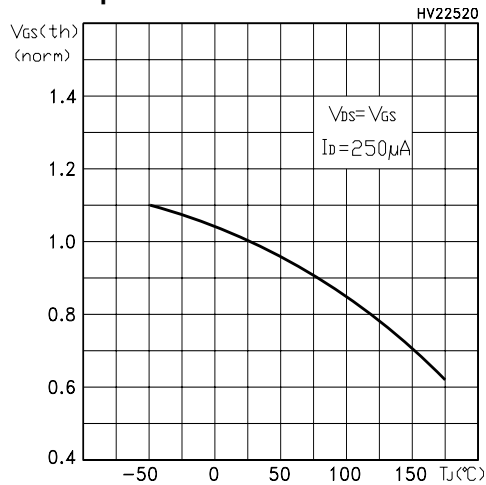


Figure 11: Dource-Drain Diode Forward Characteristics

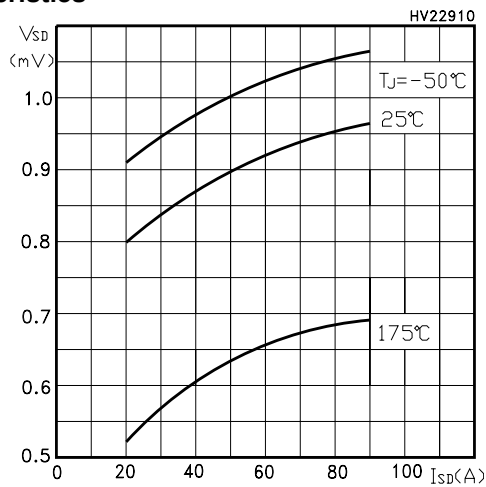


Figure 12: Capacitance Variations

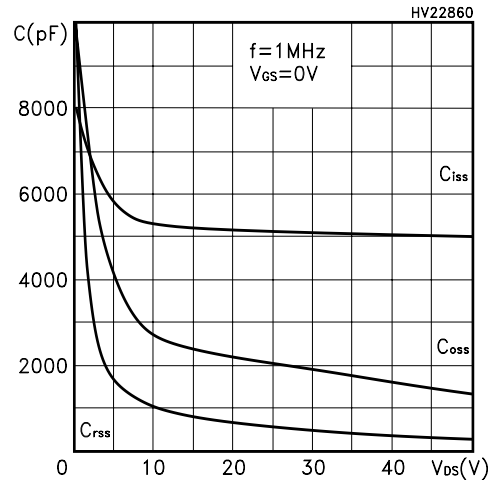


Figure 13: Normalized On Resistance vs Temperature

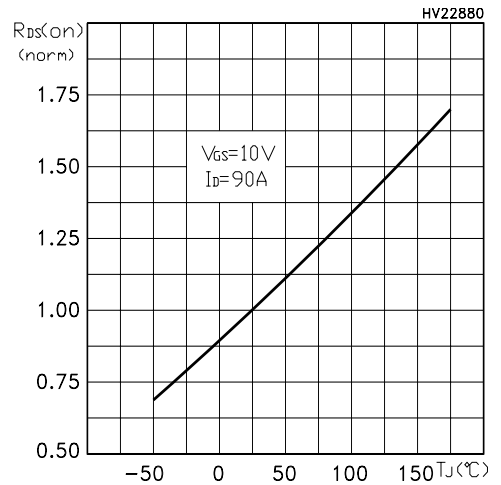


Figure 14: Normalized Breakdown Voltage vs Temperature

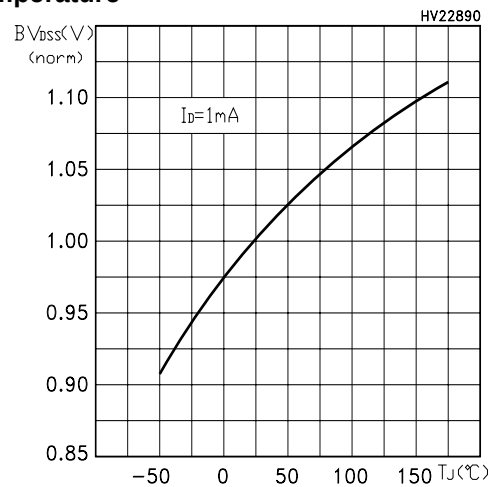


Figure 15: Thermal Resistance Rthj-a vs PCB Copper Area

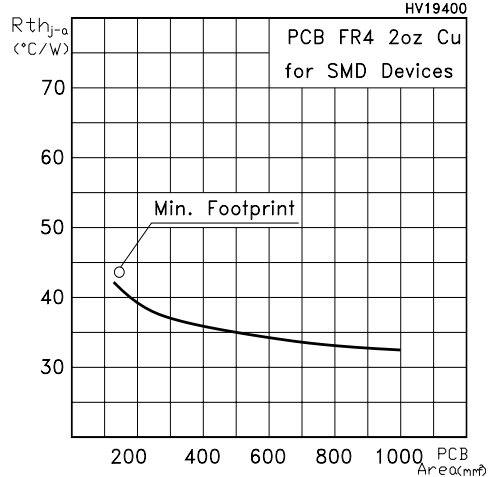


Figure 16: Max Power Dissipation vs PCB Copper Area

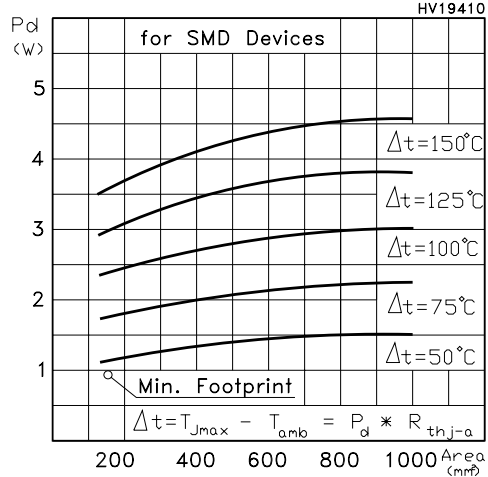
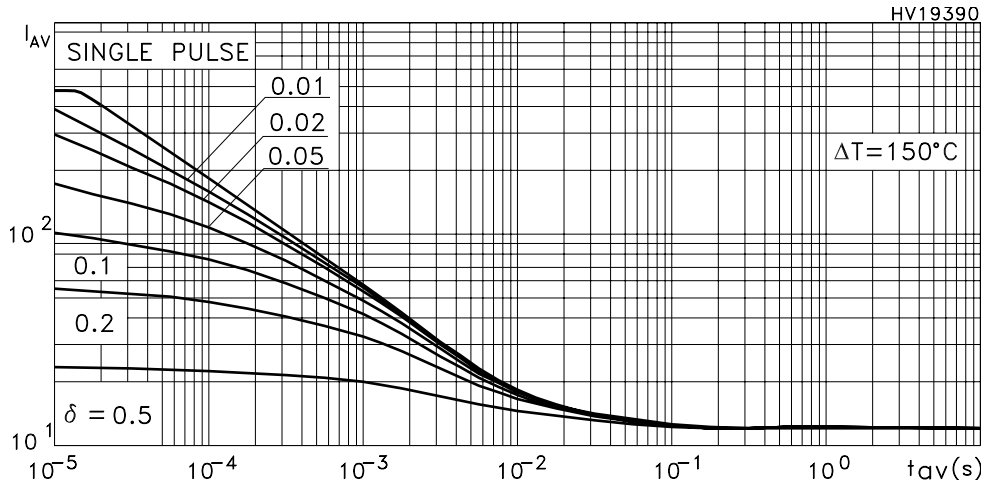


Figure 17: Allowable I_{AV} vs. Time in Avalanche



The previous curve gives the safe operating area for unclamped inductive loads, single pulse or repetitive, under the following conditions:

$$P_{D(AVE)} = 0.5 * (1.3 * BV_{DSS} * I_{AV})$$

$$E_{AS(AR)} = P_{D(AVE)} * t_{AV}$$

Where:

I_{AV} is the Allowable Current in Avalanche

$P_{D(AVE)}$ is the Average Power Dissipation in Avalanche (Single Pulse)

t_{AV} is the Time in Avalanche

To derate above 25 °C, at fixed I_{AV} , the following equation must be applied:

$$I_{AV} = 2 * (T_{jmax} - T_{CASE}) / (1.3 * BV_{DSS} * Z_{th})$$

Where:

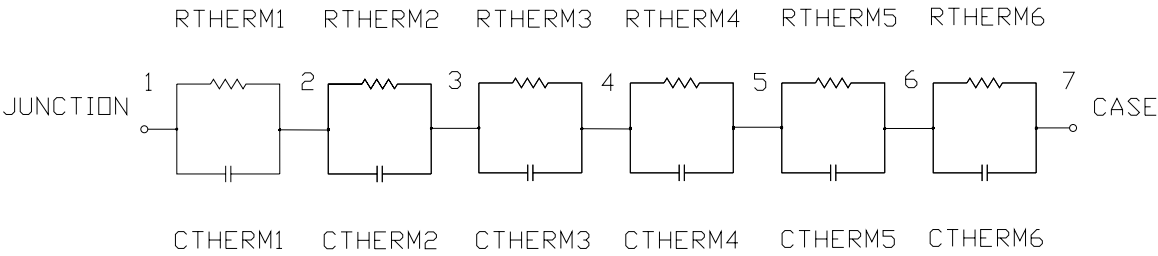
$Z_{th} = K * R_{th}$ is the value coming from Normalized Thermal Response at fixed pulse width equal to T_{AV} .

SPICE THERMAL MODEL

Table 9: 6th Order RC Network

Parameter	Node	Value
CTHERM1	1 - 2	1.4958E-3
CTHERM2	2 - 3	3.5074E-2
CTHERM3	3 - 4	5.939E-2
CTHERM4	4 - 5	9.7411E-2
CTHERM5	5 - 6	8.8596E-2
CTHERM6	6 - 7	8.2755E-1
RTHERM1	1 - 2	0.0384
RTHERM2	2 - 3	0.0624
RTHERM3	3 - 4	0.072
RTHERM4	4 - 5	0.0912
RTHERM5	5 - 6	0.1008
RTHERM6	6 - 7	0.1152

Figure 18: Schematic of 6th Order RC Network



SC16500-B

Figure 19: Unclamped Inductive Load Test Circuit

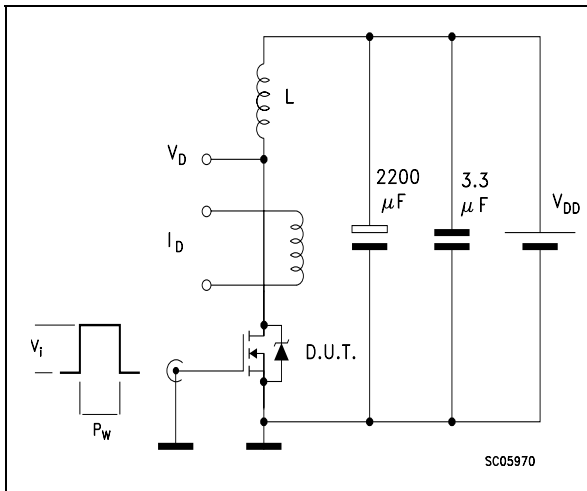


Figure 20: Switching Times Test Circuit For Resistive Load

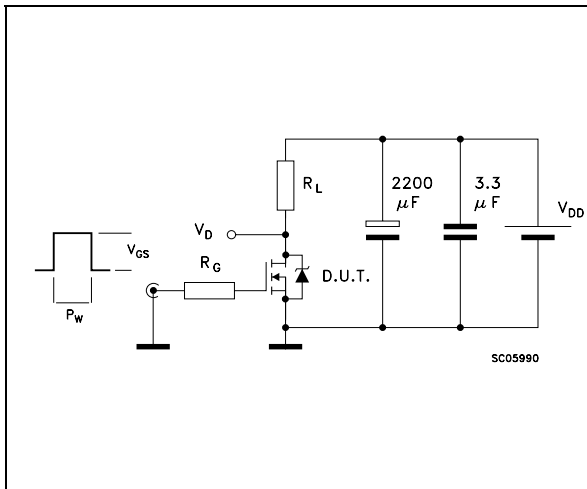


Figure 21: Test Circuit For Inductive Load Switching and Diode Recovery Times

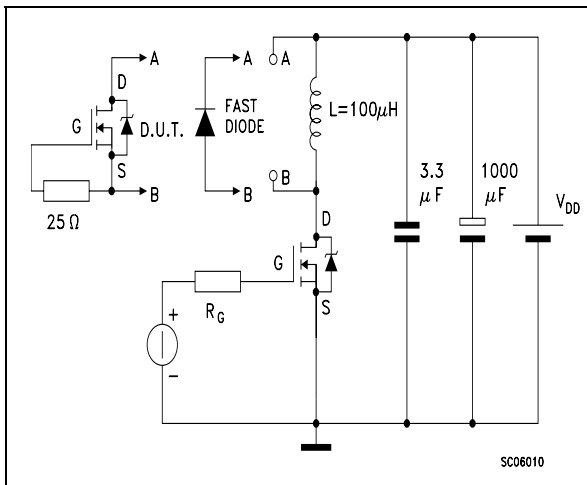


Figure 22: Unclamped Inductive Waferform

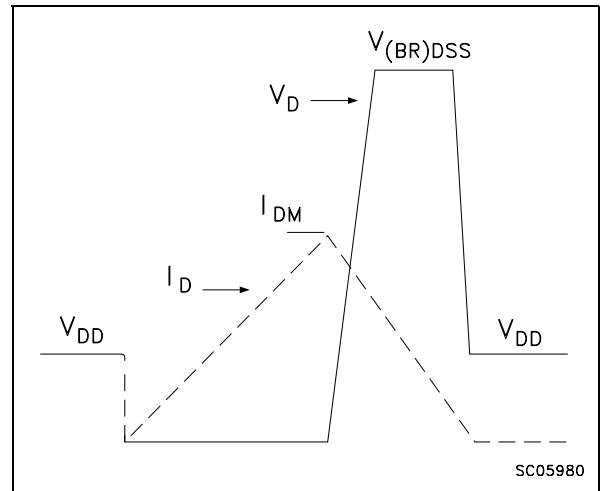
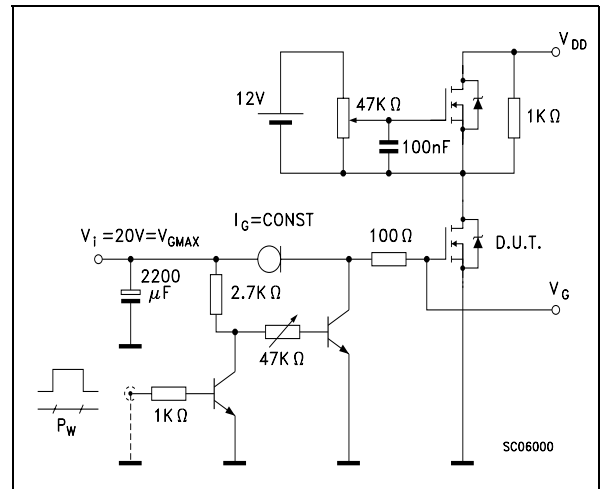
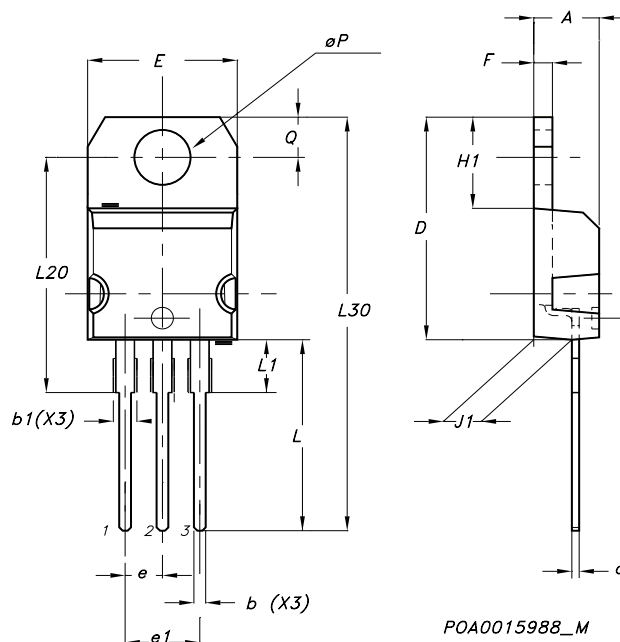


Figure 23: Gate Charge Test Circuit



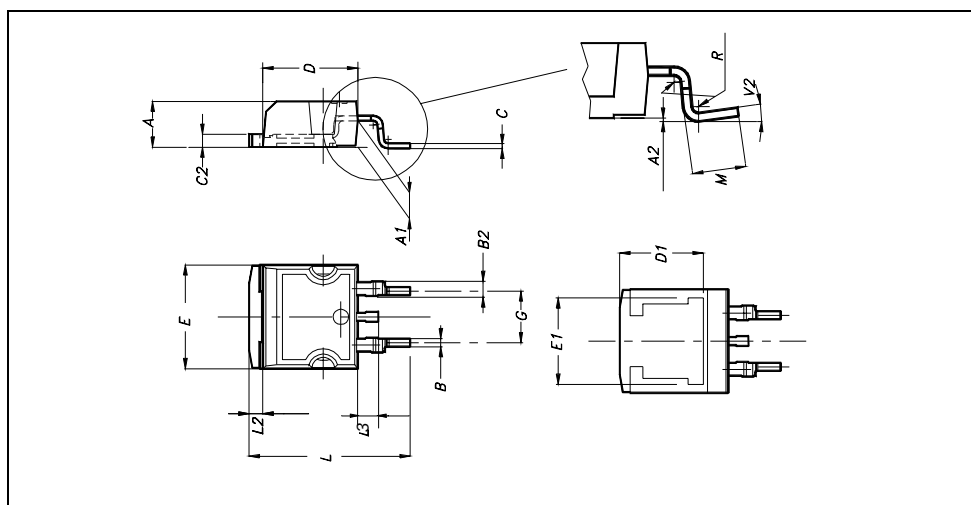
TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



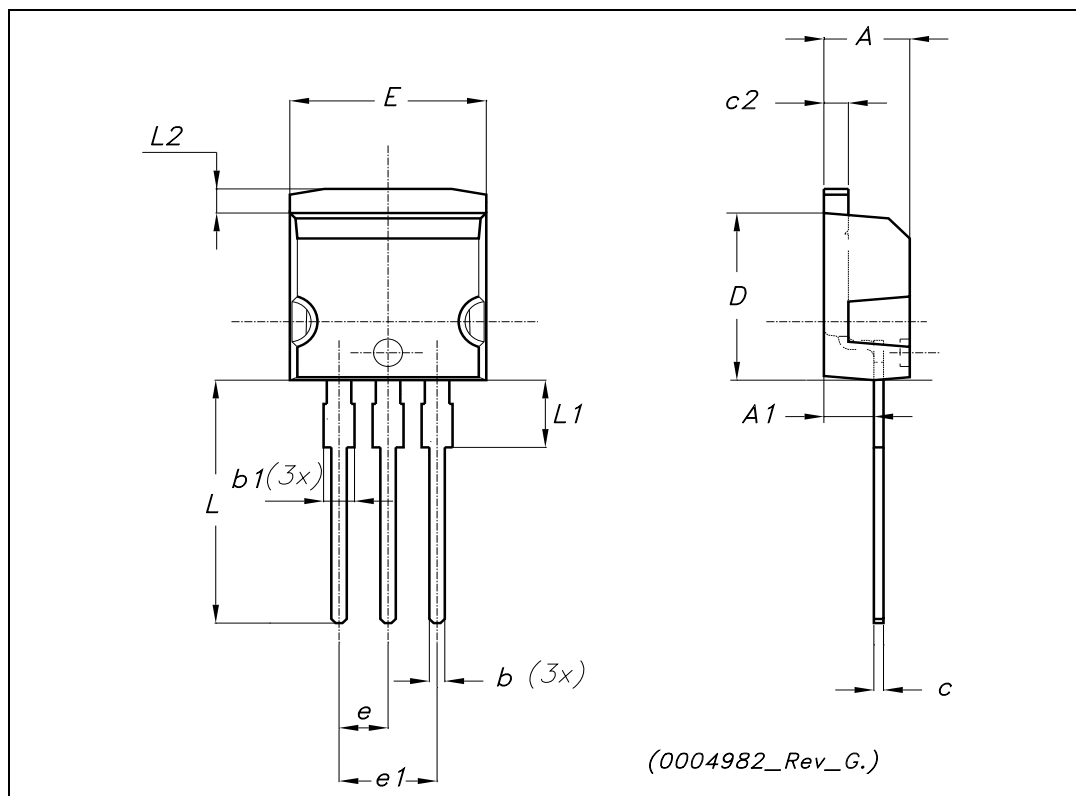
D²PAK MECHANICAL DATA

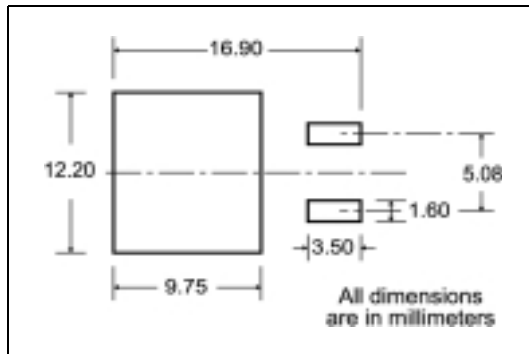
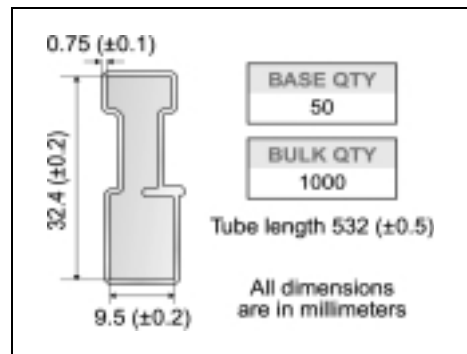
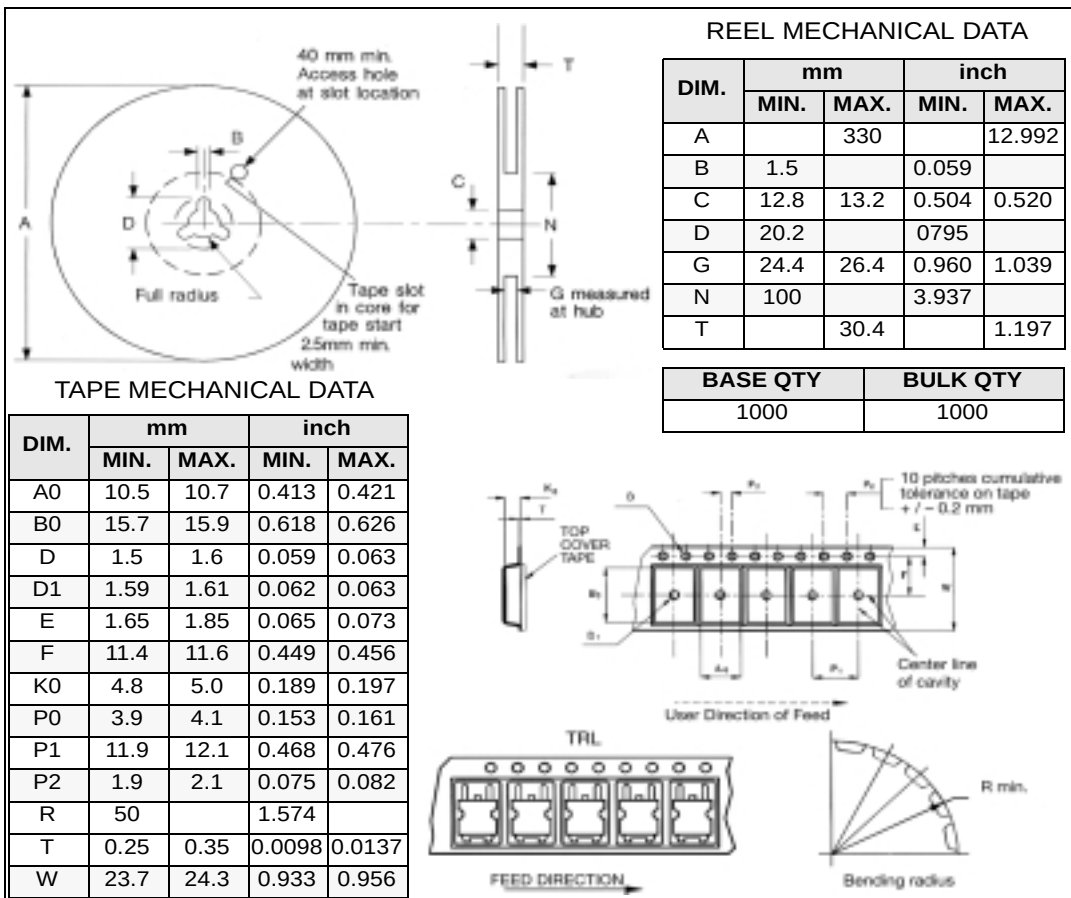
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			



TO-262 (I²PAK) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
A1	2.40		2.72	0.094		0.107
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.49		0.70	0.019		0.027
c2	1.23		1.32	0.048		0.052
D	8.95		9.35	0.352		0.368
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
E	10		10.40	0.393		0.410
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L2	1.27		1.40	0.050		0.055



D²PAK FOOTPRINT**TUBE SHIPMENT (no suffix)*****TAPE AND REEL SHIPMENT (suffix "T4")***

* on sales type

Table 10: Revision History

Date	Revision	Description of Changes
28-Sep-2004	2	New Stylesheet. No Content Change
11-Oct-2004	3	Final datasheet

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics

All other names are the property of their respective owners

© 2004 STMicroelectronics - All Rights Reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America