STD815CP40

Complementary transistor pair in a single package

Features

- Low $V_{CE(sat)}$
- Simplified circuit design
- Reduced component count
- Low spread of dynamic parameters

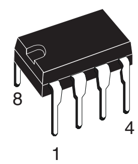
Application

- Compact fluorescent lamp (CFL) 220 V mains

Description

The STD815CP40 is a hybrid complementary pair of power bipolar transistors manufactured by using the high voltage multi-epitaxial planar technology for high switching speeds and medium voltage capability.

The STD815CP40 is housed in dual island DIP-8 package with separated terminals for higher assembly flexibility, specifically recommended to be used in a new solution for compact fluorescent lamp (CFL).



DIP-8

Figure 1. Internal schematic diagram

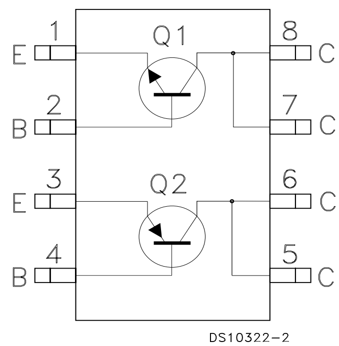


Table 1. Device summary

Order code	Marking	Package	Packing
STD815CP40	D815CP40	DIP-8	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		NPN	PNP	
V_{CBO}	Collector-base voltage (I_E = 0)	700	500	V
V_{CEO}	Collector-emitter voltage (I_B = 0)	400		V
V_{EBO}	Emitter-base voltage (I_C = 0, I_B = 0.75 A, t_p < 10 ms)	$V_{(BR)EBO}$		V
I_C	Collector current	1.5		A
I_{CM}	Collector peak current (t_P < 5 ms)	3		A
I_B	Base current	0.75		A
I_{BM}	Base peak current (t_P < 1 ms)	1.5		A
P_{TOT}	Total dissipation at T_{amb} = 25 °C single transistor	2.6		W
P_{TOT}	Total dissipation at T_{amb} = 25 °C both transistors	2		W
T_{STG}	Storage temperature	- 65 to 150		°C
T_J	Max. operating junction temperature	150		°C

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA} (1)	Thermal resistance junction-ambient (Single transistor)	48	°C/W
R_{thJA} (1)	Thermal resistance junction-ambient (Both transistors)	63	°C/W

1. When mounted on 25mm square pad of 2 oz. copper, t ≤ 10 sec.

Note: For PNP types voltage and current values are negative.

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2 Electrical characteristics

T_{case} = 25°C unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector cut-off current (V_{BE} = 0)	For NPN: V_{CE} = 700 V V_{CE} = 700 V T_C = 125°C For PNP: V_{CE} = 500 V V_{CE} = 500 V T_C = 125°C			 1 5 1 5	 mA mA mA mA
$V_{(BR)EBO}$	Emitter-base breakdown voltage (I_C = 0)	I_E = 10 mA For NPN: For PNP:	 12 5		 18 10	 V V
$V_{CEO(sus)}$ (1)	Collector-emitter sustaining voltage (I_B = 0)	I_C = 5 mA	400			V
$V_{CE(sat)}$ (1)	Collector-emitter saturation voltage	I_C = 0.5 A I_B = 0.1 A I_C = 0.35 A I_B = 50 mA			0.5 1	V V
$V_{BE(sat)}$ (1)	Base-emitter saturation voltage	I_C = 0.5 A I_B = 0.1 A			1	V
h_{FE} (1)	DC current gain	I_C = 10 mA V_{CE} = 5 V I_C = 0.35A V_{CE} = 5 V I_C = 1 A V_{CE} = 5 V	10 16 4		 34 	
 t_r t_s t_f	Resistive load Rise time Storage time Fall time	 I_C = 0.35 A V_{CC} = 125 V I_{B1} = 70 mA I_{B2} = -70 mA t_p ≥ 25 µs		 100 2.2 0.2		 ns µs µs
 t_s t_f	Inductive load Storage time Fall time	I_C = 0.5 A I_{B1} = 0.1 A $V_{BE(off)}$ = -5 V V_{clamp} = 300 V L = 10 mH		 450 80		 ns ns

1. Pulse test: pulse duration ≤ 300 µs, duty cycle ≤ 2 %.

Note: For PNP types voltage and current values are negative

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2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

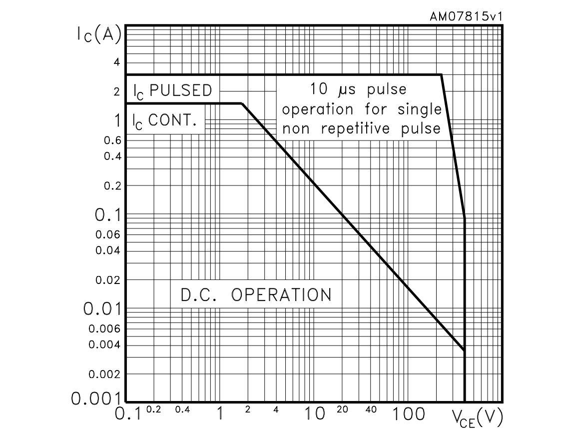

Figure 3. Derating curve

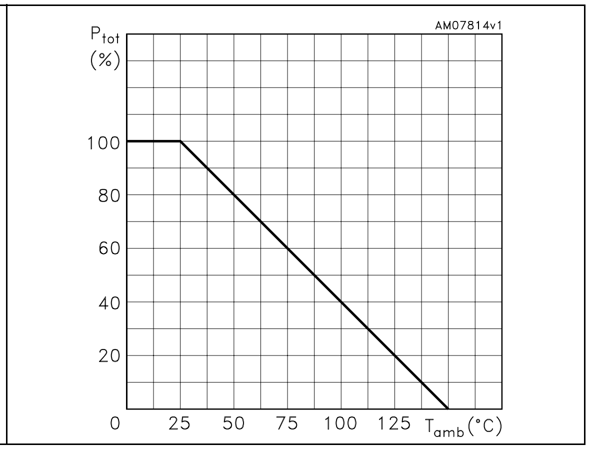

Figure 4. DC current gain NPN (V_{CE} = 5 V)

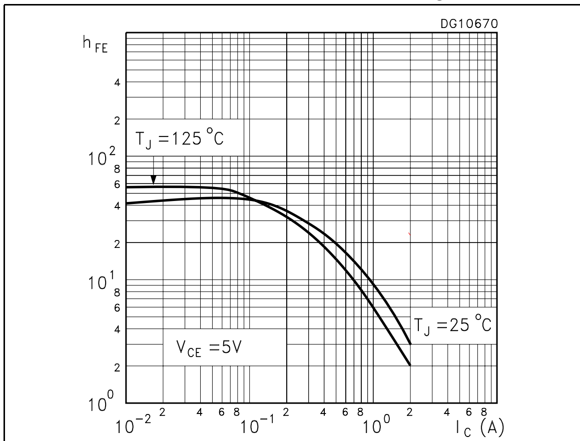

Figure 5. DC current gain PNP (V_{CE} = - 5 V)

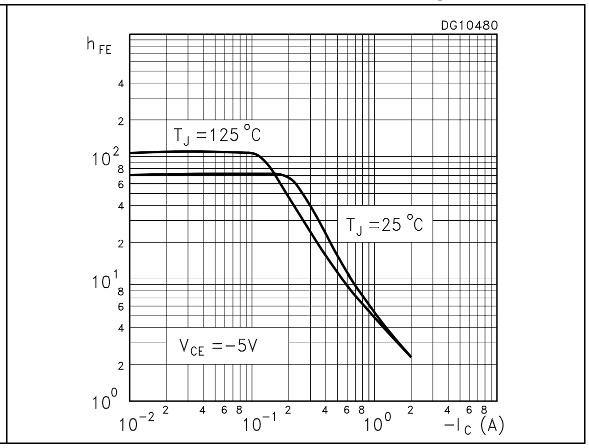

Figure 6. DC current gain NPN (V_{CE} = 1 V)

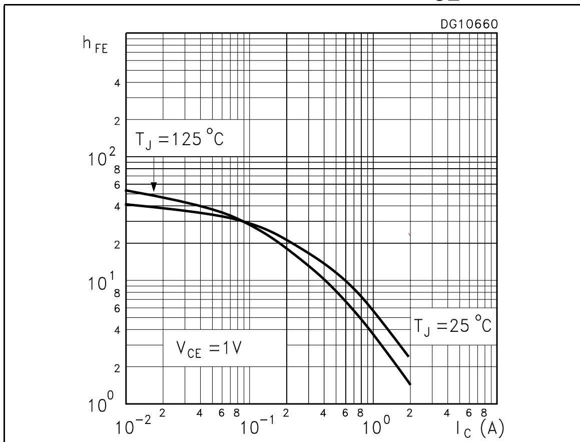

Figure 7. DC current gain PNP (V_{CE} = - 1 V)

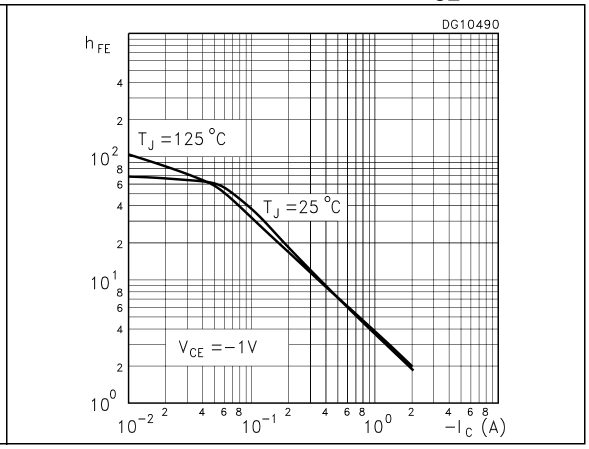

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Figure 8. Collector emitter saturation voltage NPN

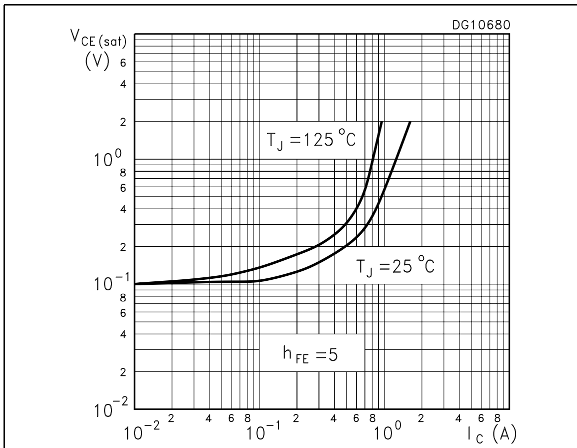

Figure 9. Collector emitter saturation voltage PNP

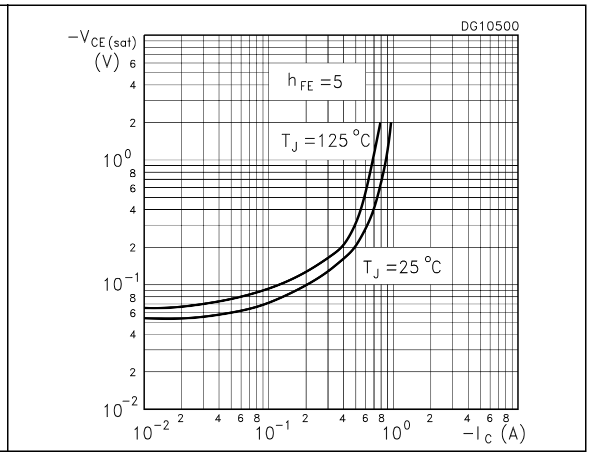

Figure 10. Base emitter saturation voltage NPN

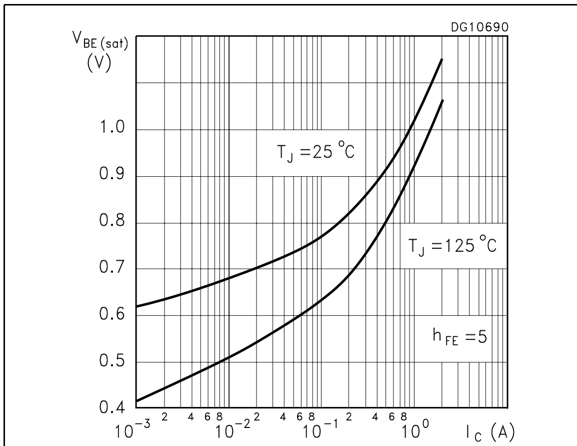

Figure 11. Base emitter saturation voltage PNP

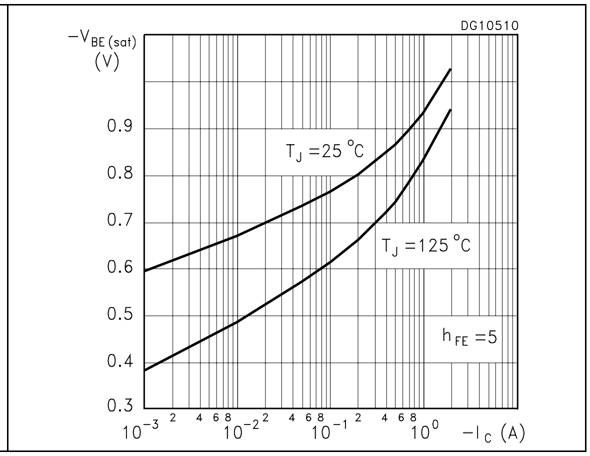

Figure 12. Resistive load fall time NPN

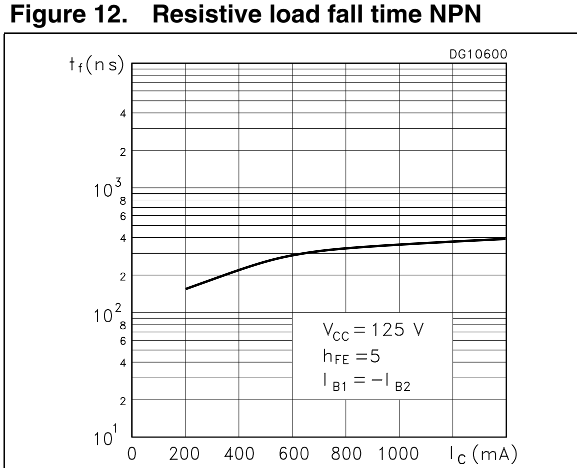

Figure 13. Resistive load fall time PNP

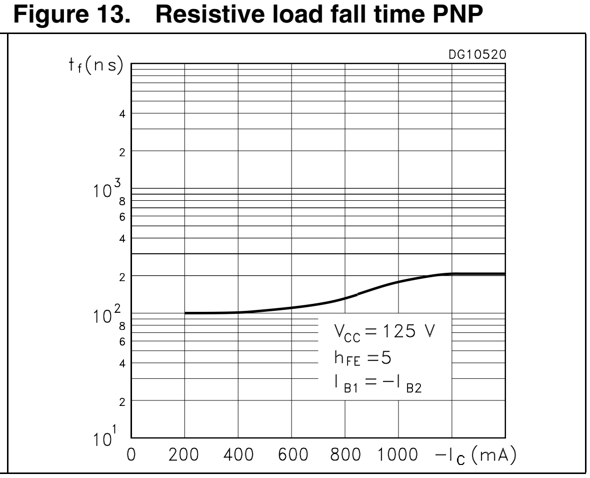

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Figure 14. Resistive load storage time NPN

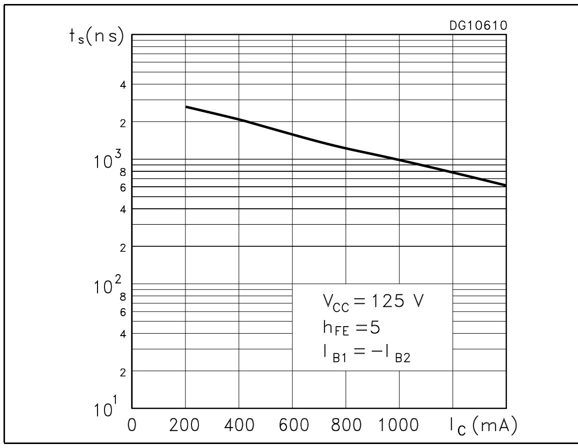

Figure 15. Resistive load storage time PNP

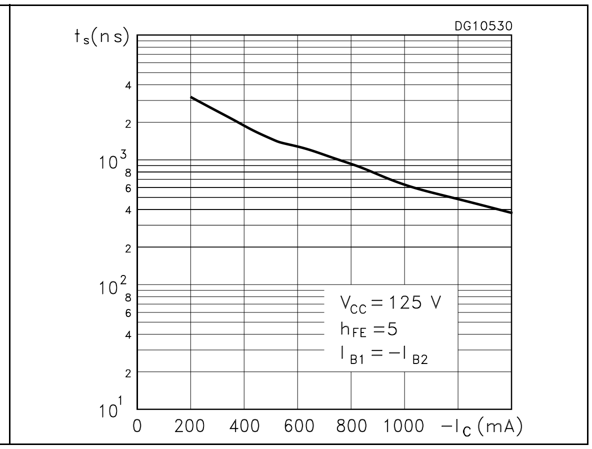

Figure 16. Inductive load fall time NPN

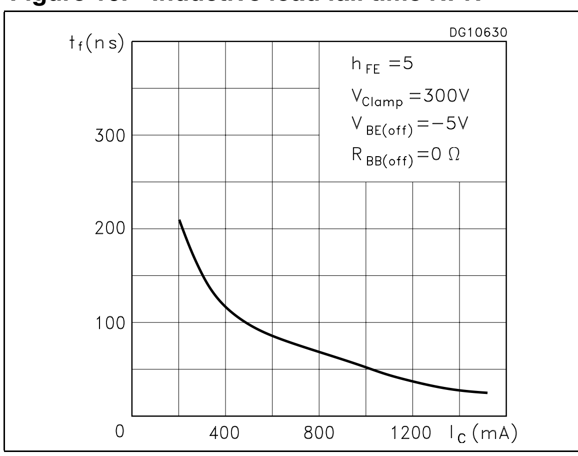

Figure 17. Inductive load fall time PNP

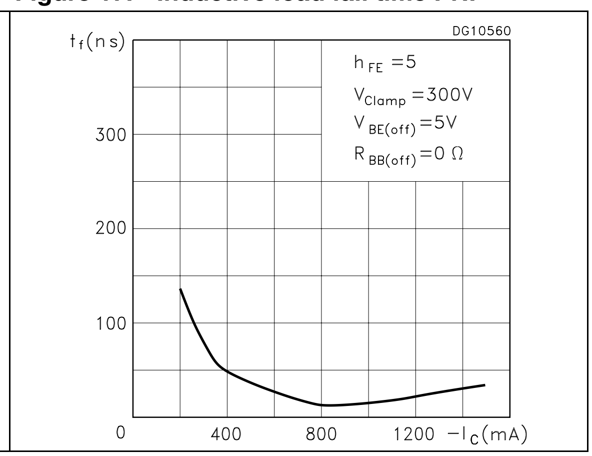

Figure 18. Inductive load storage time NPN

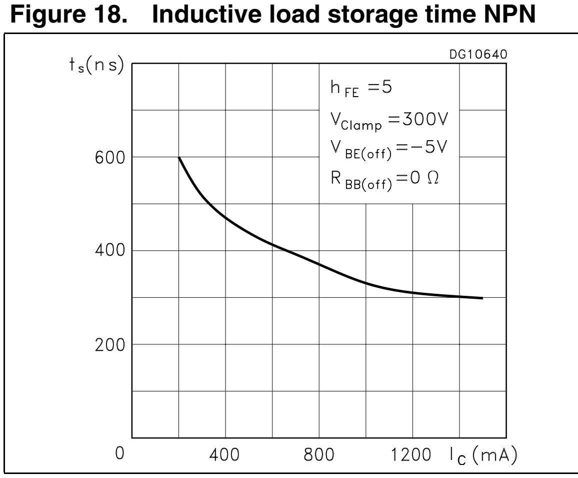

Figure 19. Inductive load storage time PNP

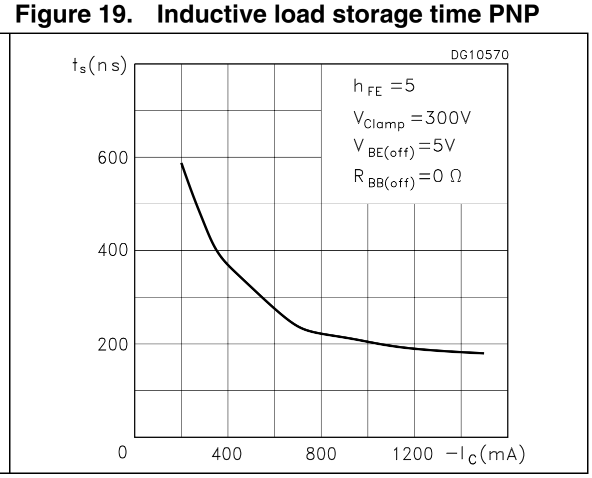

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Figure 20. Reverse biased SOA (NPN)

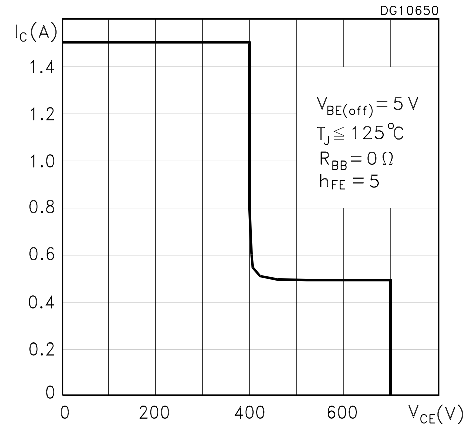
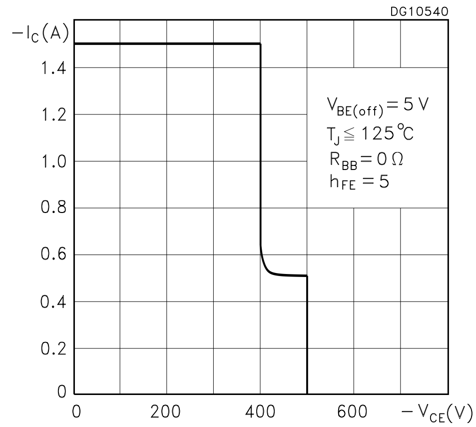


Figure 21. Reverse biased SOA (PNP)



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3 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 5. DIP-8 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A			4.80
A1	0.50		
A2	3.10		3.50
A3	1.40		1.60
b	0.38		0.55
b1	0.38		0.51
b2	1.47		1.57
b3	0.89		1.09
c	0.21		0.35
c1	0.20		0.30
D	9.10		9.30
D1	0.13		
E	7.62		8.25
E1	6.25		6.45
e		2.54	
eA		7.62	
eB	7.62		10.90
eC	0		1.52
L	2.92		3.81

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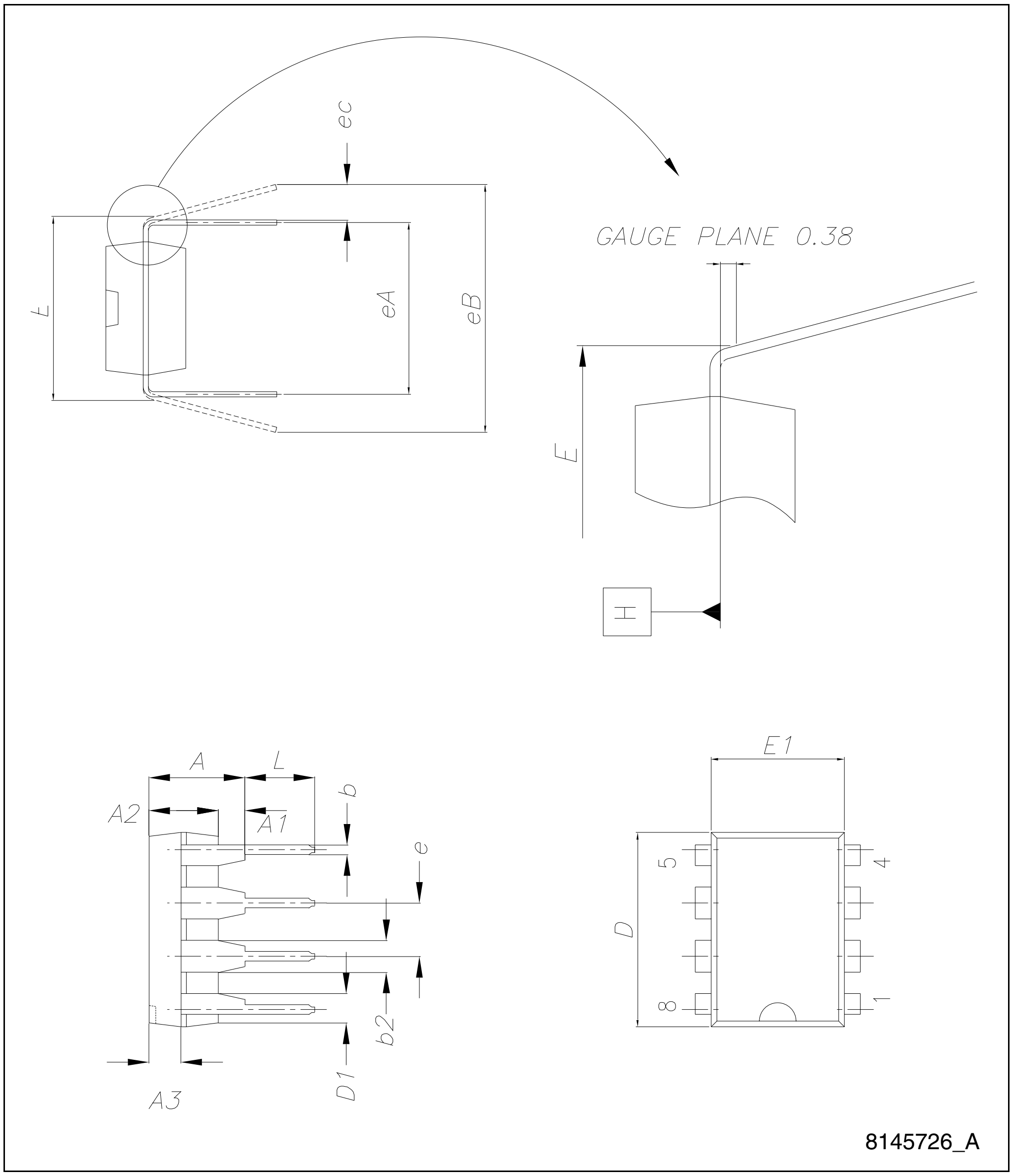
Figure 22. Drawing dimension DIP-8



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4 Revision history

Table 6. Document revision history

Date	Revision	Changes
20-Jun-2008	1	Initial release
26-May-2009	2	Updated mechanical data *Table 5 on page 8* and *Figure 22 on page 9*.
29-Jun-2010	3	Modified: *Table 2* and *Table 3 on page 2*, added *Section 2.1: Electrical characteristics (curves)*.

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