



# STFI13NK60Z

N-channel 600 V, 0.48  $\Omega$ , 13 A, Zener-protected SuperMESH™ Power MOSFET in I<sup>2</sup>PakFP

Preliminary data

## Features

Order code	V <sub>DSS</sub>	R <sub>DS(on) max</sub>	I <sub>D</sub>	P <sub>TOT</sub>
STFI13NK60Z	600 V	<0.55 $\Omega$	13 A	35 W

- Fully insulated and low profile package with increased creepage path from pin to heatsink plate
- Gate charge minimized
- Very low intrinsic capacitance

## Applications

- Switching applications

## Description

This device is an N-channel Zener-protected Power MOSFET developed using STMicroelectronics' SuperMESH™ technology, achieved through optimization of ST's well established strip-based PowerMESH™ layout. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

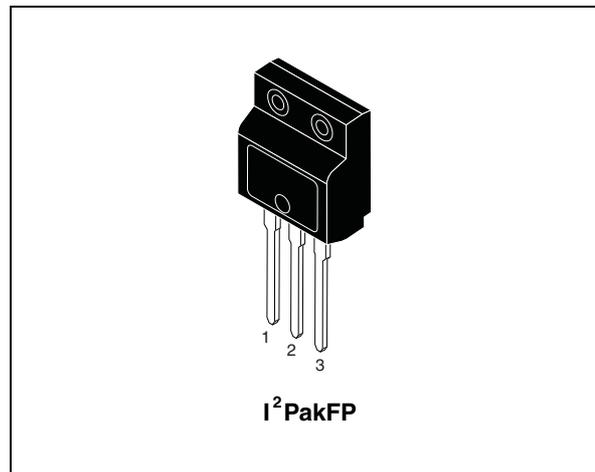


Figure 1. Internal schematic diagram

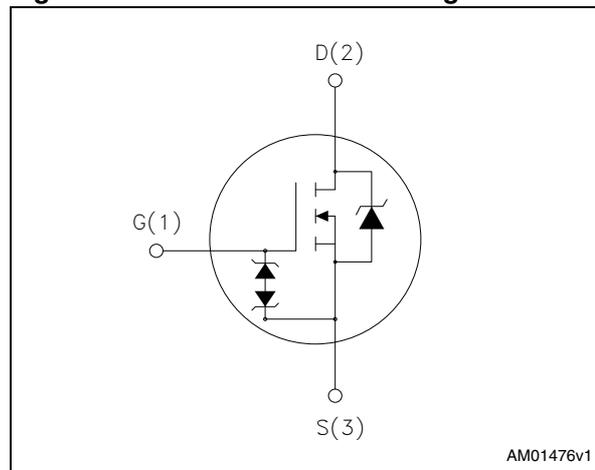


Table 1. Device summary

Order code	Marking	Package	Packaging
STFI13NK60Z	13NK60Z	I <sup>2</sup> PakFP	Tube

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	600	V
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	13 <sup>(1)</sup>	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	8.2 <sup>(1)</sup>	A
$I_{DM}^{(2)}$	Drain current (pulsed)	52 <sup>(1)</sup>	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	35	W
ESD	Gate-source human body model (R=1,5 k $\Omega$ , C=100 pF)	4	kV
dv/dt <sup>(3)</sup>	Peak diode recovery voltage slope	4.5	V/ns
$V_{ISO}$	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; $T_C=25\text{ }^\circ\text{C}$ )	2500	V
$T_j$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. Limited by maximum junction temperature.
2. Pulse width limited by safe operating area.
3.  $I_{SD} < 13\text{ A}$ ,  $di/dt < 200\text{ A}/\mu\text{s}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$ .

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case Max	3.6	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-amb Max	62.5	$^\circ\text{C}/\text{W}$

**Table 4. Avalanche characteristics**

Symbol	Parameter	Max value	Unit
$I_{AR}$	Repetitive or non repetitive avalanche current	10 <sup>(1)</sup>	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j=25\text{ }^\circ\text{C}$ , $I_D=I_{AR}$ , $V_{DD}=50\text{ V}$ )	400	mJ

1. Limited by maximum junction temperature

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified).

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ( $V_{GS} = 0$ )	$I_D = 1\text{ mA}$	600			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 600\text{ V}$ , $V_{DS} = 600\text{ V}$ , $T_c = 125\text{ °C}$			1 50	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 100\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ , $I_D = 4.5\text{ A}$		0.48	0.55	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 8\text{ V}$ , $I_D = 5\text{ A}$	-	11		S
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	2030		pF
$C_{oss}$	Output capacitance			210		pF
$C_{rss}$	Reverse transfer capacitance			48		pF
$C_{oss\text{ eq.}}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0$ , $V_{DS} = 0\text{ to }480\text{ V}$	-	125		pF
$Q_g$	Total gate charge	$V_{DD} = 480\text{ V}$ , $I_D = 10\text{ A}$	-	66	92	nC
$Q_{gs}$	Gate-source charge	$V_{GS} = 10\text{ V}$		11		nC
$Q_{gd}$	Gate-drain charge	(see <a href="#">Figure 16</a> )		33		nC

1. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

2.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on delay time Rise time	$V_{DD}=300\text{ V}$ , $I_D=5\text{ A}$ , $R_G=4.7\ \Omega$ , $V_{GS}=10\text{ V}$ (see <a href="#">Figure 15</a> )	-	22 14	-	ns ns
$t_{d(off)}$ $t_f$	Turn-off delay time Fall time	$V_{DD}=300\text{ V}$ , $I_D=5\text{ A}$ , $R_G=4.7\ \Omega$ , $V_{GS}=10\text{ V}$ (see <a href="#">Figure 15</a> )	-	61 12	-	ns ns
$t_{r(Voff)}$ $t_f$ $t_c$	Off-voltage rise time Fall time Cross-over time	$V_{DD}=480\text{ V}$ , $I_D=10\text{ A}$ , $R_G=4.7\ \Omega$ , $V_{GS}=10\text{ V}$ (see <a href="#">Figure 15</a> )	-	10 9 20	-	ns ns ns

**Table 8. Gate-source Zener diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage ( $I_D=0$ )	$I_{gs}=\pm 1\text{ mA}$	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

**Table 9. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)		-		10 40	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=10\text{ A}$ , $V_{GS}=0$	-		1.6	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=10\text{ A}$ , $di/dt=100\text{ A}/\mu\text{s}$ , $V_{DD}=35\text{ V}$ , $T_J=150\text{ }^\circ\text{C}$	-	570 4.5 16		ns $\mu\text{C}$ A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

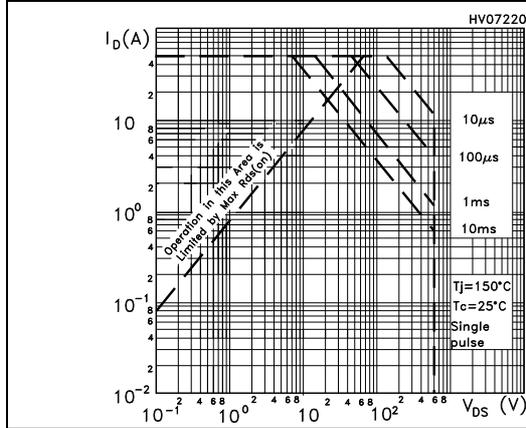


Figure 3. Thermal impedance

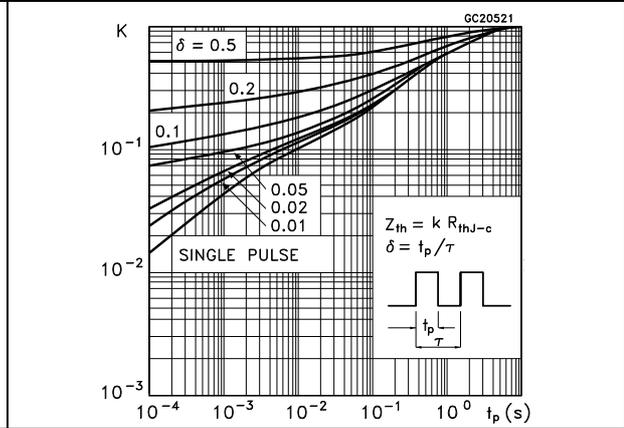


Figure 4. Output characteristics

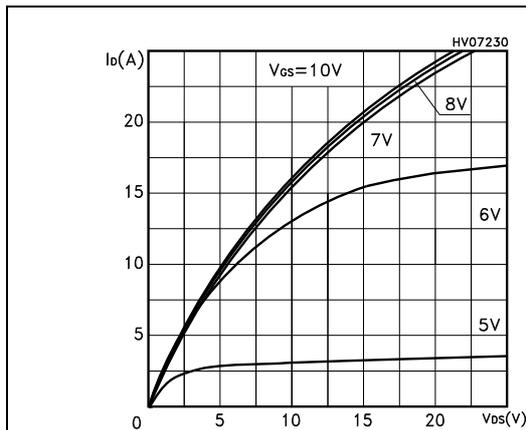


Figure 5. Transfer characteristics

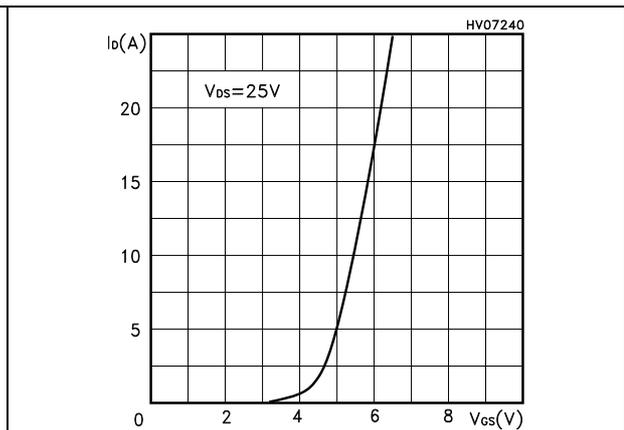


Figure 6. Transconductance

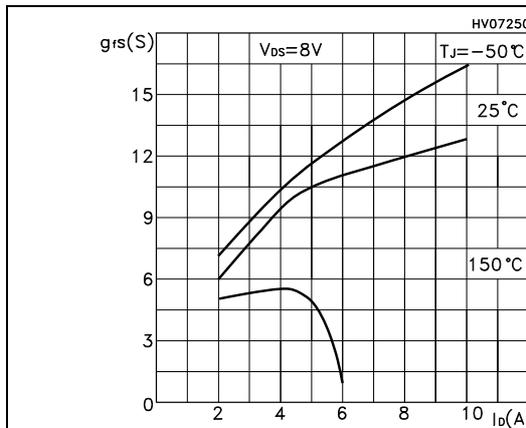


Figure 7. Static drain-source on resistance

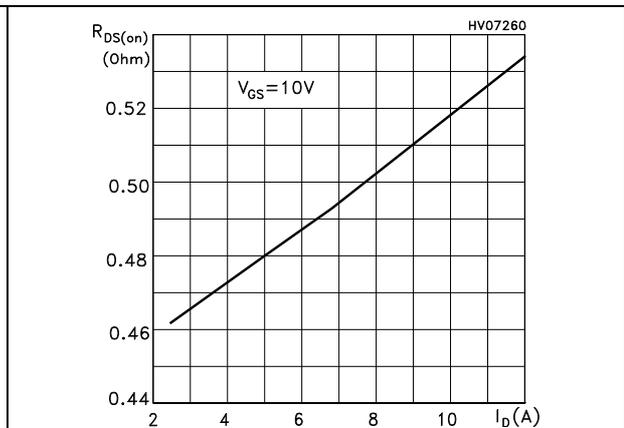


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

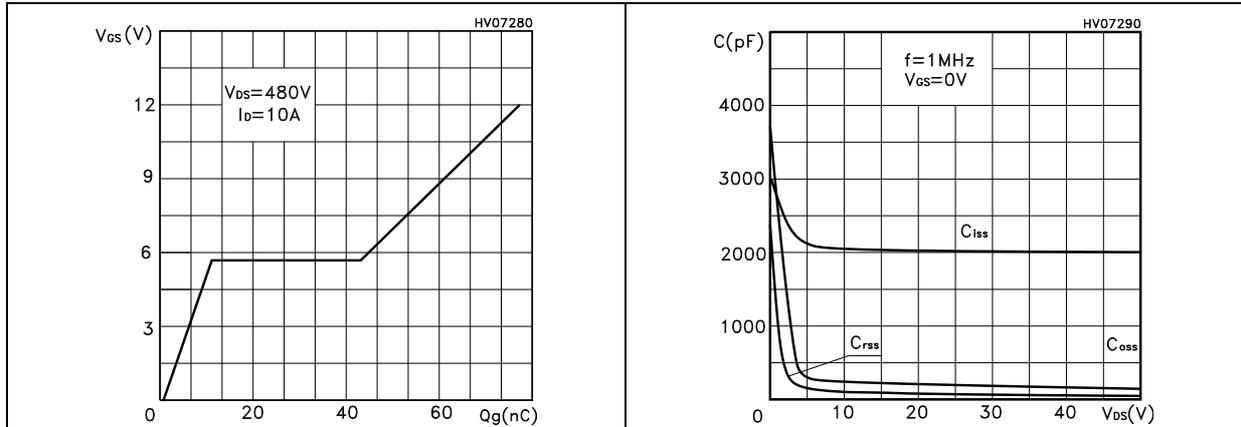


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

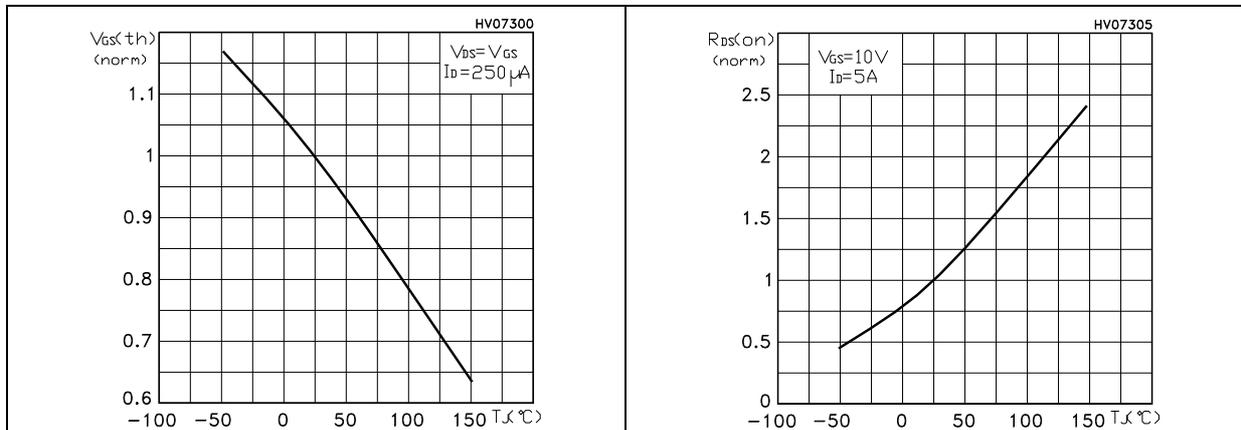


Figure 12. Source-drain diode forward characteristics Figure 13. Normalized  $B_{V_{DS}}$  vs temperature

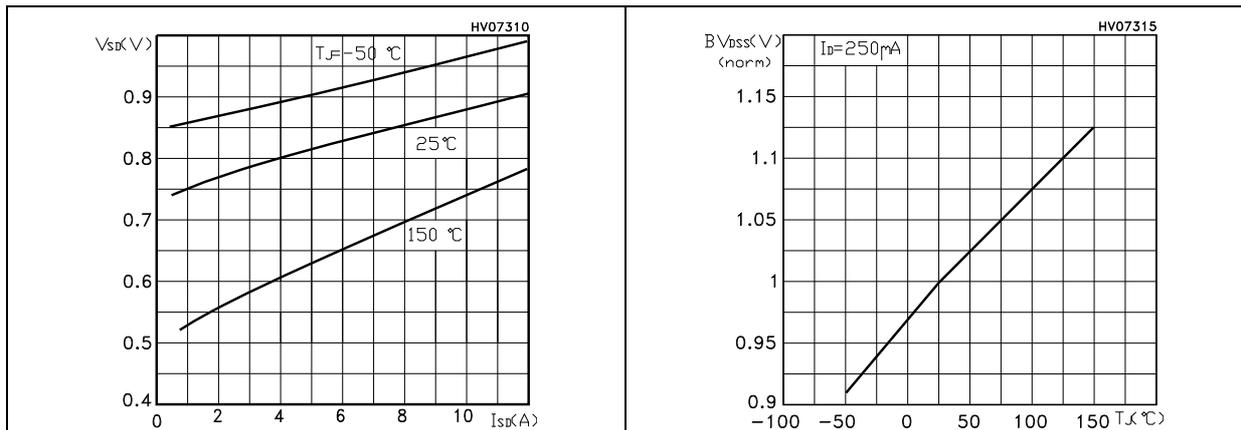
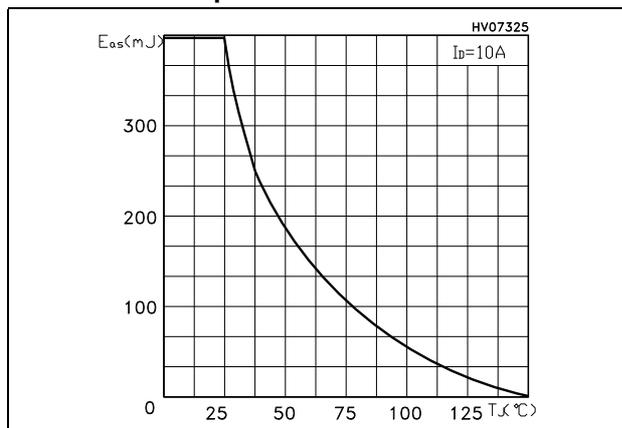
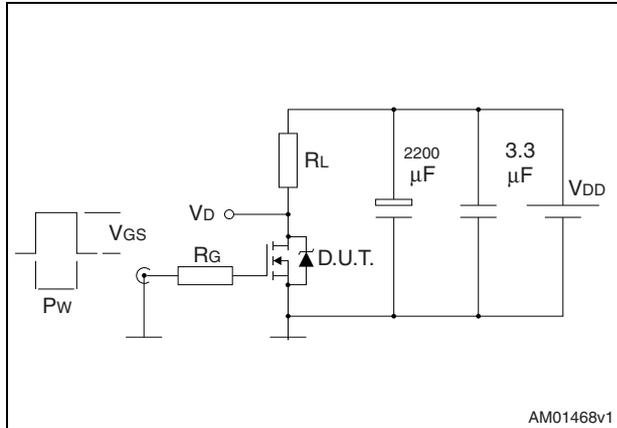


Figure 14. Maximum avalanche energy vs temperature

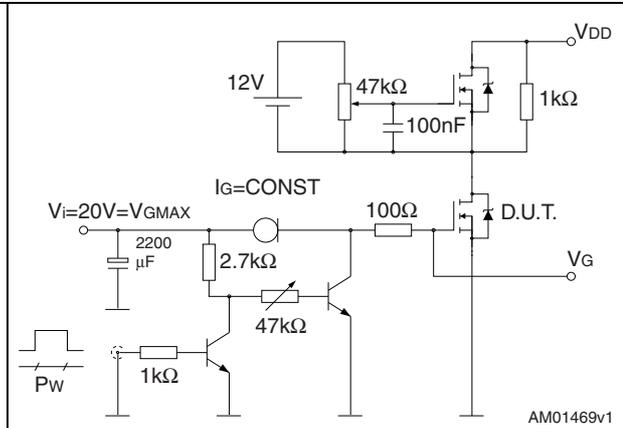


### 3 Test circuits

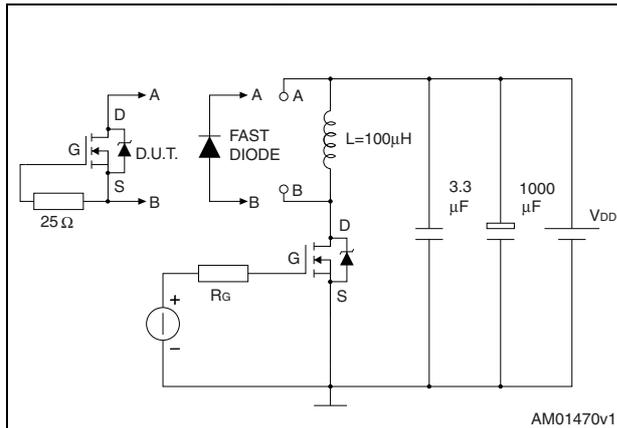
**Figure 15. Switching times test circuit for resistive load**



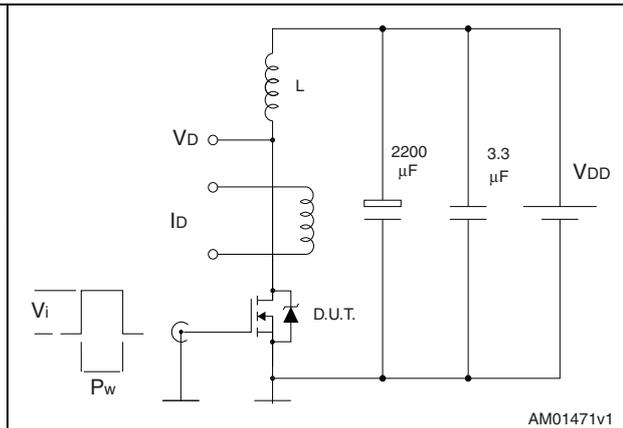
**Figure 16. Gate charge test circuit**



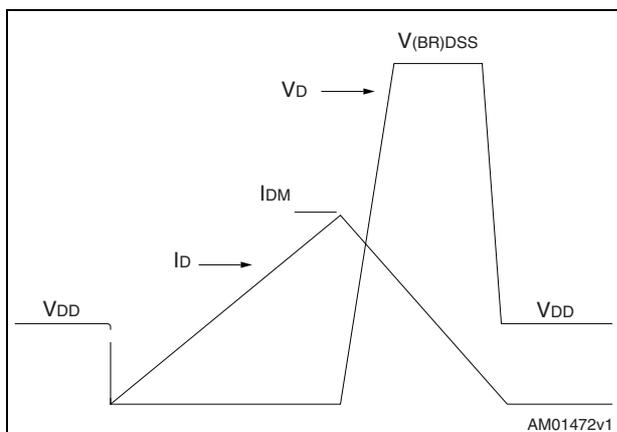
**Figure 17. Test circuit for inductive load switching and diode recovery times**



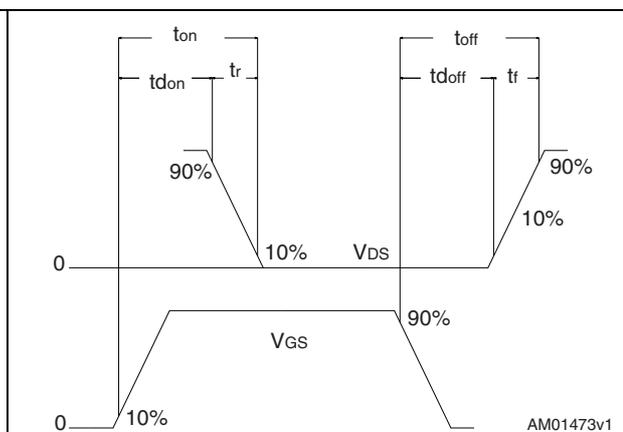
**Figure 18. Unclamped inductive load test circuit**



**Figure 19. Unclamped inductive waveform**



**Figure 20. Switching time waveform**



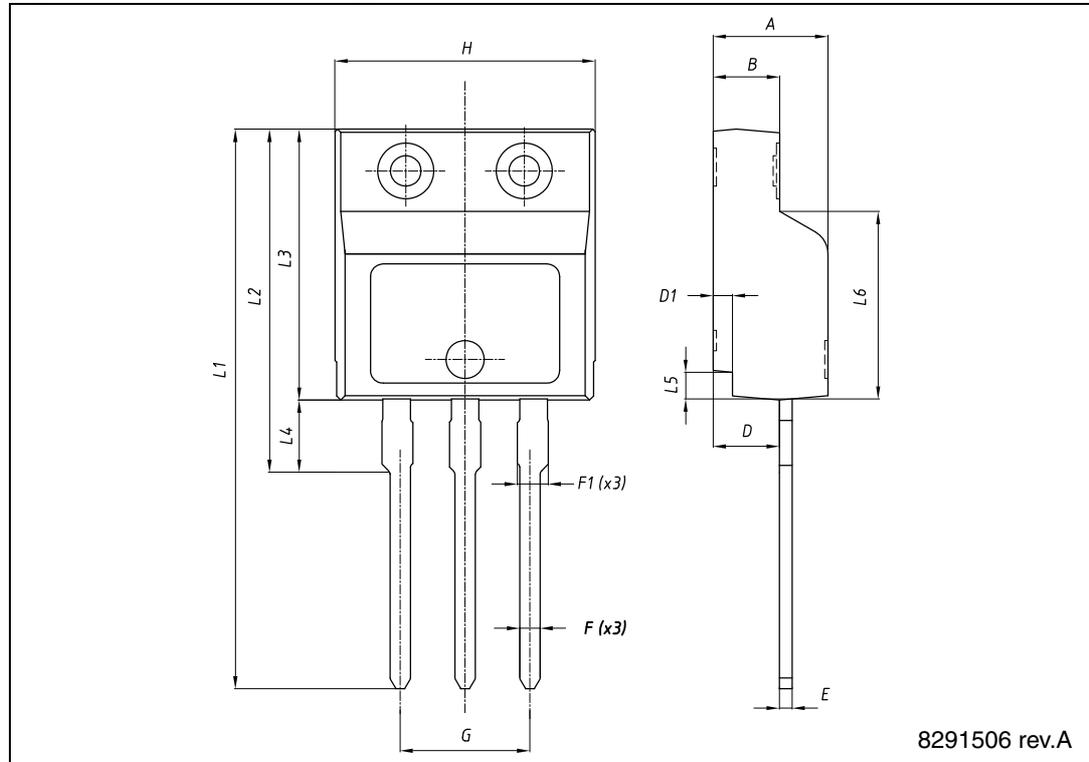
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Table 10. I<sup>2</sup>PakFP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95	-	5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.30		7.50

Figure 21. I<sup>2</sup>PakFP drawing



## 5 Revision history

Table 11. Document revision history

Date	Revision	Changes
06-Jul-2011	1	First release.
07-Nov-2011	2	<i>Figure 2: Safe operating area</i> and <i>Figure 3: Thermal impedance</i> have been added.

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