



# STFI13NM60N

N-channel 600 V, 0.28  $\Omega$ , 11 A MDmesh™ II Power MOSFET  
in I<sup>2</sup>PakFP

Preliminary data

## Features

Type	V <sub>DSS</sub> (@T <sub>jmax</sub> )	R <sub>DS(on)</sub> max	I <sub>D</sub>	P <sub>TOT</sub>
STFI13NM60N	650 V	< 0.36 $\Omega$	11 A	25 W

- Fully insulated and low profile package with increased creepage path from pin to heatsink plate
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

## Applications

- Switching applications

## Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

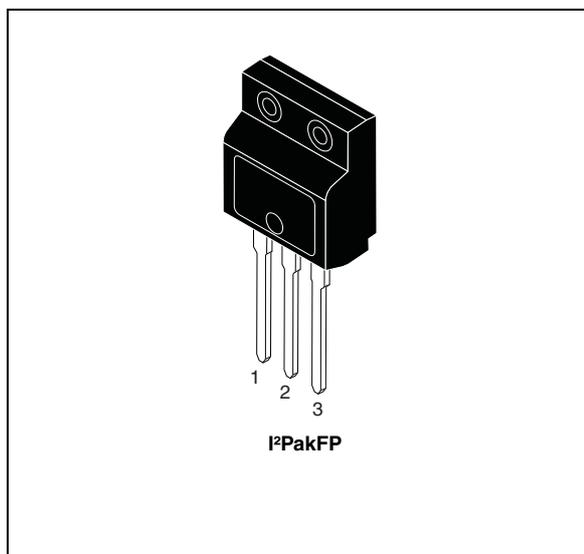
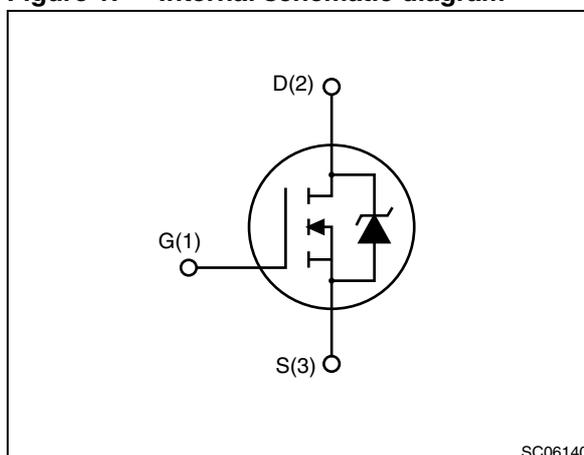


Figure 1. Internal schematic diagram



SC06140

Table 1. Device summary

Order codes	Marking	Packages	Packaging
STFI13NM60N	13NM60N	I <sup>2</sup> PakFP	Tube

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	600	V
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	11 <sup>(1)</sup>	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	6.93 <sup>(1)</sup>	A
$I_{DM}^{(2)}$	Drain current (pulsed)	44 <sup>(1)</sup>	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	25	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope	15	V/ns
$V_{ISO}$	Insulation withstand voltage (RMS) from all three leads to external heat sink ( $t=1\text{ s}; T_C=25\text{ }^\circ\text{C}$ )	2500	V
$T_{stg}$	Storage temperature	- 55 to 150	$^\circ\text{C}$
$T_j$	Max. operating junction temperature	150	$^\circ\text{C}$

1. Limited by maximum junction temperature.
2. Pulse width limited by safe operating area.
3.  $I_{SD} \leq 11\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DSpeak} \leq V_{(BR)DSS}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	5	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	$^\circ\text{C}/\text{W}$

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AS}$	Repetitive or non repetitive avalanche current	3.5 <sup>(1)</sup>	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J=25\text{ }^\circ\text{C}$ , $I_D=I_{AS}$ , $V_{DD}=50\text{ V}$ )	200	mJ

1. Limited by maximum junction temperature.

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified).

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ( $V_{GS} = 0$ )	$I_D = 1\text{ mA}$	600			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 600\text{ V}$ $V_{DS} = 600\text{ V}, T_c = 125\text{ °C}$			1 100	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 25\text{ V}$			$\pm 0.1$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}, I_D = 5.5\text{ A}$		0.28	0.36	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 50\text{ V}, f = 1\text{ MHz},$ $V_{GS} = 0$	-	790	-	$\text{pF}$
$C_{oss}$	Output capacitance			60		$\text{pF}$
$C_{rss}$	Reverse transfer capacitance			3.6		$\text{pF}$
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0, V_{DS} = 0\text{ to }480\text{ V}$	-	135	-	$\text{pF}$
$Q_g$	Total gate charge	$V_{DD} = 480\text{ V}, I_D = 11\text{ A},$ $V_{GS} = 10\text{ V},$ (see <a href="#">Figure 14</a> )	-	30	-	$\text{nC}$
$Q_{gs}$	Gate-source charge			4		$\text{nC}$
$Q_{gd}$	Gate-drain charge			15		$\text{nC}$
$R_G$	Gate input resistance	$f = 1\text{ MHz}, I_D = 0$	-	4.7	-	$\Omega$

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DS}$

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}, I_D = 5.5\text{ A}$ $R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ (see <a href="#">Figure 13</a> )	-	3	-	$\text{ns}$
$t_r$	Rise time			8		$\text{ns}$
$t_{d(off)}$	Turn-off delay time			30		$\text{ns}$
$t_f$	Fall time			10		$\text{ns}$

**Table 8. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current		-		11	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		44	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 11\text{ A}, V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 9\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	-	230		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 100\text{ V}$	-	2		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see <a href="#">Figure 15</a> )	-	18		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 9\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	-	290		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 100\text{ V}, T_j = 150\text{ }^\circ\text{C}$	-	190		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see <a href="#">Figure 15</a> )	-	17		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

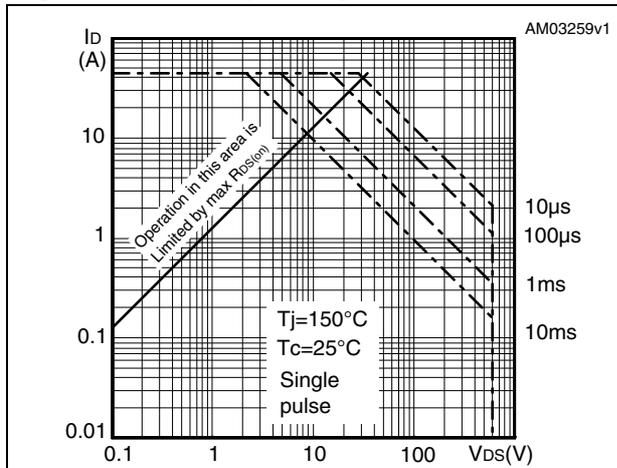


Figure 3. Thermal impedance

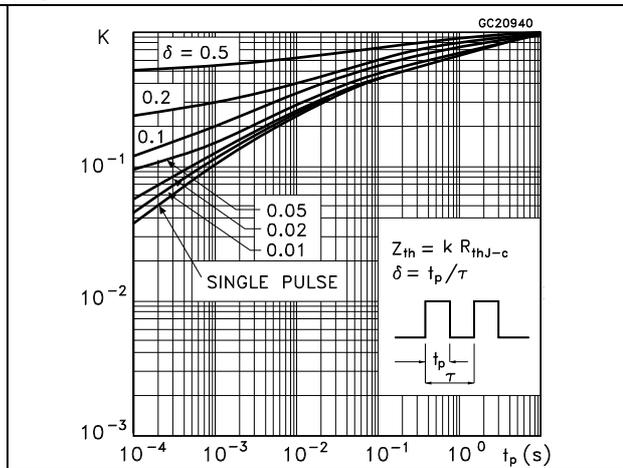


Figure 4. Output characteristics

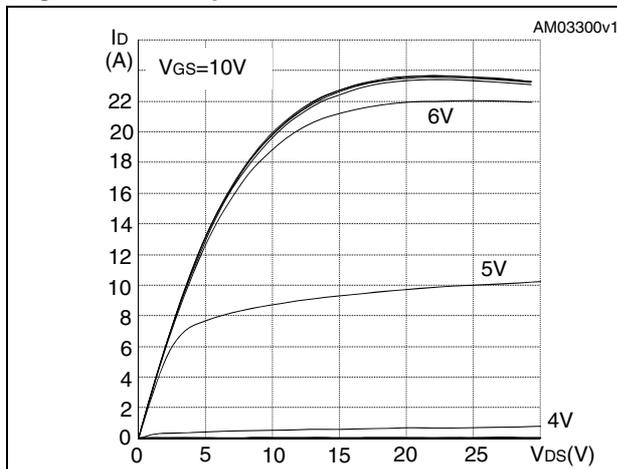


Figure 5. Transfer characteristics

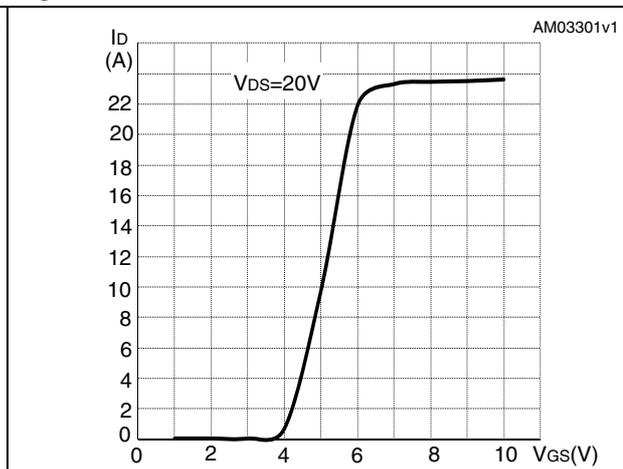


Figure 6. Normalized  $V_{DS}$  vs temperature

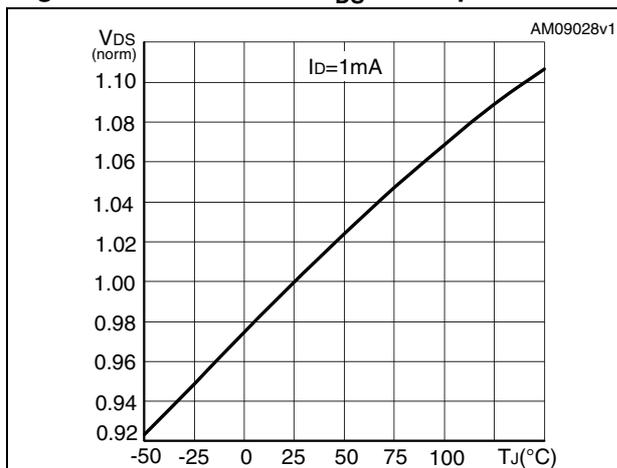


Figure 7. Static drain-source on resistance

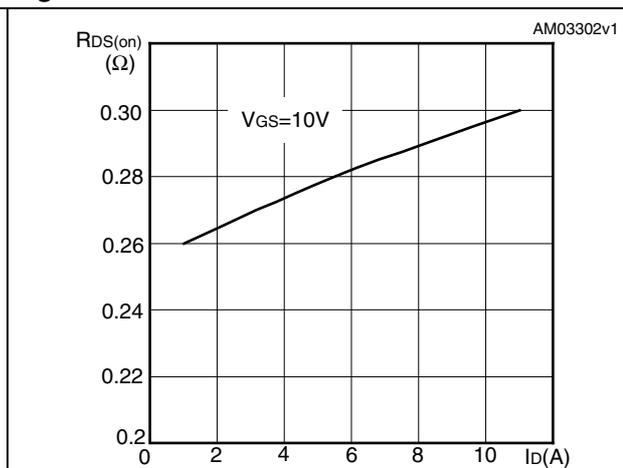


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

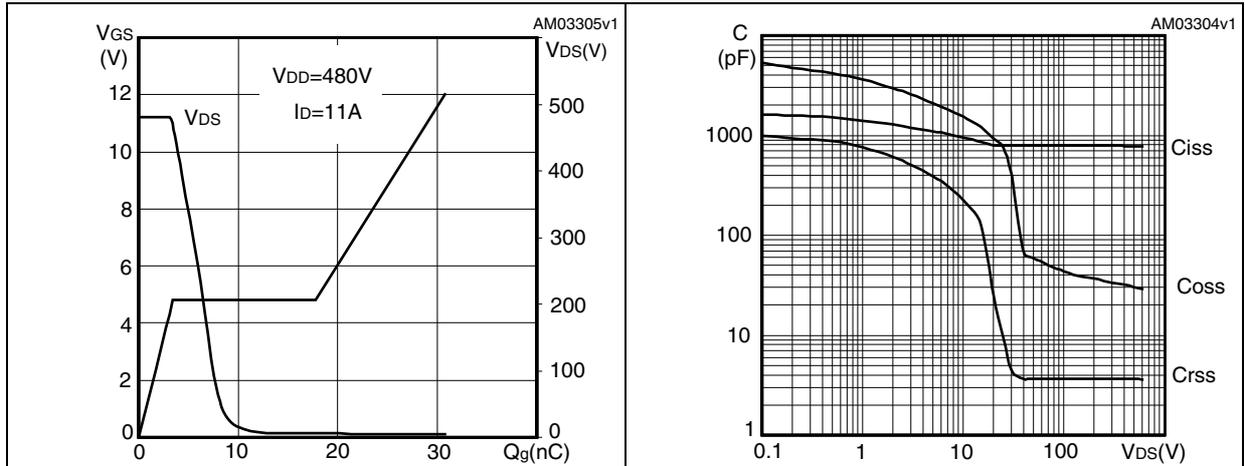


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

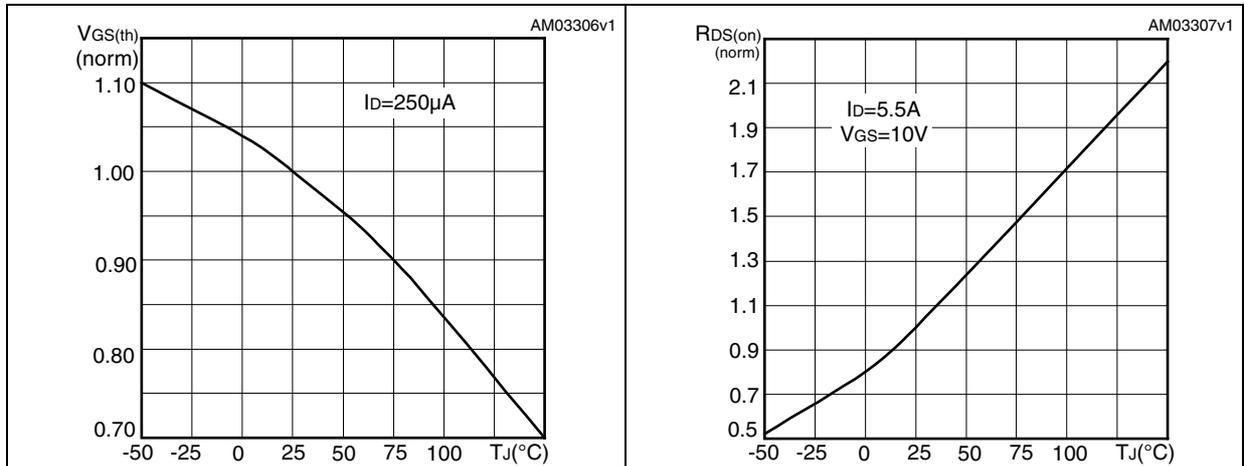
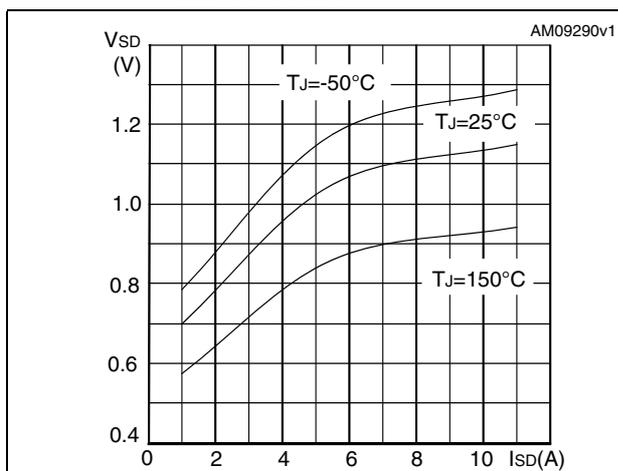
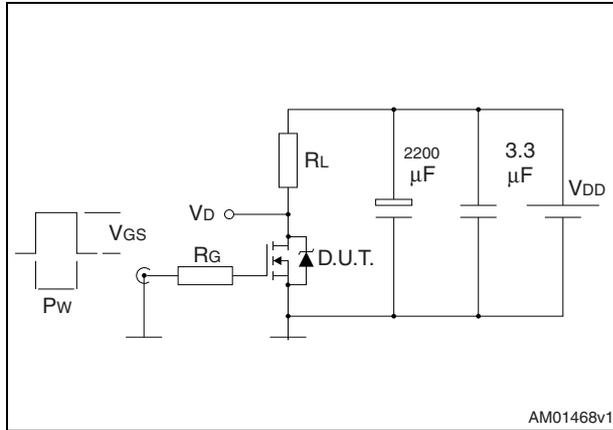


Figure 12. Source-drain diode forward characteristics

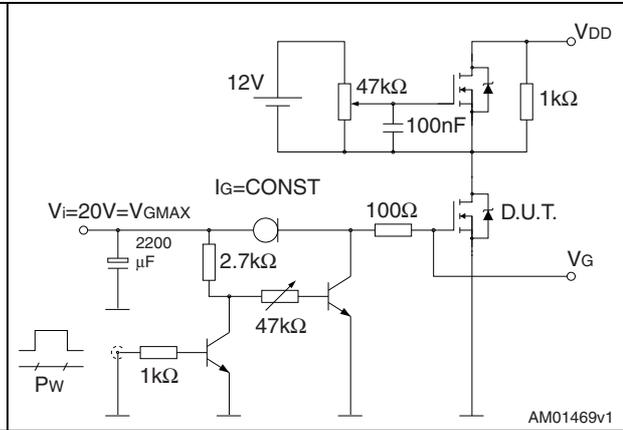


### 3 Test circuits

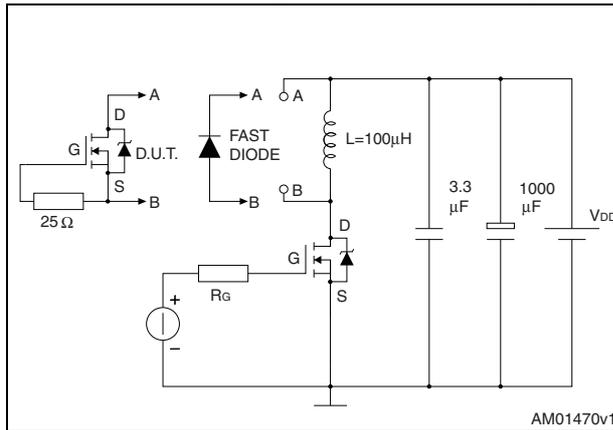
**Figure 13. Switching times test circuit for resistive load**



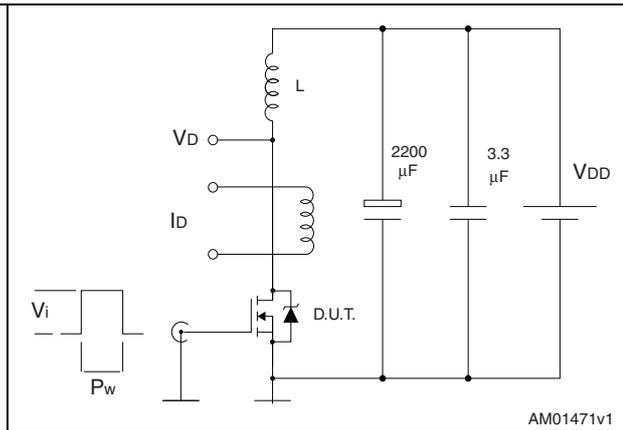
**Figure 14. Gate charge test circuit**



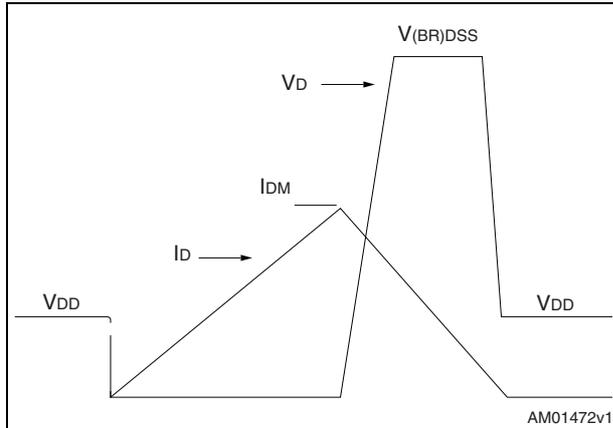
**Figure 15. Test circuit for inductive load switching and diode recovery times**



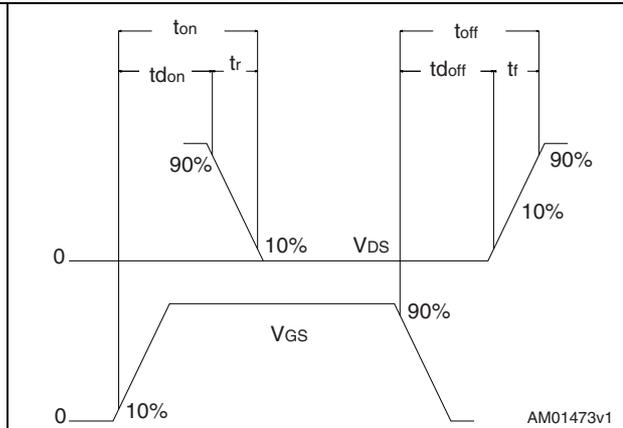
**Figure 16. Unclamped inductive load test circuit**



**Figure 17. Unclamped inductive waveform**



**Figure 18. Switching time waveform**



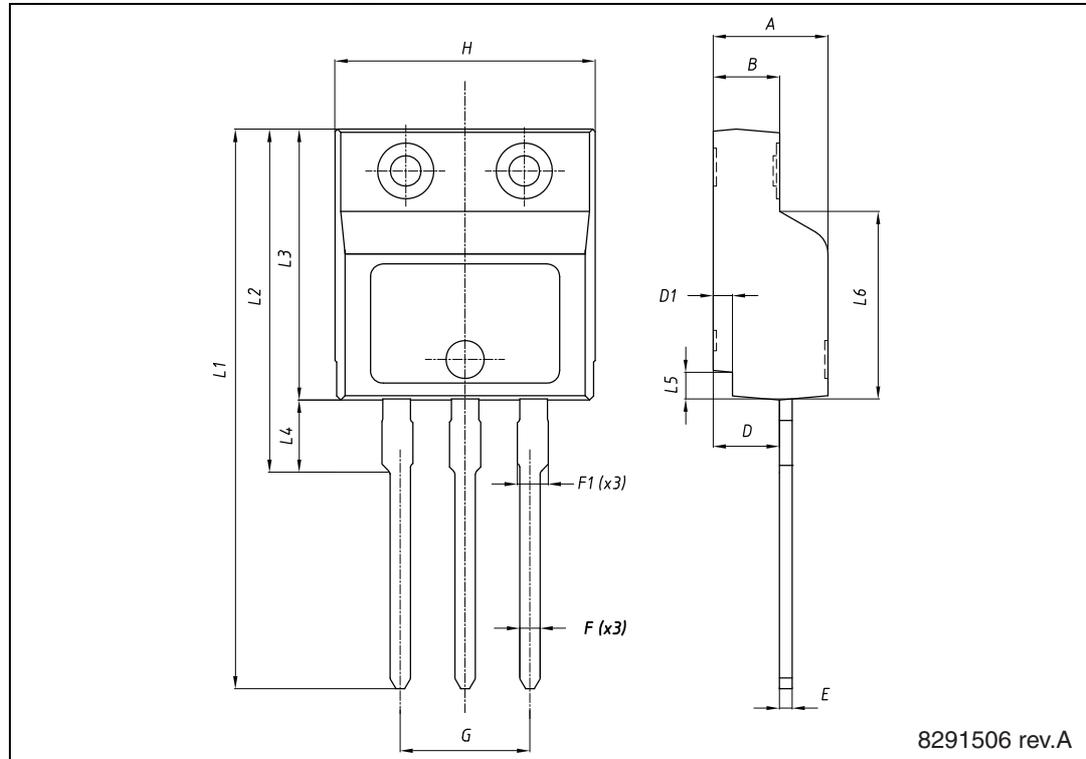
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Table 9. I<sup>2</sup>PakFP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95	-	5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.30		7.50

Figure 19. I<sup>2</sup>PakFP drawing



## 5 Revision history

Table 10. Document revision history

Date	Revision	Changes
21-Jun-2011	1	First release.
03-Nov-2011	2	<i>Figure 2: Safe operating area</i> and <i>Figure 3: Thermal impedance</i> have been added.

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