STK22C48

16 Kbit (2K x 8) AutoStore nvSRAM

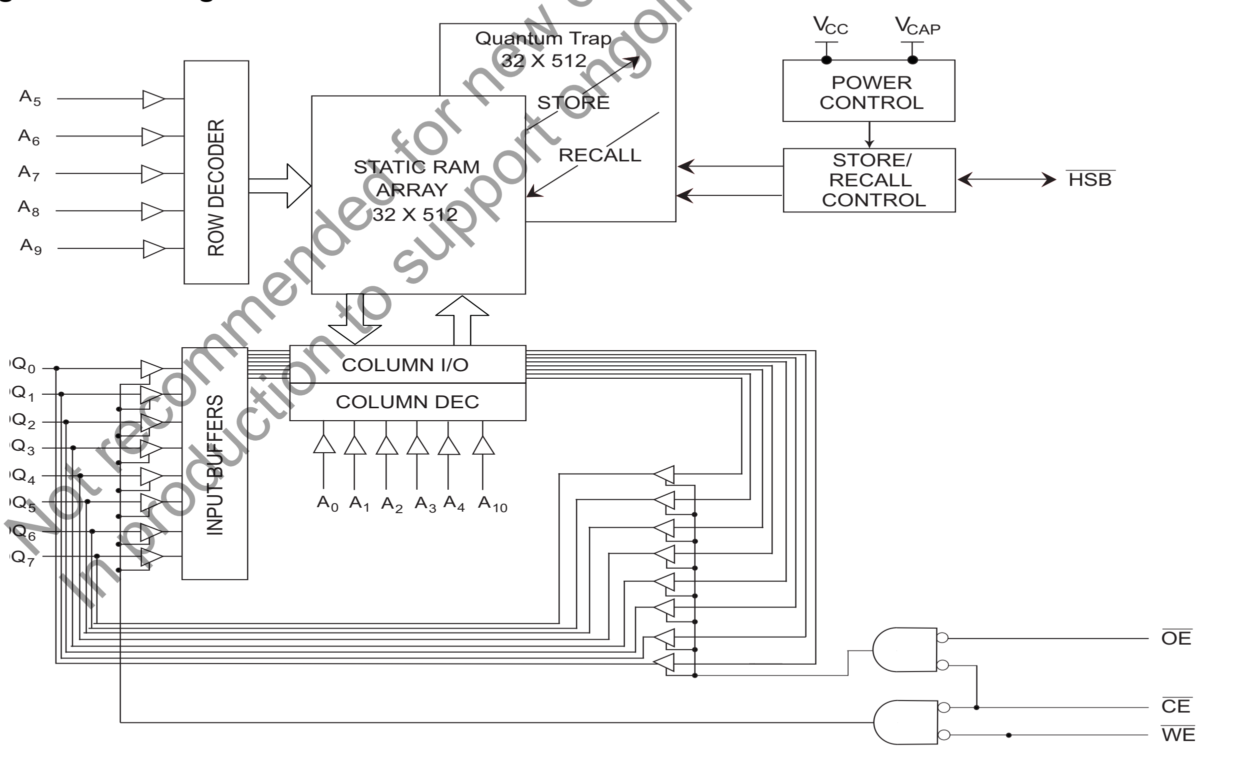
Features

- 25 ns and 45 ns access times
- Hands off automatic STORE on power down with external 68 µF capacitor
- STORE to QuantumTrap™ nonvolatile elements is initiated by software, hardware, or AutoStore™ on power down
- RECALL to SRAM initiated by software or power up
- Unlimited Read, Write, and Recall cycles
- 1,000,000 STORE cycles to QuantumTrap
- 100 year data retention to QuantumTrap
- Single 5V±10% operation
- Commercial and industrial temperatures
- 28-pin 300 mil and (330 mil) SOIC package
- RoHS compliance

Functional Description

The Cypress STK22C48 is a fast static RAM with a nonvolatile element in each memory cell. The embedded nonvolatile elements incorporate QuantumTrap technology producing the world's most reliable nonvolatile memory. The SRAM provides unlimited read and write cycles, while independent nonvolatile data resides in the highly reliable QuantumTrap cell. Data transfers from the SRAM to the nonvolatile elements (the STORE operation) takes place automatically at power down. On power up, data is restored to the SRAM (the RECALL operation) from the nonvolatile memory. A hardware STORE is initiated with the HSB pin.

Logic Block Diagram



Contents

Device Operation

The STK22C48 nvSRAM is made up of two functional components paired in the same physical cell. These are an SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates as a standard fast static RAM. Data in the SRAM is transferred to the nonvolatile cell (the STORE operation) or from the nonvolatile cell to SRAM (the RECALL operation). This unique architecture enables the storage and recall of all cells in parallel. During the STORE and RECALL operations, SRAM Read and Write operations are inhibited. The STK22C48 supports unlimited reads and writes similar to a typical SRAM. In addition, it provides unlimited RECALL operations from the nonvolatile cells and up to one million STORE operations.

SRAM Read

The STK22C48 performs a Read cycle whenever $\overline{CE}$ and $\overline{OE}$ are LOW while $\overline{WE}$ and $\overline{HSB}$ are HIGH. The address specified on pins A_{0-10} determines the 2,048 data bytes accessed. When the Read is initiated by an address transition, the outputs are valid after a delay of t_{AA} (Read cycle 1). If the Read is initiated by $\overline{CE}$ or $\overline{OE}$, the outputs are valid at t_{ACE} or at t_{DOE}, whichever is later (Read cycle 2). The data outputs repeatedly respond to address changes within the t_{AA} access time without the need for transitions on any control input pins, and remains valid until another address change or until $\overline{CE}$ or $\overline{OE}$ is brought HIGH, or $\overline{WE}$ or $\overline{HSB}$ is brought LOW.

SRAM Write

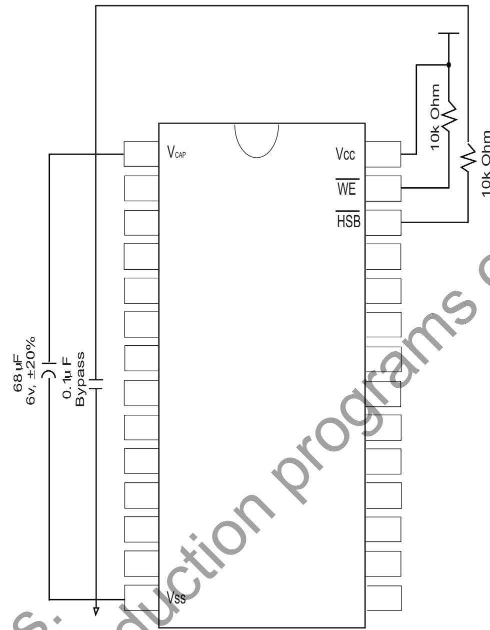
A Write cycle is performed whenever $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{HSB}$ is HIGH. The address inputs must be stable prior to entering the Write cycle and must remain stable until either $\overline{CE}$ or $\overline{WE}$ goes HIGH at the end of the cycle. The data on the common I/O pins DQ_{0-7} are written into the memory if it has valid t_{SD}, before the end of a $\overline{WE}$ controlled Write or before the end of an $\overline{CE}$ controlled Write. Keep $\overline{OE}$ HIGH during the entire Write cycle to avoid data bus contention on common I/O lines. If $\overline{OE}$ is left LOW, internal circuitry turns off the output buffers t_{HZWE} after $\overline{WE}$ goes LOW.

AutoStore Operation

During normal operation, the device draws current from V_{CC} to charge a capacitor connected to the V_{CAP} pin. This stored charge is used by the chip to perform a single STORE operation. If the voltage on the V_{CC} pin drops below V_{SWITCH}, the part automatically disconnects the V_{CAP} pin from V_{CC}. A STORE operation is initiated with power provided by the V_{CAP} capacitor.

Figure 1 shows the proper connection of the storage capacitor (V_{CAP}) for automatic store operation. A charge storage capacitor between 68 µF and 220 µF (±20%) rated at 6V should be

Figure 1. AutoStore Mode



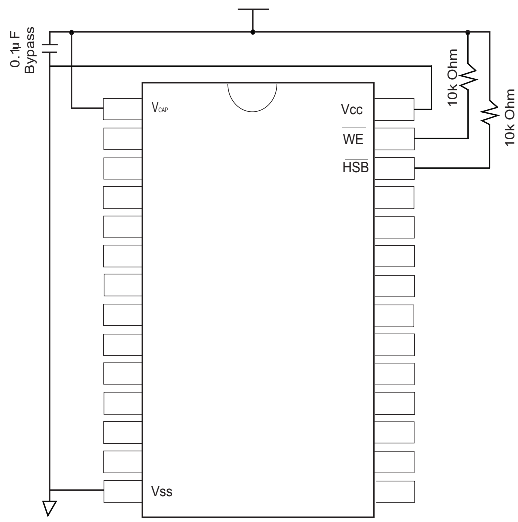
In system power mode, both V_{CC} and V_{CAP} are connected to the +5V power supply without the 68 µF capacitor. In this mode, the AutoStore function of the STK22C48 operates on the stored system charge as power goes down. The user must, however, guarantee that V_{CC} does not drop below 3.6V during the 10 ms STORE cycle.

To prevent unneeded STORE operations, automatic STOREs and those initiated by externally driving $\overline{HSB}$ LOW are ignored, unless at least one WRITE operation takes place since the most recent STORE or RECALL cycle. An optional pull up resistor is shown connected to $\overline{HSB}$. This is used to signal the system that the AutoStore cycle is in progress.

AutoStore Inhibit mode

If an automatic STORE on power loss is not required, then V_{CC} is tied to ground and +5V is applied to V_{CAP} (Figure 2). This is the AutoStore Inhibit mode, where the AutoStore function is disabled. If the STK22C48 is operated in this configuration, references to V_{CC} are changed to V_{CAP} throughout this data sheet. In this mode, STORE operations are triggered with the $\overline{HSB}$ pin. It is not permissible to change between these three options "on the fly".

Figure 2. AutoStore Inhibit Mode



Hardware STORE (HSB) Operation

The STK22C48 provides the HSB pin for controlling and acknowledging the STORE operations. The HSB pin is used to request a hardware STORE cycle. When the HSB pin is driven LOW, the STK22C48 conditionally initiates a STORE operation after t_{DELAY}. An actual STORE cycle only begins if a Write to the SRAM takes place since the last STORE or RECALL cycle. The HSB pin also acts as an open drain driver that is internally driven LOW to indicate a busy condition, while the STORE (initiated by any means) is in progress. Pull up this pin with an external 10K ohm resistor to V_{CAP} if HSB is used as a driver.

SRAM Read and Write operations, that are in progress when HSB is driven LOW by any means, are given time to complete before the STORE operation is initiated. After HSB goes LOW, the STK22C48 continues SRAM operations for t_{DELAY}. During t_{DELAY}, multiple SRAM Read operations take place. If a Write is in progress when HSB is pulled LOW, it allows a time, t_{DELAY} to complete. However, any SRAM Write cycles requested after HSB goes LOW are inhibited until HSB returns HIGH.

During any STORE operation, regardless of how it is initiated, the STK22C48 continues to drive the HSB pin LOW, releasing it only when the STORE is complete. After completing the STORE operation, the STK22C48 remains disabled until the HSB pin returns HIGH.

If HSB is not used, it is left unconnected.

Hardware RECALL (Power Up)

During power up or after any low power condition (V_{CC} < V_{RESET}), an internal RECALL request is latched. When V_{CC} once again exceeds the sense voltage of V_{SWITCH}, a RECALL cycle is automatically initiated and takes $t_{HRECALL}$ to complete.

Data Protection

The STK22C48 protects data from corruption during low voltage conditions by inhibiting all externally initiated STORE and Write operations. The low voltage condition is detected when V_{CC} is less than V_{SWITCH}. If the STK22C48 is in a Write mode (both CE and WE are low) at power up after a RECALL or after a STORE, the Write is inhibited until a negative transition on CE or WE is detected. This protects against inadvertent writes during power up or brown out conditions.

Noise Considerations

The STK22C48 is a high speed memory. It must have a high frequency bypass capacitor of approximately 0.1 µF connected between V_{CC} and $V_{SS,}$ using leads and traces that are as short as possible. As with all high speed CMOS ICs, careful routing of power, ground, and signals reduce circuit noise.

Hardware Protect

The STK22C48 offers hardware protection against inadvertent STORE operation and SRAM Writes during low voltage conditions. When V_{CAP}<V_{SWITCH}, all externally initiated STORE operations and SRAM Writes are inhibited. AutoStore can be completely disabled by tying VCC to ground and applying +5V to V_{CAP}. This is the AutoStore Inhibit mode; in this mode, STOREs are only initiated by explicit request using either the software sequence or the HSB pin.

Low Average Active Power

CMOS technology provides the STK22C48 the benefit of drawing significantly less current when it is cycled at times longer than 50 ns. Figure 3 shows the relationship between I_{CC} and Read or Write cycle time. Worst case current consumption is shown for both CMOS and TTL input levels (commercial temperature range, VCC = 5.5V, 100% duty cycle on chip enable). Only standby current is drawn when the chip is disabled. The overall average current drawn by the STK22C48 depends on the following items:

- The duty cycle of chip enable
- The overall cycle rate for accesses
- The ratio of Reads to Writes
- CMOS versus TTL input levels
- The operating temperature
- The V_{CC} level
- I/O loading

Figure 3. Current Versus Cycle Time (Read)

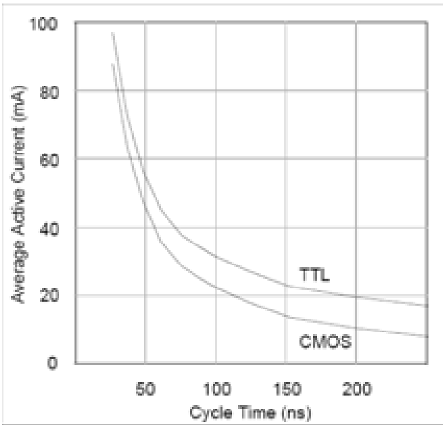
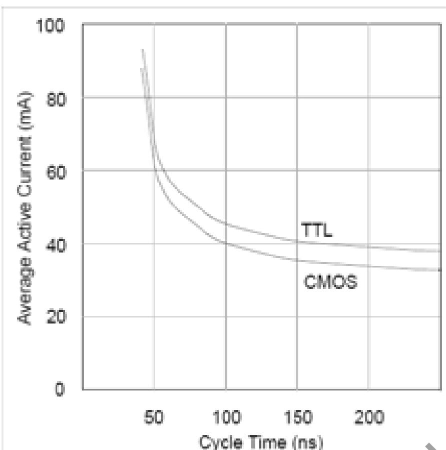


Figure 4. Current Versus Cycle Time (Write)



Preventing Store

The STORE function is disabled by holding $\overline{\text{HSB}}$ high with a driver capable of sourcing 30 mA at a V_{OH} of at least 2.2V, because it must overpower the internal pull down device. This device drives $\overline{\text{HSB}}$ LOW for 20 ns at the onset of a STORE. When the STK22C48 is connected for AutoStore operation (system V_{CC} connected to V_{CC} and a 68 µF capacitor on V_{CAP}) and V_{CC} crosses V_{SWITCH} on the way down, the STK22C48 attempts to pull $\overline{\text{HSB}}$ LOW. If $\overline{\text{HSB}}$ does not actually get below V_{IL}, the part stops trying to pull $\overline{\text{HSB}}$ LOW and abort the STORE attempt.

Best Practices

nvSRAM products have been used effectively for over 15 years. While ease of use is one of the product's main system values, experience gained working with hundreds of applications has resulted in the following suggestions as best practices:

- The nonvolatile cells in an nvSRAM are programmed on the test floor during final test and quality assurance. Incoming inspection routines at customer or contract manufacturer's sites sometimes reprogram these values. Final NV patterns are typically repeating patterns of AA, 55, 00, FF, A5, or 5A. The end product's firmware should not assume that an NV array is in a set programmed state. Routines that check memory content values to determine first time system configuration, cold or warm boot status, and so on must always program a unique NV pattern (for example, complex 4-byte pattern of 46 E6 49 53 hex or more random bytes) as part of the final system manufacturing test to ensure these system routines work consistently.
- Power up boot firmware routines should rewrite the nvSRAM into the desired state. While the nvSRAM is shipped in a preset state, best practice is to again rewrite the nvSRAM into the desired state as a safeguard against events that might flip the bit inadvertently (program bugs, incoming inspection routines, and so on).
- The V_{CAP} value specified in this data sheet includes a minimum and a maximum value size. The best practice is to meet this requirement and not exceed the maximum V_{CAP} value because the higher inrush currents may reduce the reliability of the internal pass transistor. Customers who want to use a larger V_{CAP} value to make sure there is extra store charge should discuss their V_{CAP} size selection with Cypress.

Table 1. Hardware Mode Selection

$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{HSB}}$	A10–A0	Mode	I/O	Power
H	X	H	X	Not Selected	Output High Z	Standby
L	H	H	X	Read SRAM	Output Data	Active[1]
L	L	H	X	Write SRAM	Input Data	Active
X	X	L	X	Nonvolatile STORE	Output High Z	I_{CC2}[2]

Notes
1. I/O state assumes $\overline{\text{OE}} \le V_{IL}$. Activation of nonvolatile cycles does not depend on state of $\overline{\text{OE}}$.
2. $\overline{\text{HSB}}$ STORE operation occurs only if an SRAM Write is done since the last nonvolatile cycle. After the STORE (If any) completes, the part goes into standby mode, inhibiting all operations until $\overline{\text{HSB}}$ rises.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage Temperature .... –65°C to +150°C
Temperature under bias............................. –55°C to +125°C
Supply Voltage on V_{CC} Relative to GND ....–0.5V to 7.0V
Voltage on Input Relative to Vss...........–0.6V to V_{CC} + 0.5V
Voltage on DQ_{0-7} or $\overline{HSB}$ ....–0.5V to Vcc + 0.5V
Power Dissipation 1.0W
DC Output Current (1 output at a time, 1s duration).... 15 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	4.5V to 5.5V
Industrial	-40°C to +85°C	4.5V to 5.5V

DC Electrical Characteristics

Over the operating range (V_{CC} = 4.5V to 5.5V) [3]

Parameter	Description	Test Conditions		Min	Max	Unit
I_{CC1}	Average V_{CC} Current	t_{RC} = 25 ns t_{RC} = 45 ns Dependent on output loading and cycle rate. Values obtained without output loads. I_{OUT} = 0 mA.	Commercial		85 65	mA mA
			Industrial		90 65	mA mA
I_{CC2}	Average V_{CC} Current during STORE	All Inputs Do Not Care, V_{CC} = Max Average current for duration t_{STORE}			3	mA
I_{CC3}	Average V_{CC} Current at t_{RC}= 200 ns, 5V, 25°C Typical	$\overline{WE} \geq (V_{CC} - 0.2V)$. All other inputs cycling. Dependent on output loading and cycle rate. Values obtained without output loads.			10	mA
I_{CC4}	Average V_{CAP} Current during AutoStore Cycle	All Inputs Do Not Care, V_{CC} = Max Average current for duration t_{STORE}			2	mA
I_{SB1}[4]	Average Vcc Current (Standby, Cycling TTL Input Levels)	t_{RC} = 25 ns, $\overline{CE} \geq V_{IH}$ t_{RC} = 45 ns, $\overline{CE} \geq V_{IH}$	Commercial		25 18	mA mA
			Industrial		26 19	mA mA
I_{SB2}[4]	V_{CC} Standby Current	$\overline{CE} \geq (V_{CC} - 0.2V)$. All others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$. Standby current level after nonvolatile cycle is complete. Inputs are static. f = 0 MHz.			1.5	mA
I_{ILK}	Input Leakage Current	V_{CC} = Max, $V_{SS} \leq V_{IN} \leq V_{CC}$		-1	+1	μA
I_{OLK}	Off State Output Leakage Current	V_{CC} = Max, $V_{SS} \leq V_{IN} \leq V_{CC}$, $\overline{CE}$ or $\overline{OE} \geq V_{IH}$ or $\overline{WE} \leq V_{IL}$		-5	+5	μA
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			V_{SS} – 0.5	0.8	V
V_{OH}	Output HIGH Voltage	I_{OUT} = –4 mA except $\overline{HSB}$		2.4		V
V_{OL}	Output LOW Voltage	I_{OUT} = 8 mA except $\overline{HSB}$			0.4	V
V_{BL}	Logic ‘0’ Voltage on $\overline{HSB}$ Output	I_{OUT} = 3 mA			0.4	V
V_{CAP}	Storage Capacitor	Between V_{CAP} pin and Vss, 6V rated. 68 uF -10%, +20% nom.		61	220	μF

Data Retention and Endurance

Parameter	Description	Min	Unit
$DATA_R$	Data Retention	100	Years
NV_C	Nonvolatile STORE Operations	1,000	K

Notes
3. V_{CC} reference levels throughout this data sheet refer to VCC if that is where the power supply connection is made, or V_{CAP} if VCC is connected to ground.
4. $\overline{CE} \geq V_{IH}$ does not produce standby current levels until any nonvolatile cycle in progress has timed out.

Capacitance

In the following table, the capacitance parameters are listed.[5]

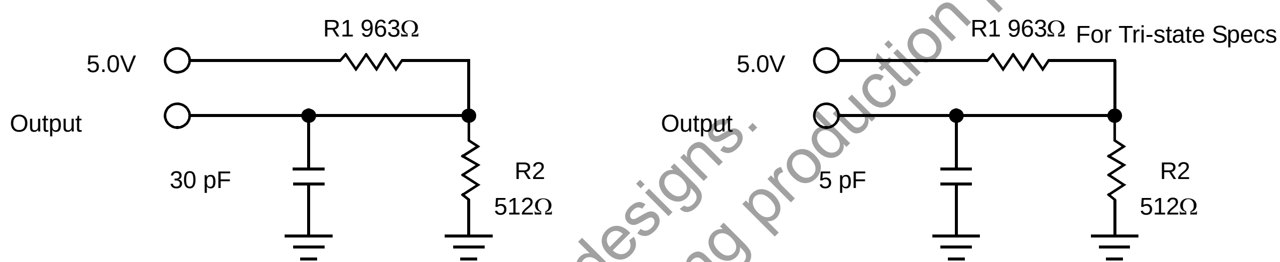
Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 0 to 3.0V	8	pF
C_{OUT}	Output Capacitance		7	pF

Thermal Resistance

In the following table, the thermal resistance parameters are listed.[5]

Parameter	Description	Test Conditions	28-SOIC (300 mil)	28-SOIC (330 mil)	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	TBD	TBD	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		TBD	TBD	°C/W

Figure 5. AC Test Loads



AC Test Conditions

Input Pulse Levels .... 0V to 3V
Input Rise and Fall Times (10% to 90%) .... ≤5 ns
Input and Output Timing Reference Levels 1.5V

Note
5. These parameters are guaranteed by design and are not tested.

AC Switching Characteristics

SRAM Read Cycle

Parameter		Description	25 ns		45 ns		Unit
Cypress Parameter	Alt		Min	Max	Min	Max	
t_{ACE}	t_{ELQV}	Chip Enable Access Time		25		45	ns
t_{RC} [6]	t_{AVAV}, t_{ELEH}	Read Cycle Time	25		45		ns
t_{AA} [7]	t_{AVQV}	Address Access Time		25		45	ns
t_{DOE}	t_{GLQV}	Output Enable to Data Valid		10		20	ns
t_{OHA} [7]	t_{AXQX}	Output Hold After Address Change	5		5		ns
t_{LZCE} [8]	t_{ELQX}	Chip Enable to Output Active	5		5		ns
t_{HZCE} [8]	t_{EHQZ}	Chip Disable to Output Inactive		10		15	ns
t_{LZOE} [8]	t_{GLQX}	Output Enable to Output Active	0		0		ns
t_{HZOE} [8]	t_{GHQZ}	Output Disable to Output Inactive		10		15	ns
t_{PU} [5]	t_{ELICCH}	Chip Enable to Power Active	0		0		ns
t_{PD} [5]	t_{EHICCL}	Chip Disable to Power Standby		25		45	ns

Switching Waveforms

Figure 6. SRAM Read Cycle 1: Address Controlled [6, 7]

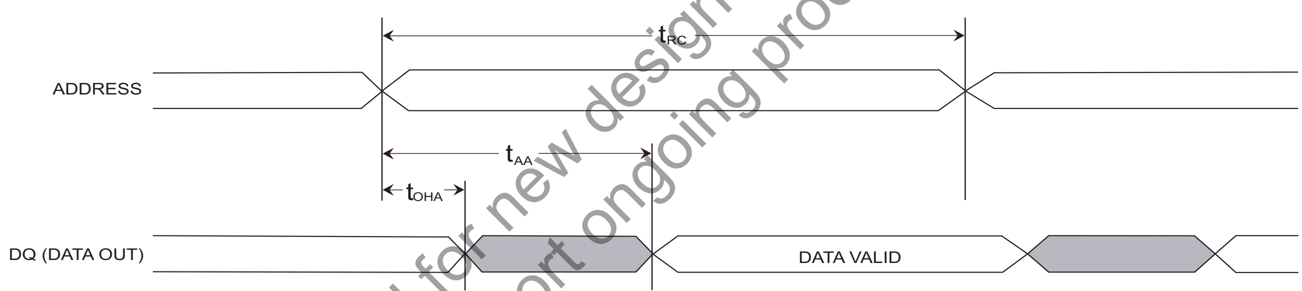
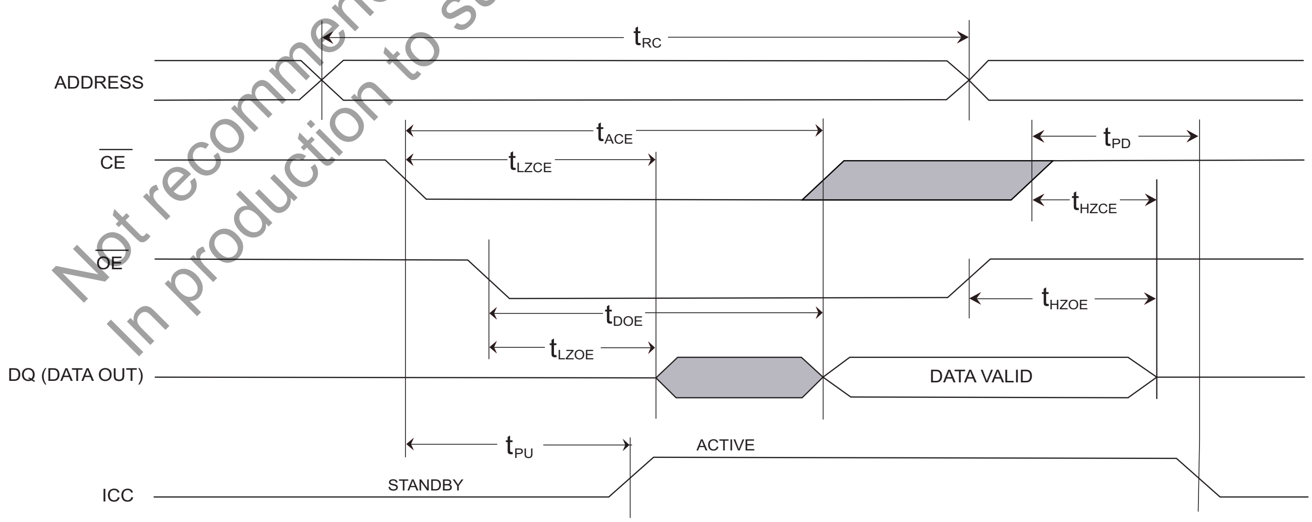


Figure 7. SRAM Read Cycle 2: $\overline{CE}$ and $\overline{OE}$ Controlled [6]



Notes
6. $\overline{WE}$ and $\overline{HSB}$ must be High during SRAM Read cycles.
7. Device is continuously selected with $\overline{CE}$ and $\overline{OE}$ both Low.
8. Measured ±200 mV from steady state output voltage.

SRAM Write Cycle

Parameter		Description	25 ns		45 ns		Unit
Cypress Parameter	Alt		Min	Max	Min	Max	
t_{WC}	t_{AVAV}	Write Cycle Time	25		45		ns
t_{PWE}	t_{WLWH}, t_{WLEH}	Write Pulse Width	20		30		ns
t_{SCE}	t_{ELWH}, t_{ELEH}	Chip Enable To End of Write	20		30		ns
t_{SD}	t_{DVWH}, t_{DVEH}	Data Setup to End of Write	10		15		ns
t_{HD}	t_{WHDX}, t_{EHDX}	Data Hold After End of Write	0		0		ns
t_{AW}	t_{AVWH}, t_{AVEH}	Address Setup to End of Write	20		30		ns
t_{SA}	t_{AVWL}, t_{AVEL}	Address Setup to Start of Write	0		0		ns
t_{HA}	t_{WHAX}, t_{EHAX}	Address Hold After End of Write	0		0		ns
t_{HZWE} [8,9]	t_{WLQZ}	Write Enable to Output Disable		10		14	ns
t_{LZWE} [8]	t_{WHQX}	Output Active After End of Write	5		5		ns

Switching Waveforms

Figure 8. SRAM Write Cycle 1: $\overline{WE}$ Controlled [10, 11]

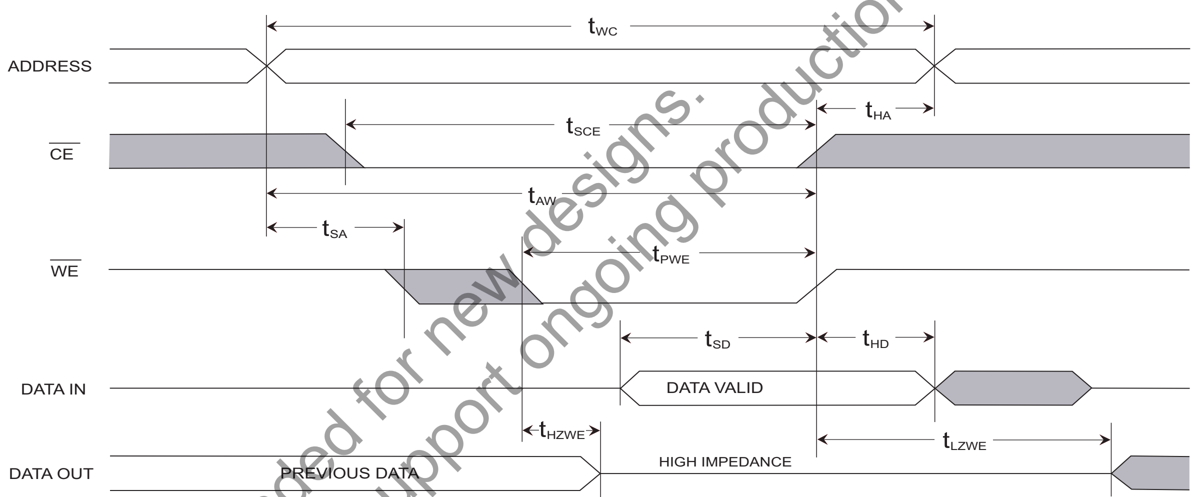
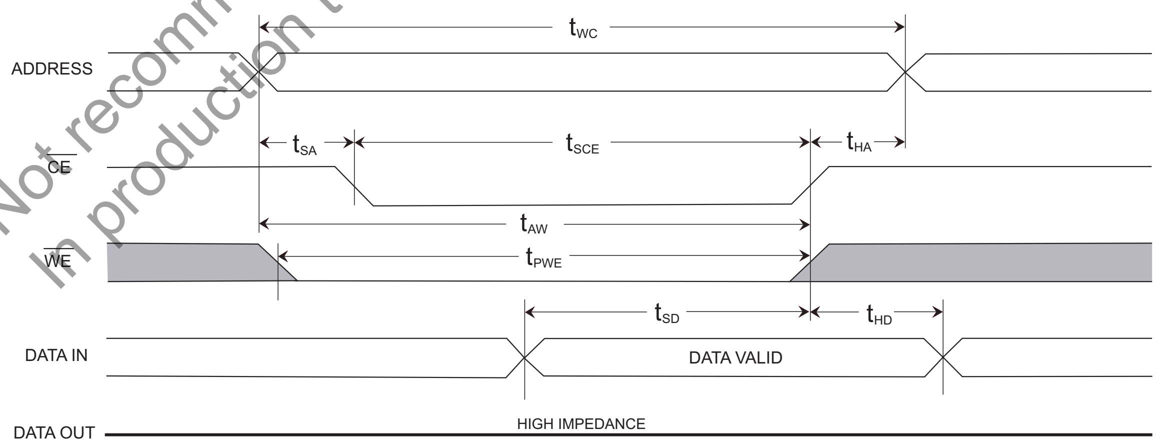


Figure 9. SRAM Write Cycle 2: $\overline{CE}$ Controlled [10, 11]



Notes

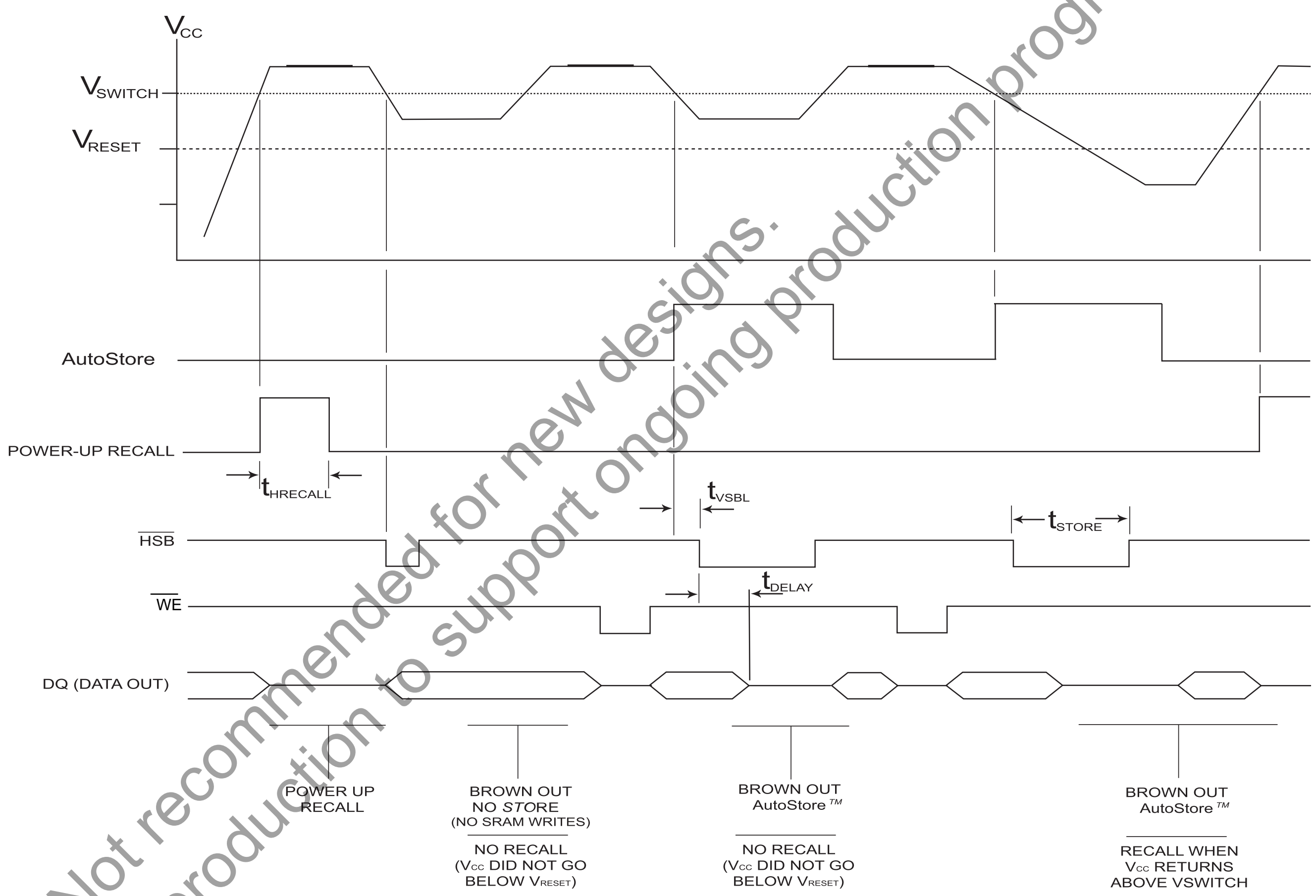
9. If $\overline{WE}$ is Low when $\overline{CE}$ goes Low, the outputs remain in the high impedance state.
10. $\overline{HSB}$ must be high during SRAM Write cycles.
11. $\overline{CE}$ or $\overline{WE}$ must be greater than V_{IH} during address transitions.

AutoStore or Power Up RECALL

Parameter	Alt	Description	STK22C48		Unit
			Min	Max	
$t_{HRECALL}$ [12]	$t_{RESTORE}$	Power up RECALL Duration		550	µs
t_{STORE} [14, 15]	t_{HLHZ}	STORE Cycle Duration		10	ms
t_{DELAY} [13]	t_{HLQZ} , t_{BLQZ}	Time Allowed to Complete SRAM Cycle	1		µs
V_{SWITCH}		Low Voltage Trigger Level	4.0	4.5	V
V_{RESET}		Low Voltage Reset Level		3.6	V
t_{VSBL} [10]		Low Voltage Trigger (V_{SWITCH}) to $\overline{HSB}$ Low		300	ns

Switching Waveform

Figure 10. AutoStore/Power Up RECALL



Notes

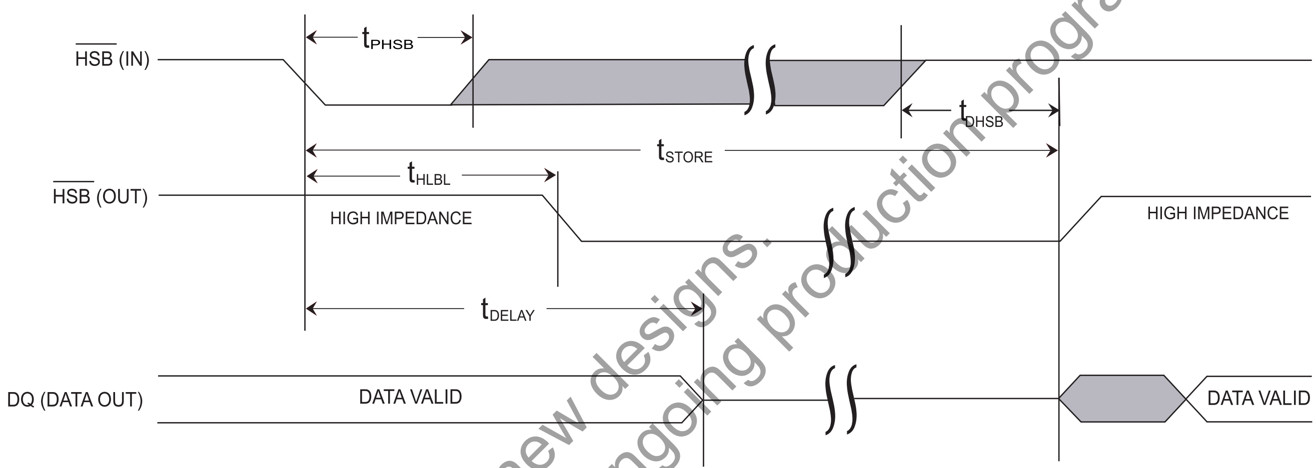
12. $t_{HRECALL}$ starts from the time V_{CC} rises above V_{SWITCH}.
13. $\overline{CE}$ and $\overline{OE}$ low for output behavior.
14. $\overline{CE}$ and $\overline{OE}$ low and WE high for output behavior.
15. $\overline{HSB}$ is asserted low for 1us when V_{CAP} drops through V_{SWITCH}. If an SRAM Write has not taken place since the last nonvolatile cycle, $\overline{HSB}$ is released and no store takes place.

Hardware STORE Cycle

Parameter	Alt	Description	STK22C48		Unit
			Min	Max	
t_{DHSB} [13, 16]	$t_{RECOVER}$, t_{HHQX}	Hardware STORE High to Inhibit Off		700	ns
t_{PHSB}	t_{HLHX}	Hardware STORE Pulse Width	15		ns
t_{HLBL}		Hardware STORE Low to STORE Busy		300	ns

Switching Waveform

Figure 11. Hardware STORE Cycle



Note

16. t_{DHSB} is only applicable after t_{STORE} is complete.

Part Numbering Nomenclature

STK22C48 - N F 45 I TR

Packaging Option:
TR = Tape and Reel
Blank = Tube

Temperature Range:
Blank - Commercial (0 to 70°C)
I - Industrial (-40 to 85°C)

Speed:
25 - 25 ns
45 - 45 ns

Lead Finish
F = 100% Sn (Matte Tin)

Package:
N = Plastic 28-pin 300 mil SOIC
S = Plastic 28-pin 330 mil SOIC

Ordering Information

These parts are not recommended for new designs. They are in production to support ongoing production programs only.

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
25	STK22C48-NF25TR	51-85026	28-pin SOIC (300 mil)	Commercial
	STK22C48-NF25	51-85026	28-pin SOIC (300 mil)	
	STK22C48-SF25TR	51-85058	28-pin SOIC (330 mil)	
	STK22C48-SF25	51-85058	28-pin SOIC (330 mil)	
	STK22C48-NF25ITR	51-85026	28-pin SOIC (300 mil)	Industrial
	STK22C48-NF25I	51-85026	28-pin SOIC (300 mil)	
	STK22C48-SF25ITR	51-85058	28-pin SOIC (330 mil)	
	STK22C48-SF25I	51-85058	28-pin SOIC (330 mil)	
45	STK22C48-NF45TR	51-85026	28-pin SOIC (300 mil)	Commercial
	STK22C48-NF45	51-85026	28-pin SOIC (300 mil)	
	STK22C48-SF45TR	51-85058	28-pin SOIC (330 mil)	
	STK22C48-SF45	51-85058	28-pin SOIC (330 mil)	
	STK22C48-NF45ITR	51-85026	28-pin SOIC (300 mil)	Industrial
	STK22C48-NF45I	51-85026	28-pin SOIC (300 mil)	
	STK22C48-SF45ITR	51-85058	28-pin SOIC (330 mil)	
	STK22C48-SF45I	51-85058	28-pin SOIC (330 mil)	

All parts are Pb-free. The above table contains Final information. Please contact your local Cypress sales representative for availability of these parts

Package Diagrams

Figure 12. 28-Pin (300 mil) SOIC (51-85026)

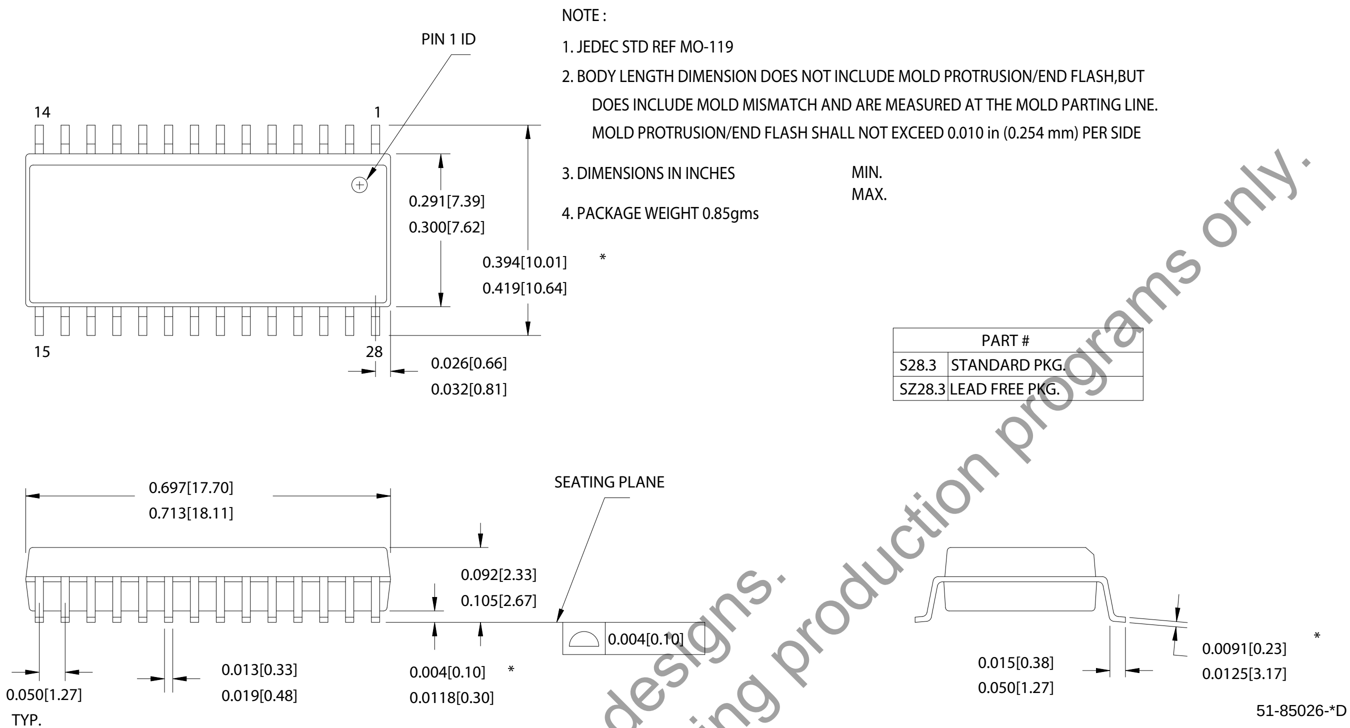
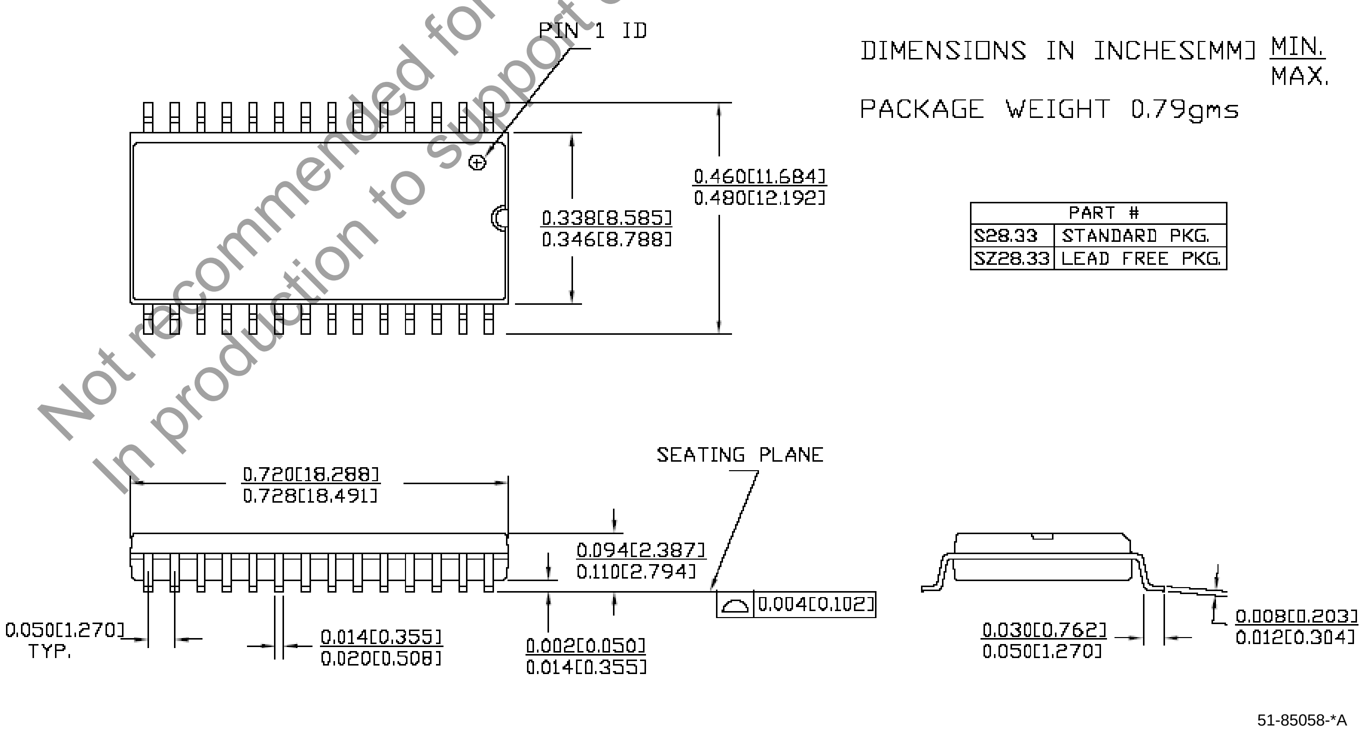


Figure 13. 28-Pin (330 mil) SOIC (51-85058)



Document History Page

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Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	2625139	GVCH/PYRS	01/30/09	New data sheet
*A	2826441	GVCH	12/11/2009	Added following text in the Ordering Information section: “These parts are not recommended for new designs. In production to support ongoing production programs only.” Added watermark in PDF stating “Not recommended for new designs. In production to support ongoing production programs only.” Added Contents on page 2.

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