Ordering number : EN*A2327

STK541UC60C-E

Advance Information

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Inverter IPM for 3-phase Motor Drive

Overview

This "Inverter IPM" includes the output stage of a 3-phase inverter, pre-drive circuits, and bootstrap circuits as well as protection circuits in one package.

Function

- SIP(Single in-line package) using a solid transfer mold.
- Protective circuits including over current and pre-drive low voltage protection are built in.
- Direct input of CMOS level control signals without an insulating circuit is possible.
- A single power supply drive is enabled through the use of bootstrap circuits for upper IGBT gate drives.
- Overcurrent protection current is programmable with an external resistance.

Certification

- UL1557 (File Number : E339285).

Specifications

Absolute Maximum Ratings at Tc = 25°C

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{CC}	+ to -, surge<500V	*1	450	V
Collector-emitter voltage	V_{CE}	+ to U,V,W or U,V,W to -		600	V
Output current	Io	+, -, U,V,W terminal current		±10	A
		+, -, U,V,W terminal current at Tc=100°C		±5	A
Output peak current	Iop	+, -, U,V,W terminal current for a Pulse width of 1ms		±20	A
Pre-driver voltage	VD1,2,3,4	VB1 to U, VB2 to V, VB3 to W, V_{DD} to V_{SS}	*2	20	V
Input signal voltage	VIN	HIN1, 2, 3, LIN1, 2, 3		−0.3 to V_{DD}	V
FAULT terminal voltage	VFAULT	FAULT terminal		−0.3 to V_{DD}	V
Maximum power dissipation	Pd	IGBT per channel		22	W
Junction temperature	Tj	IGBT,FRD		150	°C
Storage temperature	Tstg			−40 to +125	°C
Operating substrate temperature	Tc	IPM case temperature		−40 to +100	°C
Tightening torque		Case mounting screws	*3	0.9	Nm
Withstand voltage	Vis	50Hz sine wave AC 1 minute	*4	2000	VRMS

Reference voltage is "V_{SS}" terminal voltage unless otherwise specified.

*1 : Surge voltage developed by the switching operation due to the wiring inductance between + and - terminal.

*2 : VD1=VB1 to U, VD2=VB2 to V, VD3=VB3 to W, VD4=V_{DD} to V_{SS} terminal voltage.

*3 : Flatness of the heat-sink should be less than 0.15mm.

*4 : Test conditions : AC2500V, 1 second.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ORDERING INFORMATION

See detailed ordering and shipping information on page 16 of this data sheet.

Electrical Characteristics at Tc = 25°C, VD1, VD2, VD3, VD4 = 15V

Parameter	Symbol	Conditions		Test circuit	Ratings min	Ratings typ	Ratings max	Unit
Power output section								
Collector-emitter cut-off current	ICE	V_{CE} = 600V		Fig.1	-	-	0.1	mA
Bootstrap diode reverse current	IR(BD)	VR(BD)			-	-	0.1	mA
Collector to emitter saturation voltage	VCE(SAT)	Ic=10A Tj=25°C	Upper side	Fig.2	-	1.4	2.3	V
			Lower side *1		-	1.7	2.6	
		Ic=5A Tj=100°C	Upper side		-	1.3	-	
			Lower side *1		-	1.6	-	
Diode forward voltage	VF	IF=–10A Tj=25°C	Upper side	Fig.3	-	1.3	2.2	V
			Lower side *1		-	1.6	2.5	
		IF=–5A Tj=100°C	Upper side		-	1.2	-	
			Lower side *1		-	1.5	-	
Junction to case thermal resistance	θj-c(T)	IGBT			-	-	5.5	°C/W
	θj-c(D)	FRD			-	-	6.5	
Control (Pre-driver) section								
Pre-driver power dissipation	ID	VD1, 2, 3 = 15V		Fig.4	-	0.08	0.4	mA
		VD4 = 15V			-	1.6	4	
High level Input voltage	Vin H	HIN1, HIN2, HIN3, LIN1, LIN2, LIN3 to V_{SS}			-	-	0.8	V
Low level Input voltage	Vin L				2.5	-	-	V
Input threshold voltage hysteresis	Vinth(hys)				0.5	0.8	-	V
Logic 0 input leakage current	I_{IN+}	VIN=+3.3V			76	118	160	μA
Logic 1 input leakage current	I_{IN-}	VIN=0V			97	150	203	μA
FAULT terminal input electric current	IoSD	FAULT : ON/VFAULT=0.1V			-	2	-	mA
FAULT clearance delay time	FLTCLR	From time fault condition clears.			6	9	12	ms
V_{CC} and V_S undervoltage upper threshold.	V_{CCUV+} V_{SUV+}				10.5	11.1	11.7	V
V_{CC} and V_S undervoltage lower threshold.	V_{CCUV-} V_{SUV-}				10.3	10.9	11.5	V
V_{CC} and V_S undervoltage hysteresis	V_{CCUVH} V_{SUVH-}				0.14	0.2	-	A
Over current protection current	ISD	PW=100μs, RSD = 0Ω		Fig.5	10	-	17	A
Electric current output signal level	ISO	Io = 10A			0.30	0.33	0.36	V

Reference voltage is "V_{SS}" terminal voltage unless otherwise specified.

*1 : The lower side's VCE(SAT) and VF include a loss by the shunt resistance

Parameter	Symbol	Conditions	Test circuit	Ratings min	Ratings typ	Ratings max	Unit
Switching Character							
Switching time	tON	Io = 10A Inductive load	Fig.6	0.3	0.6	1.3	μs
	tOFF			-	1.0	1.8	
Turn-on switching loss	Eon	Ic=5A,V^+=300V, V_{DD}=15V,L=3.9mH Tc=25°C	Fig.6	-	240	-	uJ
Turn-off switching loss	Eoff			-	220	-	uJ
Total switching loss	Etot			-	460	-	uJ
Turn-on switching loss	Eon	Ic=5A,V^+=300V, V_{DD}=15V,L=3.9mH Tc=100°C	Fig.6	-	300	-	uJ
Turn-off switching loss	Eoff			-	260	-	uJ
Total switching loss	Etot			-	560	-	uJ
Diode reverse recovery energy	Erec	I_F=5A, V^+=400V, V_{DD}=15V, L=3.9mH, Tc=100°C		-	17	-	uJ
Diode reverse recovery time	Trr			-	62	-	ns
Reverse bias safe operating area	RBSOA	Io =20A, V_{CE} = 450V	Fig.7	Full square			
Short circuit safe operating area	SCSOA	VCE = 400V, Tc=100°C		4	-	-	μs
Allowable offset voltage slew rate	dv/dt	Between U, V, W to -		–50	-	50	V/ns

Reference voltage is "V_{SS}" terminal voltage unless otherwise specified.

Notes: 1. Input ON voltage indicates a value to turn on output stage IGBT of Vin >= Vin H.
Input OFF voltage indicates a value to turn off output stage IGBT of Vin < Vin L.

2. Please refer to Figure 8 below.

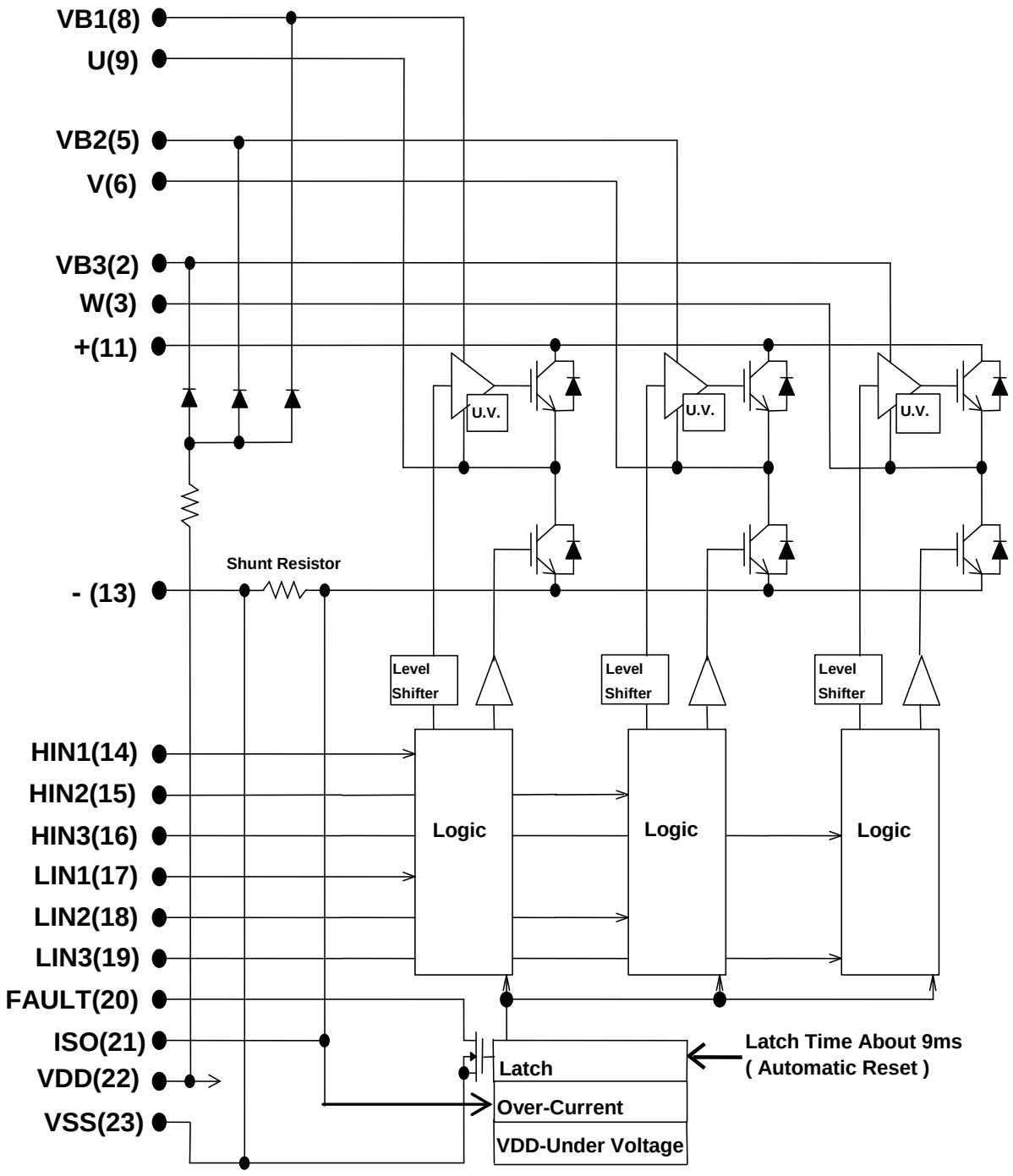
When an under voltage condition occurs the internal protection circuit operation is indicated by FAULT asserted via an active open-drain pulldown.
This signal is non-latching and will release as soon as the fault condition has cleared.
Upon detection of a fault condition all input signals should be set low externally to ensure all outputs are off.
This signal has about 200mV of hysteresis.
Fault condition operation:

1. An under voltage fault will turn off all gates and turn off all output IGBT's.
2. The under voltage lockut will persist until the fault condition clears and will then release the open-drain output immediately.
3. The under voltage FAULT output is not asserted if the only fault is upper gate drive voltage although the upper and lower gates will be turned off.

3. When assembling the IPM on the heat sink, tightening torque range is 0.6Nm to 0.9Nm. Please refer to the Application note for more information.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Equivalent Block Diagram



Module Pin-Out Description

Pin	Name	Description
1	NA	None
2	VB3	High Side Floating Supply Voltage 3
3	W	Output 3 - High Side Floating Supply Offset Voltage
4	NA	None
5	VB2	High Side Floating Supply voltage 2
6	V	Output 2 - High Side Floating Supply Offset Voltage
7	NA	None
8	VB1	High Side Floating Supply voltage 1
9	U	Output 1 - High Side Floating Supply Offset Voltage
10	NA	None
11	+	Positive Bus Input Voltage
12	NA	None
13	-	Negative Bus Input Voltage
14	HIN1	Logic Input High Side Gate Driver - Phase U
15	HIN2	Logic Input High Side Gate Driver - Phase V
16	HIN3	Logic Input High Side Gate Driver - Phase W
17	LIN1	Logic Input Low Side Gate Driver - Phase U
18	LIN2	Logic Input Low Side Gate Driver - Phase V
19	LIN3	Logic Input Low Side Gate Driver - Phase W
20	FAULT	Fault output
21	ISO	Current monitor output
22	VDD	+15V Main Supply
23	VSS	Negative Main Supply

Test Circuit

The tested phase U+ shows the upper side of the U phase and U- shows the lower side of the U phase.

■ ICE / IR(BD)

	U+	V+	W+	U-	V-	W-
M	11	11	11	9	6	3
N	9	6	3	13	13	13

	U(BD)	V(BD)	W(BD)
M	8	5	2
N	23	23	23

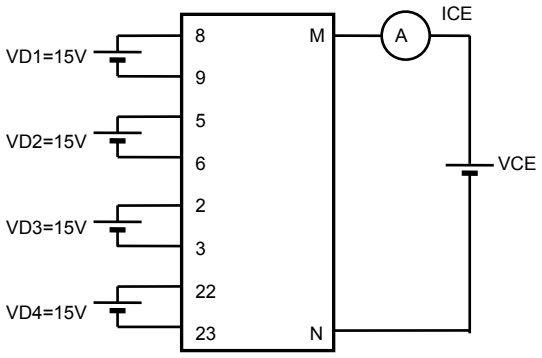


Fig.1

■ VCE(SAT) (test by pulse)

	U+	V+	W+	U-	V-	W-
M	11	11	11	9	6	3
N	9	6	3	13	13	13
m	14	15	16	17	18	19

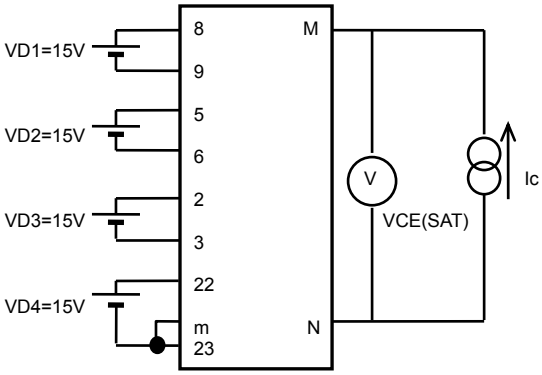


Fig.2

■ VF (test by pulse)

	U+	V+	W+	U-	V-	W-
M	11	11	11	9	6	3
N	9	6	3	13	13	13

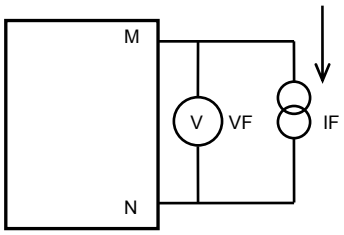


Fig.3

■ ID

	VD1	VD2	VD3	VD4
M	8	5	2	22
N	9	6	3	23

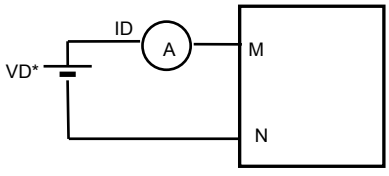


Fig.4

■ ISD

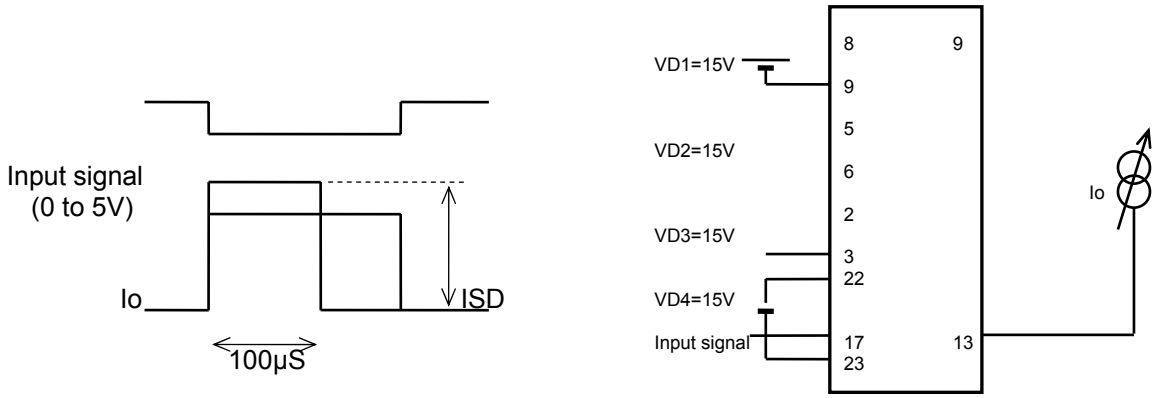


Fig.5

■ Switching time (The circuit is a representative example of the lower side U phase.)

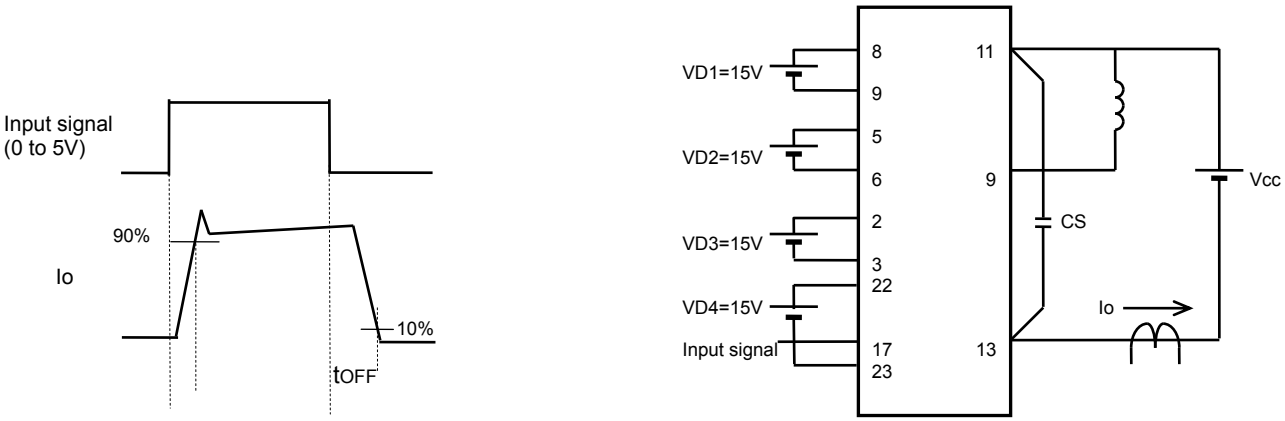


Fig.6

■ RB-SOA (The circuit is a representative example of the lower side U phase.)

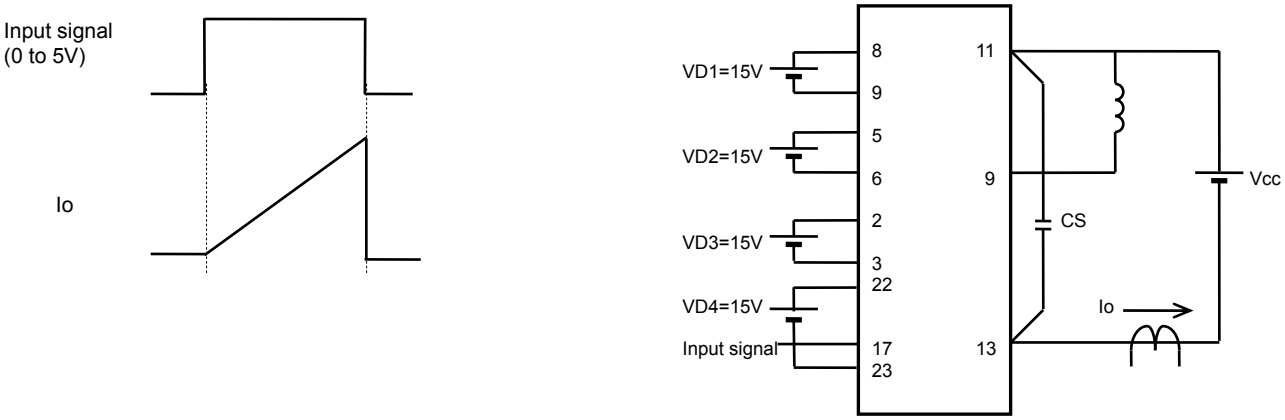


Fig.7

Input / Output Timing Diagram

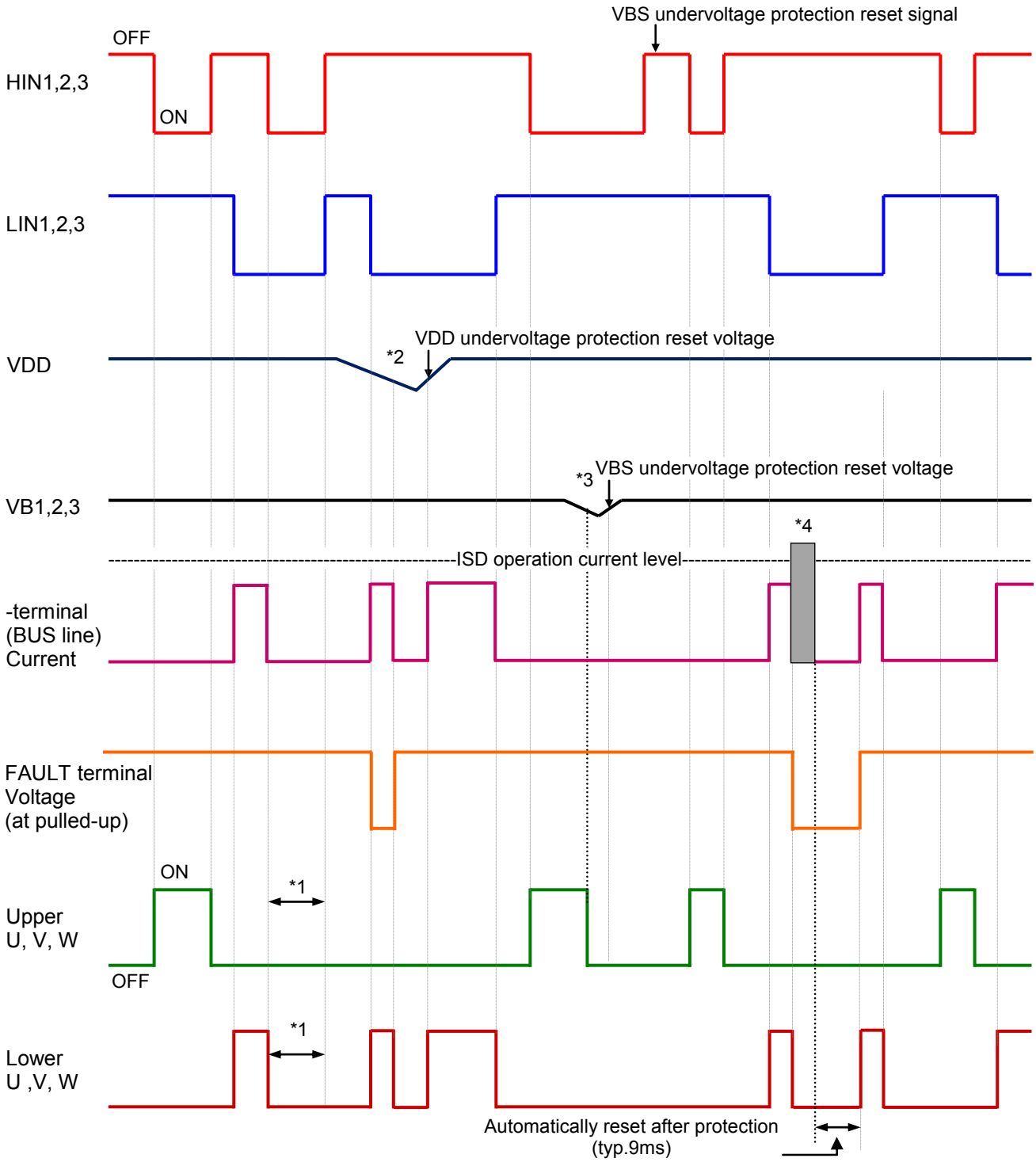


Fig.8

Notes

1. *1 : Diagram shows the prevention of shoot-through via control logic. More deadtime to account for switching delay needs to be added externally.
2. *2 : If lower V_{DD} drops all gate output signals will go low and cut off all of 6 IGBT outputs. part. When V_{DD} rises the operation will resume immediately.
3. *3 : When the upper side gate voltage at VB1, VB2 and VB3 drops only the corresponding upper side output is turned off. The outputs return to normal operation immediately after the upper side gat voltage rises.
4. *4 : In case of over current detection all IGBT's are turned off and the FAULT output is asserted. Normal operation resumes 9ms(typ.) after the over current condition is corrected.

Logic level table

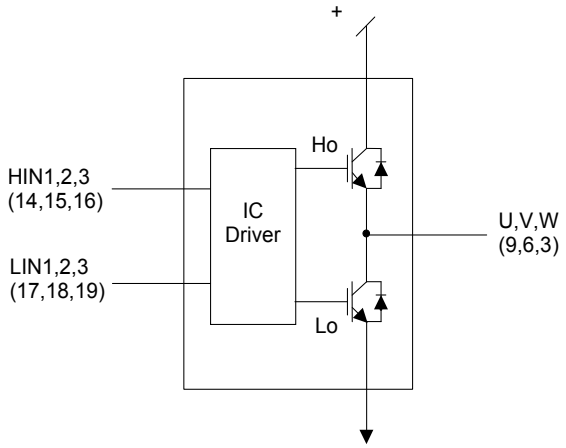
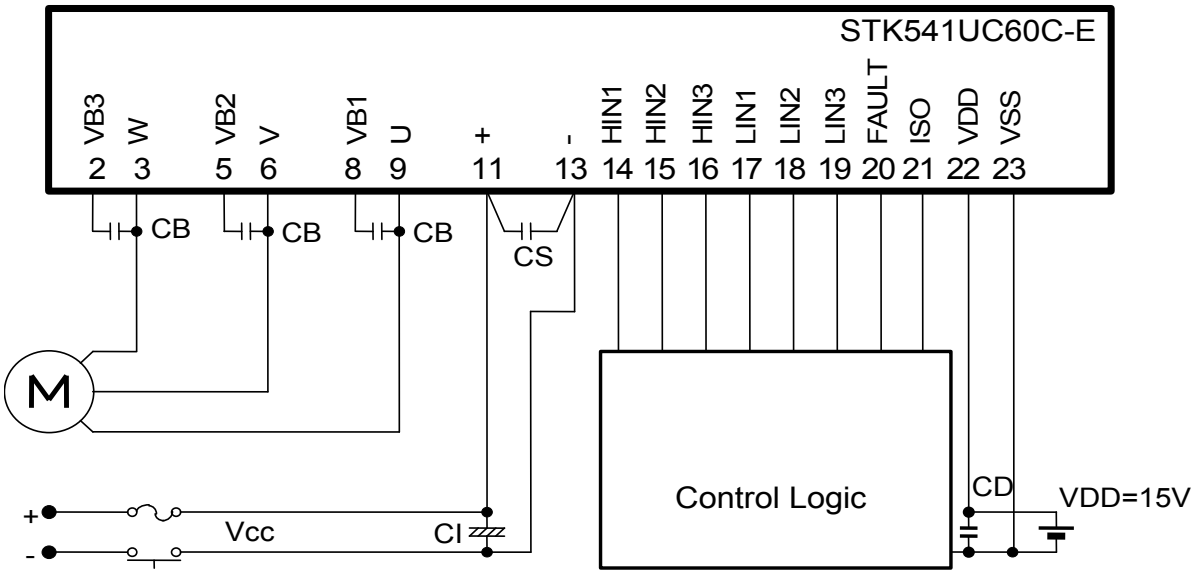


Fig. 9

1=High / 0=Low

FAULT	Itrip	HIN1,2,3	LIN1,2,3	U,V,W
1	0	0	0	Off
1	0	0	1	V+
1	0	1	0	0
1	0	1	1	Off
1	1	X	X	Off
0	X	X	X	Off

Sample Application Circuit



Recommended Operating Conditions at Ta = 25°C

Item	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{CC}	Between V+ to VRU(VRV,VRW)	0	280	450	V
Pre-driver supply voltage	VD1,2,3	Between VB1 to U,VB2 to V,VB3 to W	12.5	15	17.5	V
	VD4	Between VDD to VSS *1	13.5	15	16.5	
ON-state input voltage	VIN(ON)	HIN1,HIN2,HIN3,LIN1,LIN2,LIN3 terminal	0	-	0.3	V
OFF-state input voltage	VIN(OFF)		3.0	-	5.0	
PWM frequency	fPWM		1	-	20	kHz
Dead time	DT	Turn-off to turn-on (External)	2	-	-	μs
Mounting torque	-	'M3' type screw	0.6	-	0.9	Nm

*1 : Pre-drive power supply (VD4=15±1.5V) must be have the capacity of Io=20mA(DC), 0.5A(Peak).

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Usage Precaution

1. This IPM includes bootstrap diode and resistor. Therefore, by adding a capacitor (CB : about 1 to 47μF), a single power supply drive is enabled. In this case, an electric charge is charged to "CB" by making lower side IGBT turn on.
   And, please select the capacitance of "CB"(externally set) equal to or less than 47μF(±20%).If selecting the capacitance more than 47μF(±20%), connect a resistor(about 20Ω)in series between each 3-phase upper side power supply terminals(VB1,2,3) and each bootstrap capacitor. Also, the upper side power supply voltage sometimes declines by the way of controlling. Please confirm the voltage with an actual set.(When not using the bootstrap circuit, each upper side pre-drive power supply needs an external independent power supply.)

2. Because the jump voltage which is accompanied by the vibration in case of switching operation occurs by the influence of the floating inductance of the wiring of the outer power supply which is connected with of the "+" and "-" terminal, restrains and spares serge voltage being as the connection of the snubber circuit (Capacitor / CS /about 0.1uF to 10uF) for the voltage absorption with the neighborhood as possible between the "+" and the point of intersection of the "-" terminal, and so on, with making a wiring length (among the terminals each from "CI")short and making a wiring inductance small.

3. The "FAULT" terminal (20pin) is open Drain (It is operating as "FAULT" when becoming Low).This terminal serves as the shut down function of the built-in pre-driver. (When the terminal voltage is above 3V,normalcy works, and it is shut down when it is equal to or less than 0.8V.) Please make pulling up outside so that "FAULT" terminal voltages become more than 3V.When the pull up voltage (VP) is at 5V, pull up resistor (RP) connects above 10kΩ, and in case of VP=15V, RP connects above 39kΩ.

4. The pull-down resistor (:33kΩ(typ)) is connected with the inside of the signal input terminal, but please connect the pull-down resistor(about 2.2 to 3.3kΩ) outside to decrease the influence of the noise by wiring etc.

5. Because the IPM can be destroyed when the motor connection terminal (pins 9, 6, and 3) is opened while the motor is running, please be especially careful of the connection (soldering condition) of this terminal.

6. “Iso” terminal (21pin) is for the electric current monitor. Be careful, because the overcurrent protection does not operate when short-circuiting “Iso” terminal and “Vss” terminal (23pin).

7. When input pulse width is less than 2μs, an output may not react to the pulse.(Both ON signal and OFF signal)

8. The overcurrent protection feature is not intended to protect in exceptional fault conditions. An external fuse is recommended for safety.

9. An external resistor “RSD” is required for proper overcurrent protection.

■ This data shows the example of the application circuit, does not guarantee a design as the mass production set.

The characteristic of PWM switching frequency

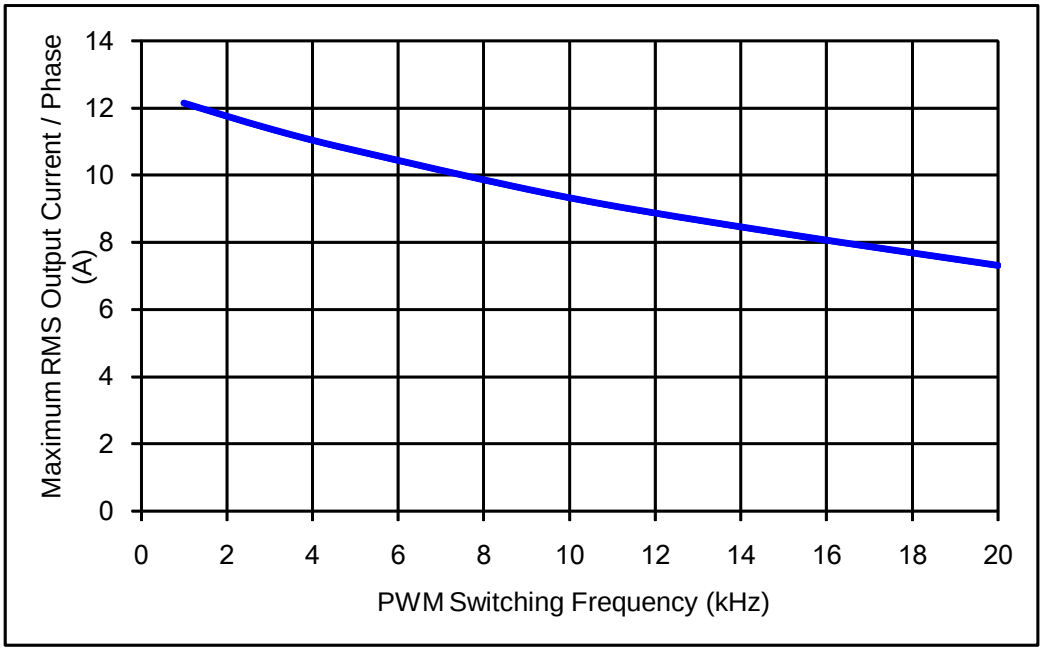


Fig. 10 Maximum sinusoidal phase current as function of switching frequency at Tc=100°C, V_{CC}=400V

Switching waveform

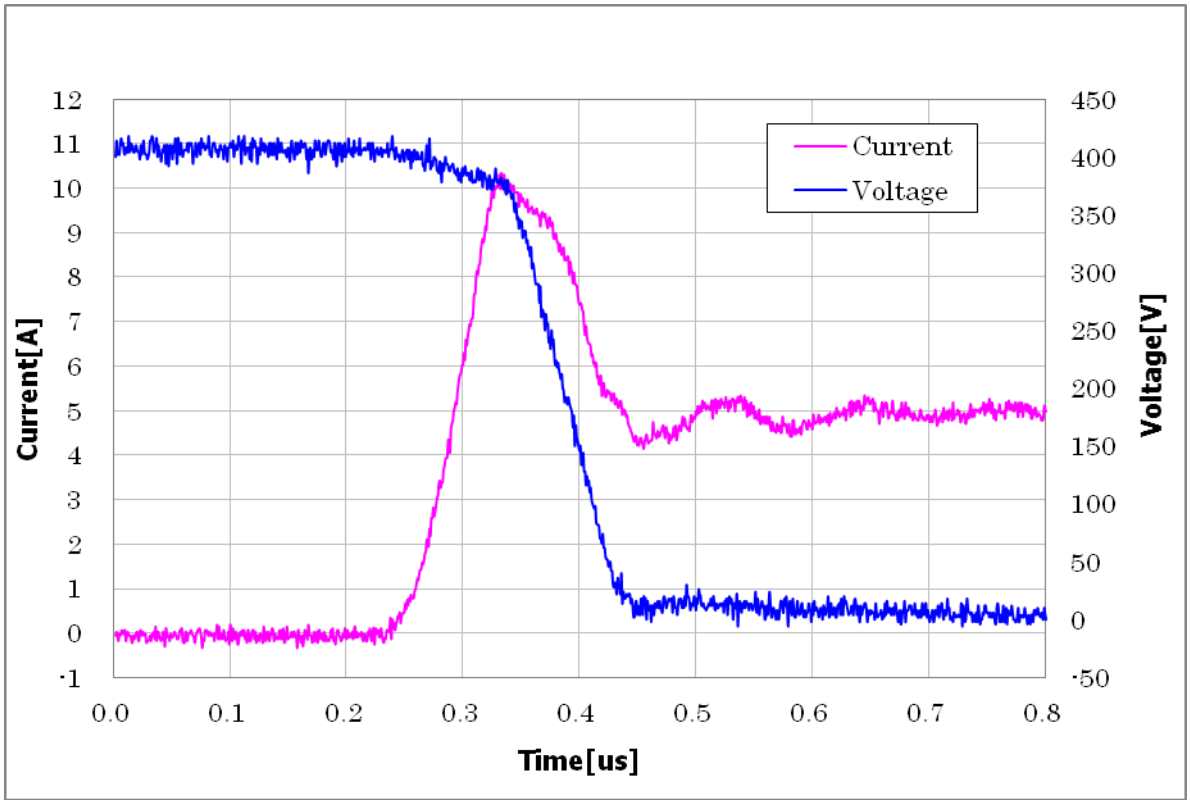


Fig. 11 IGBT Turn-on. Typical turn-on waveform at Tc=100°C, V_{CC}=400V

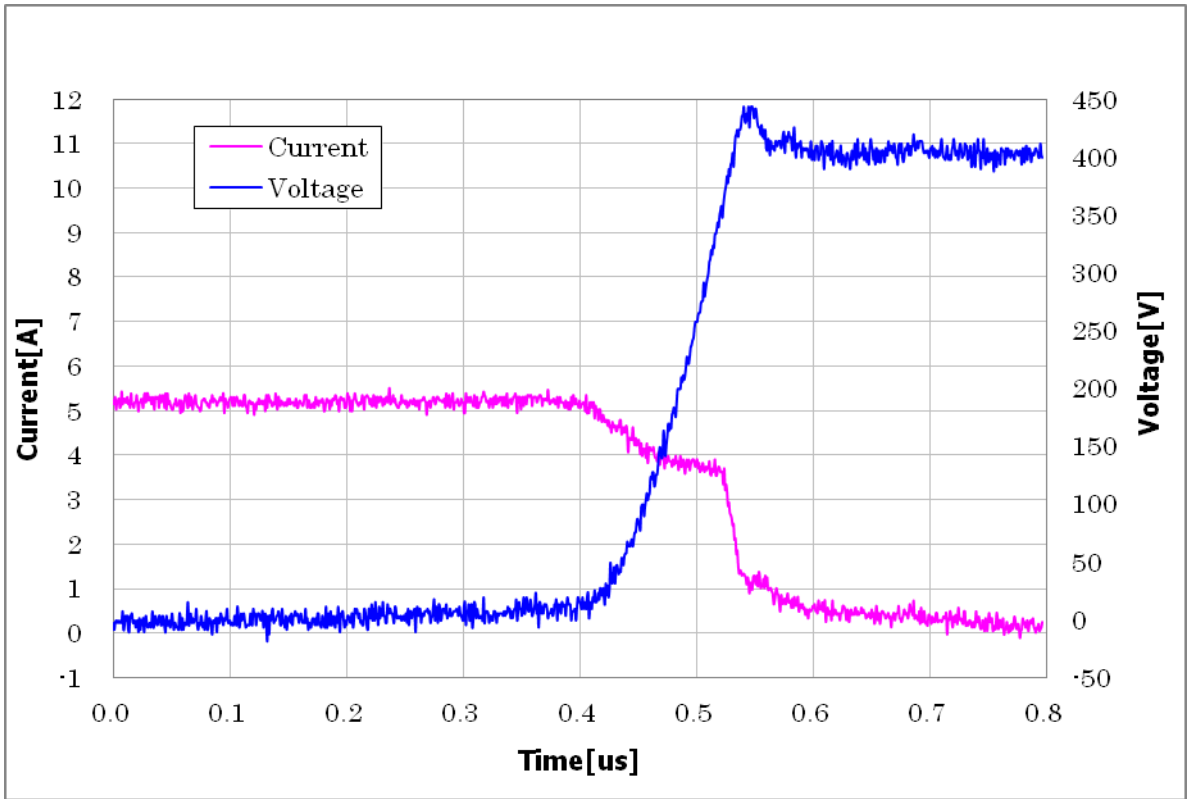


Fig. 12 IGBT Turn-off. Typical turn-off waveform at Tc=100°C, V_{CC}=400V

CB capacitor value calculation for bootstrap circuit

Calculate conditions

Parameter	Symbol	Value	Unit
Upper side power supply.	VBS	15	V
Total gate charge of output power IGBT at 15V.	QG	89	nC
Upper limit power supply low voltage protection.	UVLO	12	V
Upper side power dissipation.	IDMAX	400	μA
ON time required for CB voltage to fall from 15V to UVLO	TONMAX	-	s

Capacitance calculation formula

Thus, the following formula are true
VBS x CB - QG - IDMAX * TONMAX = UVLO * CB
therefore,
CB = (QG + IDMAX * TONMAX) / (VBS - UVLO)

The relationship between TONMAX and CB becomes as follows. CB is recommended to be approximately 3 times the value calculated above. The recommended value of CB is in the range of 1 to 47μF, however, this value needs to be verified prior to production.

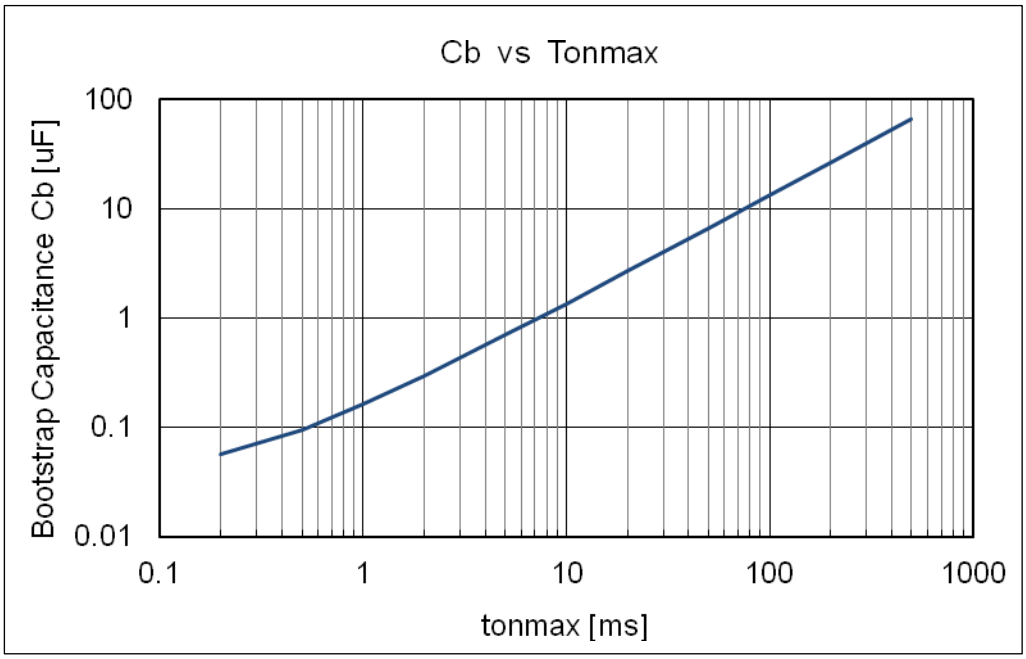


Fig. 13 TONMAX vs CB characteristic

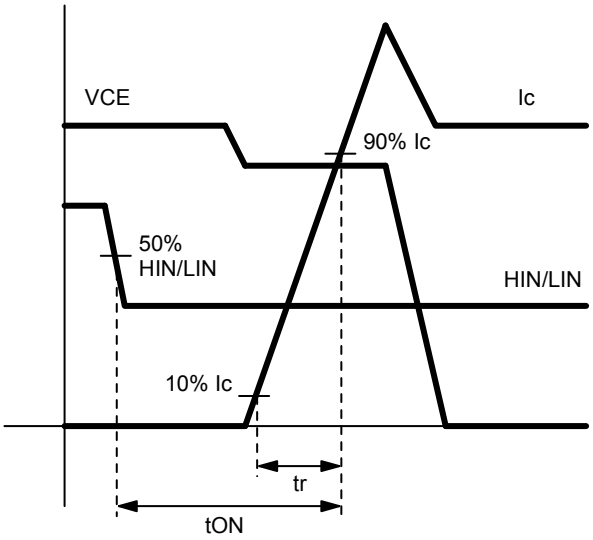


Fig. 14a Input to output propagation turn-on delay time

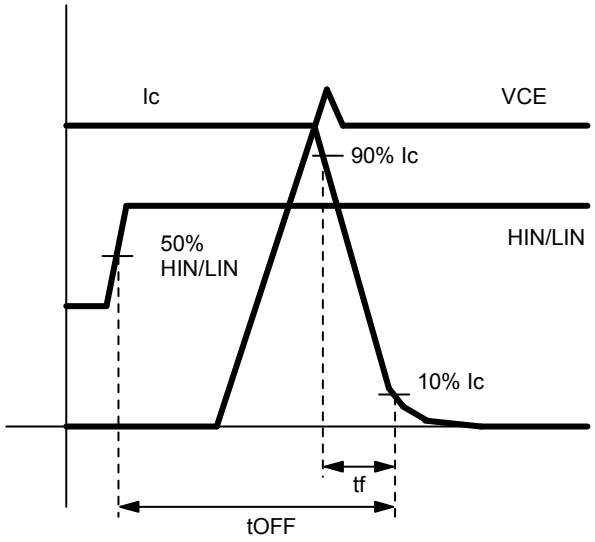


Fig. 14b Input to output propagation turn-off delay time

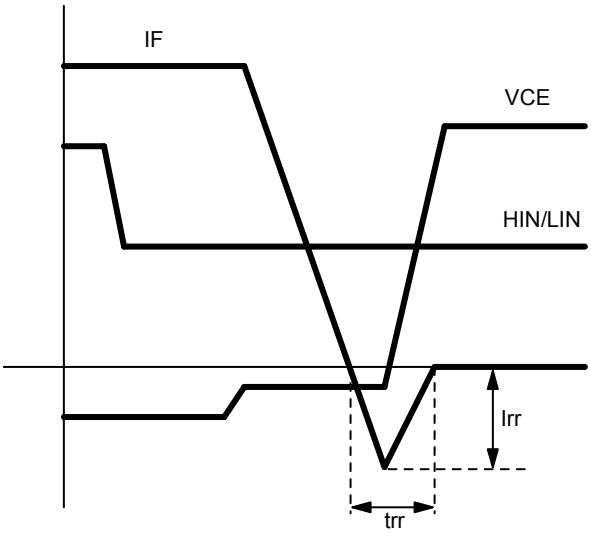
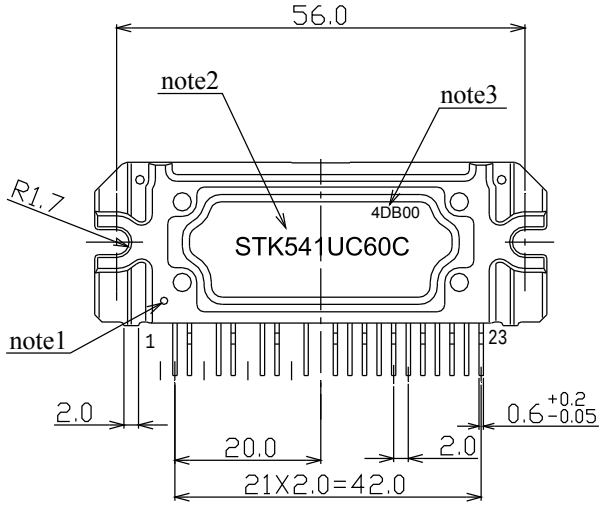


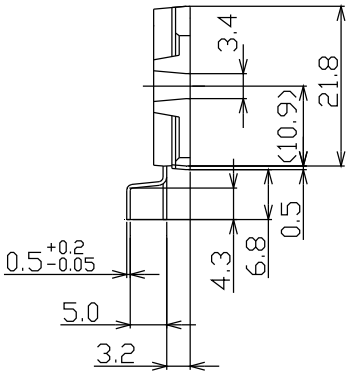
Fig. 14c Diode reverse recovery

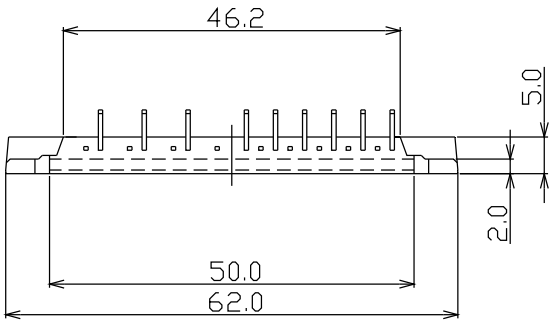
Package Dimensions

unit : mm



missing pin : 1, 4, 7, 10, 12





note1 : Mark for No.1 pin identification.
note2 : The form of a character in this drawing differs from that of IPM.
note3 : This indicates the lot code. The form of a character in this drawing differs from that of IPM.

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
STK541UC60C-E	SIP23 56x21.8 (Pb-Free)	8 / Tube

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

ON Semiconductor:

STK541UC60C-E