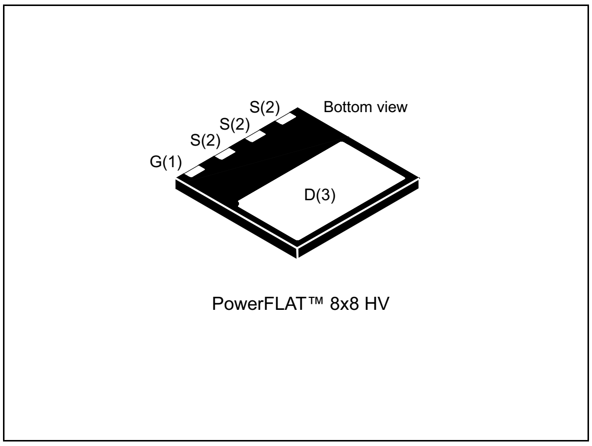
STL33N60M2

N-channel 600 V, 0.115 Ω typ., 21.5 A MDmesh II Plus™ low Q_g Power MOSFET in a PowerFLAT™ 8x8 HV package

Datasheet - preliminary data



PowerFLAT™ 8x8 HV

Features

Order code	V_{DS} @ T_{Jmax}	$R_{DS(on)max}$	I_D
STL33N60M2	650 V	0.135 Ω	21.5 A

- Extremely low gate charge
- Lower $R_{DS(on)}$ x area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using a new generation of MDmesh™ technology: MDmesh II Plus™ low Q_g. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Figure 1. Internal schematic diagram

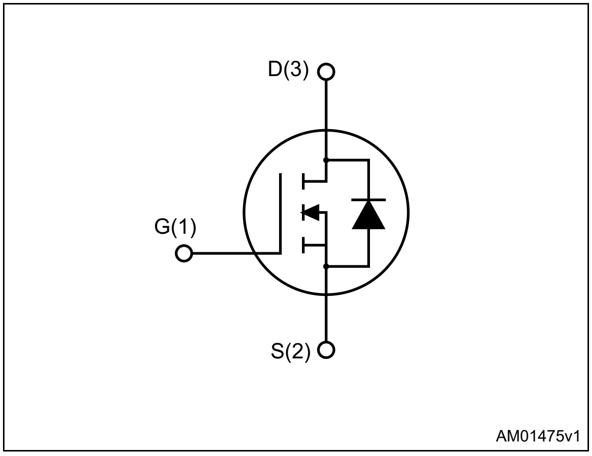


Table 1. Device summary

Order code	Marking	Package	Packaging
STL33N60M2	33N60M2	PowerFLAT™ 8x8 HV	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	21.5	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	12.5	A
I_{DM} (1),(2)	Drain current (pulsed)	86	A
I_D(3)	Drain current (continuous) at T_{amb} = 25 °C	2.9	A
I_D(3)	Drain current (continuous) at T_{amb} = 100 °C	1.8	A
P_{TOT} (3)	Total dissipation at T_{amb} = 25 °C	2.8	W
P_{TOT} (1)	Total dissipation at T_C = 25 °C	150	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	TBD	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V)	TBD	mJ
dv/dt (4)	Peak diode recovery voltage slope	15	V/ns
dv/dt (5)	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature	150	°C

1. The value is rated according to $R_{thj\text{-}case}$ and limited by package.
2. Pulse width limited by safe operating area.
3. When mounted on FR-4 board of inch², 2oz Cu.
4. $I_{SD} \leq$ 21.5 A, di/dt $\leq$ 400 A/µs, $V_{DS(peak)} < V_{(BR)DSS}$, V_{DD}=400 V
5. $V_{DS} \leq$ 480 V

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.83	°C/W
$R_{thj\text{-}amb}$(1)	Thermal resistance junction-ambient max	45	°C/W

1. When mounted on FR-4 board of inch², 2oz Cu.

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0, V_{DS} = 600 V			1	µA
		V_{GS} = 0, V_{DS} = 600 V, T_C=125 °C			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0, V_{GS} = ± 25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 10.75 A		0.115	0.135	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	1700	-	pF
C_{oss}	Output capacitance		-	120	-	pF
C_{rss}	Reverse transfer capacitance		-	3	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0	-	TBD	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	TBD	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 21.5 A, V_{GS} = 10 V (see *Figure 3*)	-	47	-	nC
Q_{gs}	Gate-source charge		-	TBD	-	nC
Q_{gd}	Gate-drain charge		-	TBD	-	nC

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 21.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 2* and *7*)	-	TBD	-	ns
t_r	Voltage rise time		-	TBD	-	ns
$t_{d(off)}$	Turn-off delay time		-	TBD	-	ns
t_f	Current fall time		-	TBD	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}(1)	Source-drain current		-		21.5	A
I_{SDM} (1),(2)	Source-drain current (pulsed)		-		TBD	A
V_{SD} (3)	Forward on voltage	I_{SD} = 21.5 A, V_{GS} = 0	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 21.5 A, di/dt = 100 A/µs V_{DD} = 100 V (see *Figure 4*)	-	TBD		ns
Q_{rr}	Reverse recovery charge		-	TBD		µC
I_{RRM}	Reverse recovery current		-	TBD		A
t_{rr}	Reverse recovery time	I_{SD} = 21.5 A, di/dt = 100 A/µs V_{DD} = 100 V, T_j = 150 °C (see *Figure 4*)	-	TBD		ns
Q_{rr}	Reverse recovery charge		-	TBD		µC
I_{RRM}	Reverse recovery current		-	TBD		A

1. The value is rated according to $R_{thj\text{-}case}$ and limited by package.
2. Pulse width limited by safe operating area
3. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

3 Test circuits

Figure 2. Switching times test circuit for resistive load

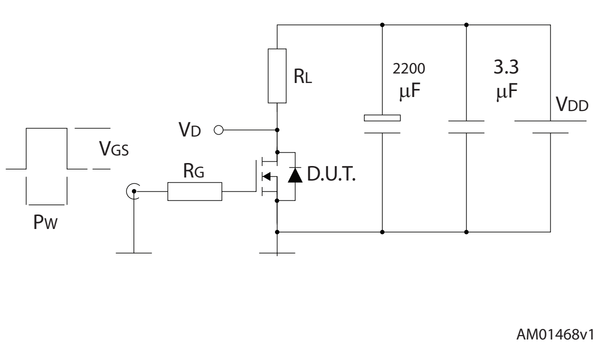


Figure 3. Gate charge test circuit

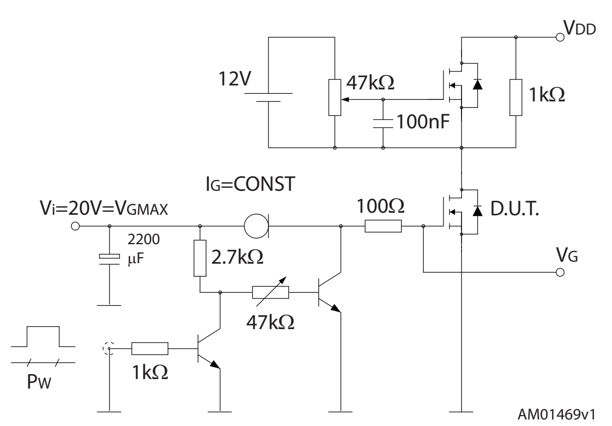


Figure 4. Test circuit for inductive load switching and diode recovery times

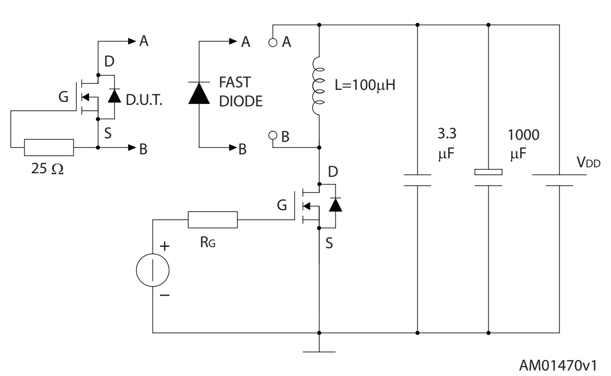


Figure 5. Unclamped inductive load test circuit

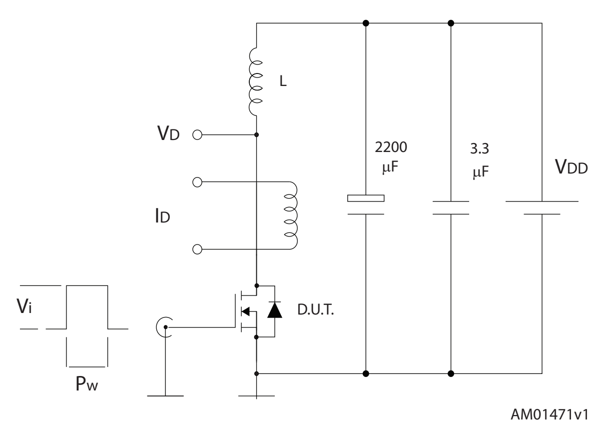


Figure 6. Unclamped inductive waveform

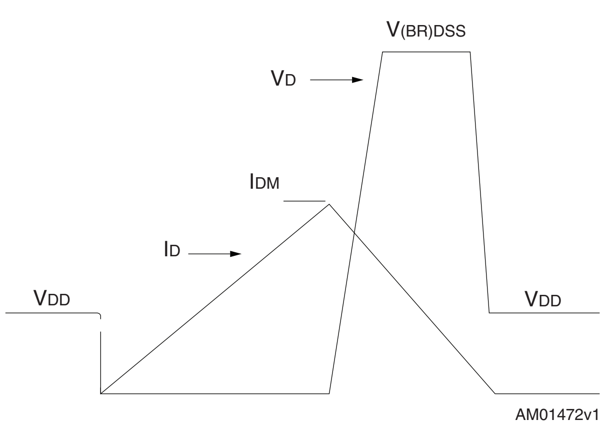
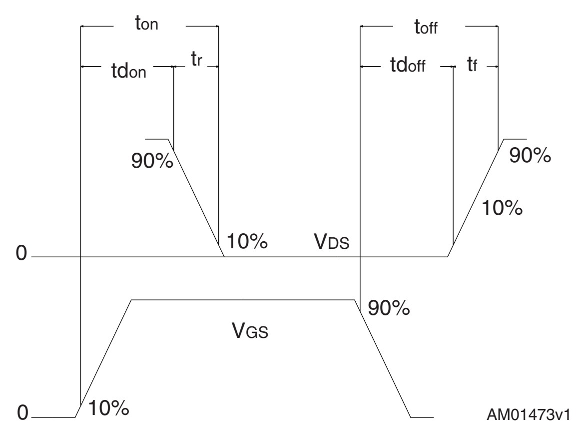


Figure 7. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 8. PowerFLAT™ 8x8 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.95	1.00	1.05
D		8.00	
E		8.00	
D2	7.05	7.20	7.30
E2	4.15	4.30	4.40
e		2.00	
L	0.40	0.50	0.60
aaa		0.10	
bbb		0.10	
ccc		0.10	

Figure 8. PowerFLAT™ 8x8 HV drawing mechanical data

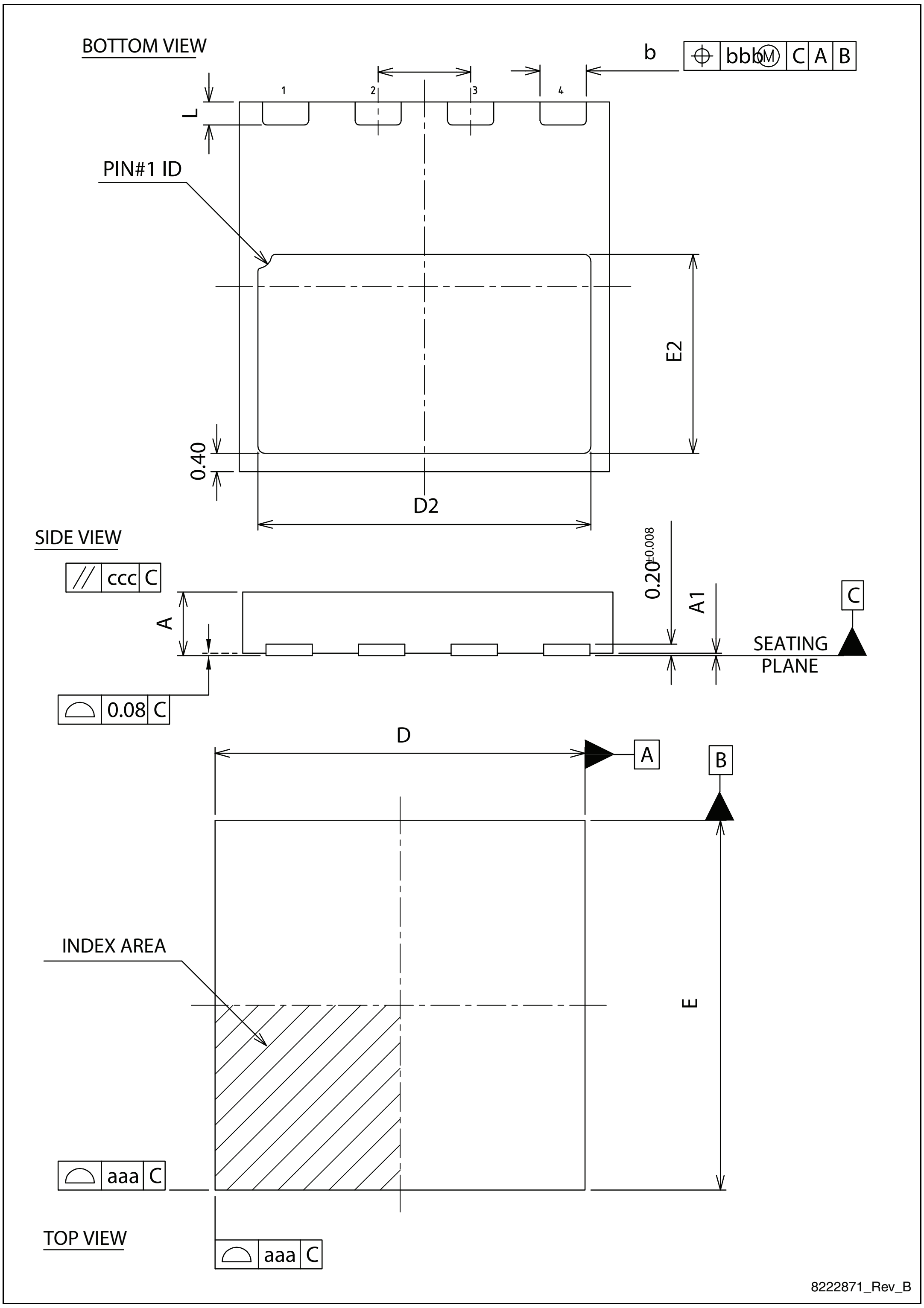
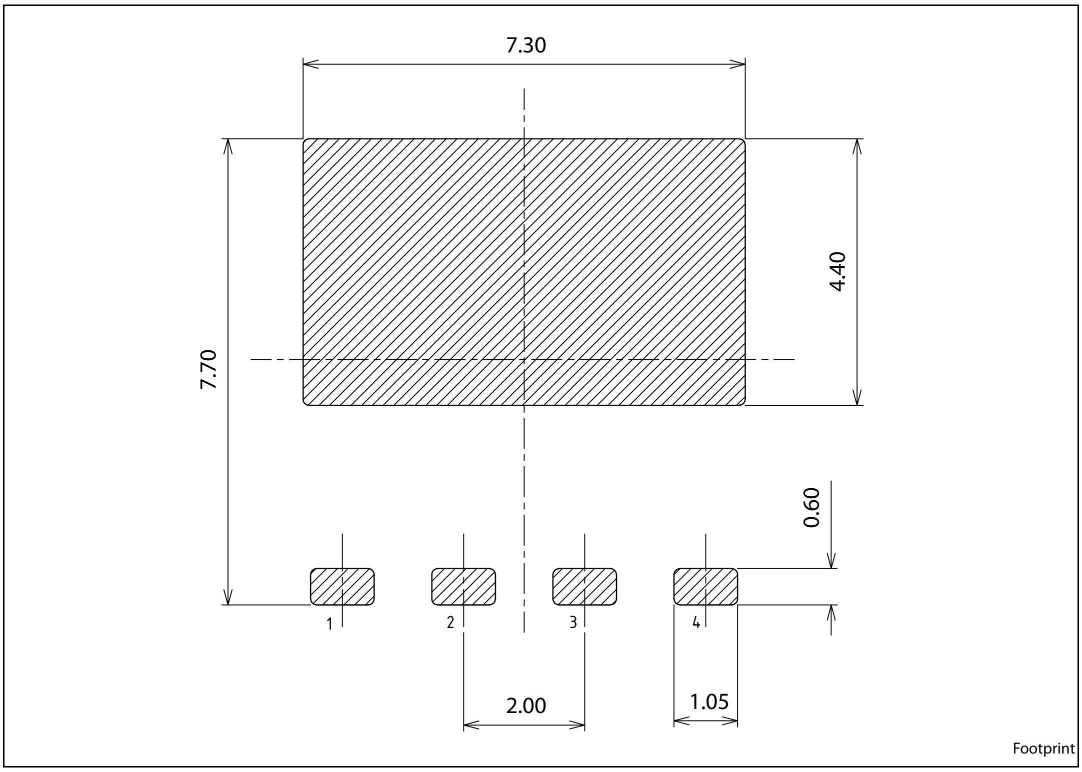
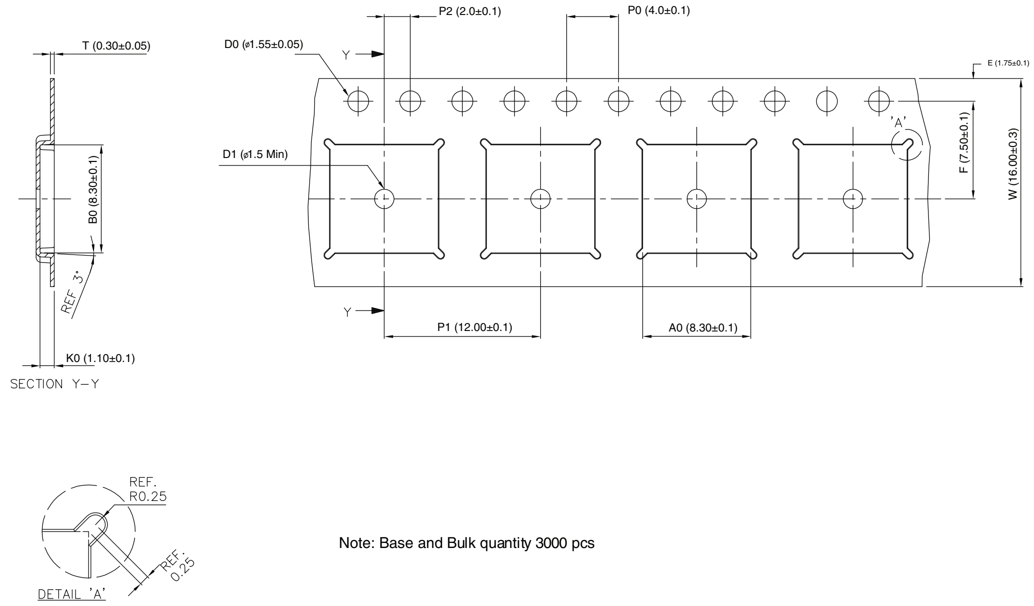


Figure 9. PowerFLAT™ 8x8 HV recommended footprint



5 Packaging mechanical data

Figure 10. PowerFLAT™ 8x8 HV tape



Note: Base and Bulk quantity 3000 pcs

8229819_Tape_revA

Figure 11. PowerFLAT™ 8x8 HV package orientation in carrier tape.

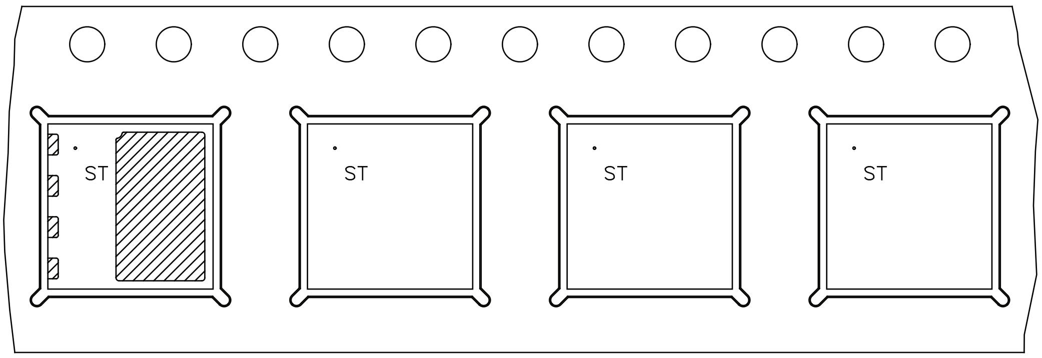
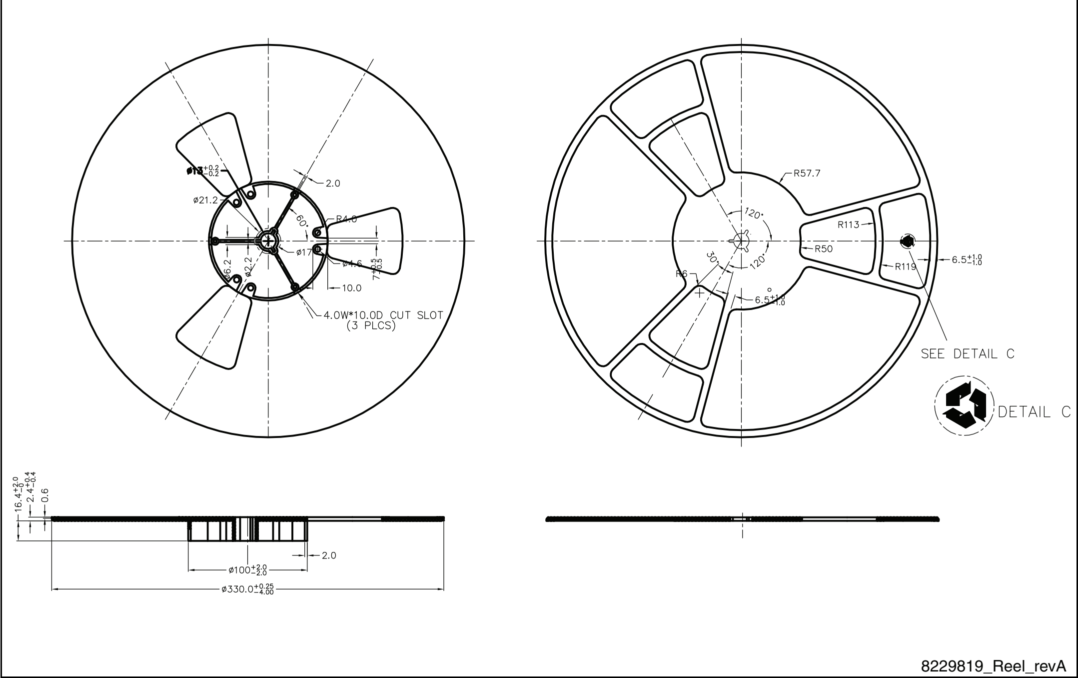


Figure 12. PowerFLAT™ 8x8 HV reel



6 Revision history

Table 9. Document revision history

Date	Revision	Changes
26-Jun-2013	1	First release.

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