

P-channel -30 V, 9 mΩ typ., -62 A STripFET™ H6 Power MOSFET in a PowerFLAT 5x6 package

Datasheet - production data

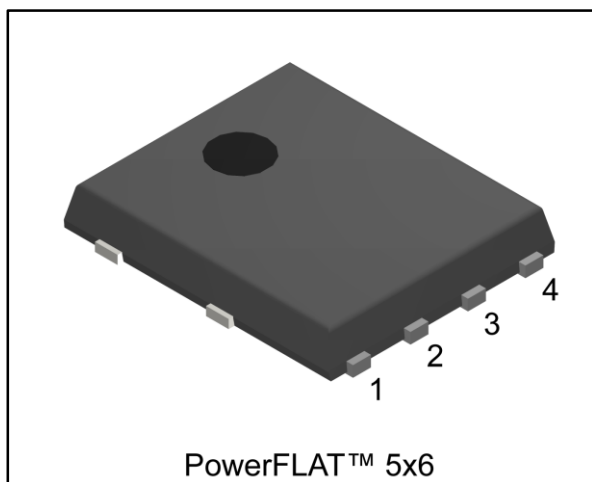
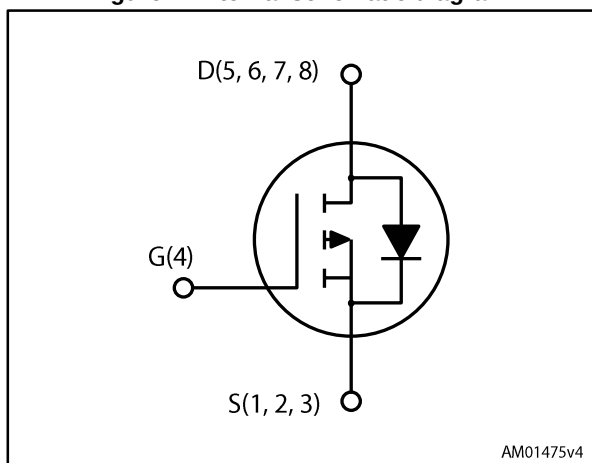


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max	I _D
STL62P3LLH6	-30 V	10.5 mΩ	-62 A

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is a P-channel Power MOSFET developed using the STripFET™ H6 technology, with a new trench gate structure. The resulting Power MOSFET exhibits very low R_{DS(on)} in all packages.

Table 1: Device summary

Order code	Marking	Package	Packing
STL62P3LLH6	62P3LLH6	PowerFLAT™ 5x6	Tape and reel

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1 Electrical ratings

Table 3: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	-62	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	-44	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^{\circ}\text{C}$	-14	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 100\text{ }^{\circ}\text{C}$	-9.5	A
$I_D^{(1)(2)}$	Drain current (pulsed)	-248	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	-56	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	100	W
$P_{TOT}^{(2)}$	Total dissipation at $T_{pcb} = 25\text{ }^{\circ}\text{C}$	4.8	W
T_{stg}	Storage temperature range	- 55 to 175	$^{\circ}\text{C}$
T_j	Operating junction temperature range		

Notes:

⁽¹⁾The value is rated according to R_{thj-c} .

⁽²⁾This value is rated according to $R_{thj-pcb}$.

⁽³⁾Pulse width is limited by safe operating area.

Table 4: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.5	$^{\circ}\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb, single operation	31.3	$^{\circ}\text{C/W}$

Notes:

⁽¹⁾When mounted on FR-4 board of 1inch², 2oz Cu

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V, I _D = -250 µA	-30			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = -30 V			-1	µA
		V _{GS} = 0 V, V _{DS} = -30 V, T _C = 125 °C ⁽¹⁾			-10	µA
I _{GSS}	Gate-body leakage current	V _{DS} = 0 V, V _{GS} = ± 20 V			±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = -250 µA	-1			V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = -10 V, I _D = -7 A		9	10.5	mΩ
		V _{GS} = -4.5 V, I _D = -7 A		13	16	mΩ

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = -25 V, f = 1 MHz, V _{GS} = 0 V	-	3350	-	pF
C _{oss}	Output capacitance		-	414	-	pF
C _{rss}	Reverse transfer capacitance		-	287	-	pF
Q _g	Total gate charge	V _{DD} = -15 V, I _D = -14 A, V _{GS} = -4.5 V (see Figure 14: "Gate charge test circuit")	-	33	-	nC
Q _{gs}	Gate-source charge		-	14	-	nC
Q _{gd}	Gate-drain charge		-	11	-	nC

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = -15 V, I _D = -7 A, R _G = 4.7 Ω, V _{GS} = -10 V (see Figure 13: "Switching times test circuit for resistive load")	-	12.8	-	ns
t _r	Rise time		-	112	-	ns
t _{d(off)}	Turn-off delay time		-	61	-	ns
t _f	Fall time		-	45	-	ns

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = -7\text{ A}$, $V_{GS} = 0\text{ V}$	-		-1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = -24\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = -16\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 15: "Source-drain diode forward characteristics")	-	25.2		ns
Q_{rr}	Reverse recovery charge		-	17.4		nC
I_{RRM}	Reverse recovery current		-	1.4		A

Notes:

⁽¹⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)



Note: For the P-channel Power MOSFET, current and voltage polarities are reversed.

Figure 2: Safe operating area

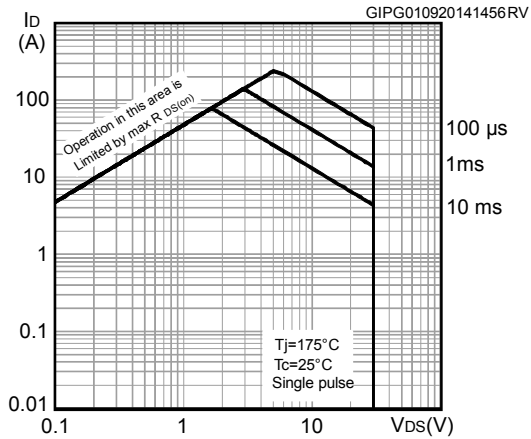


Figure 3: Thermal impedance

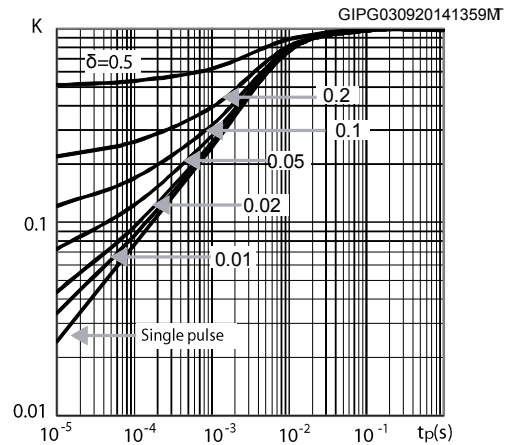


Figure 4: Output characteristics

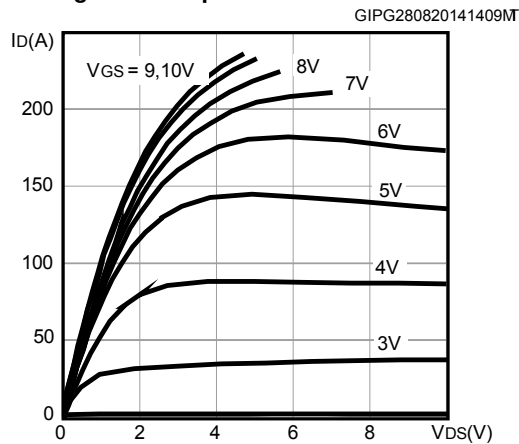


Figure 5: Transfer characteristics

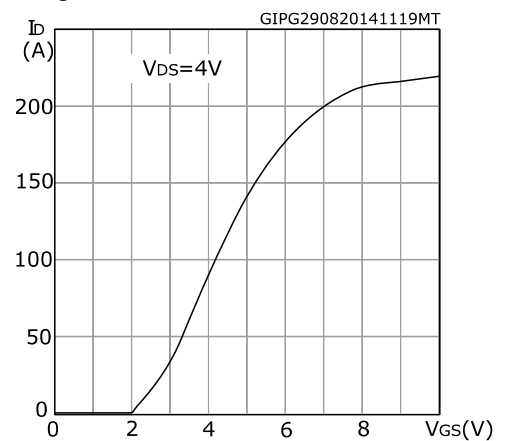


Figure 6: Gate charge vs gate-source voltage

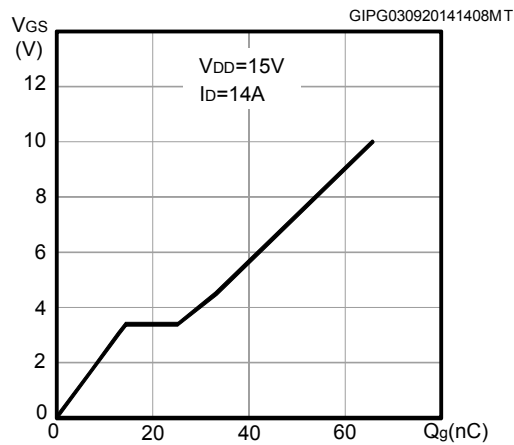


Figure 7: Static drain-source on-resistance

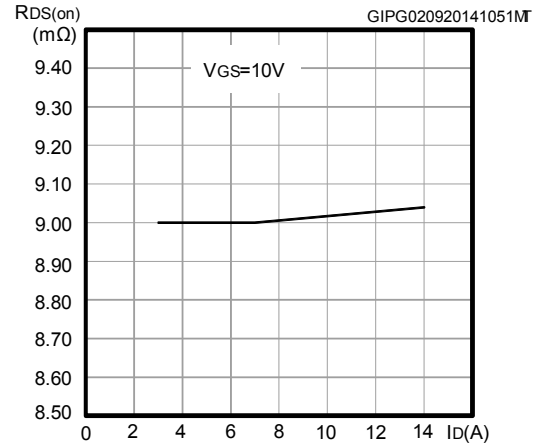


Figure 8: Capacitance variations

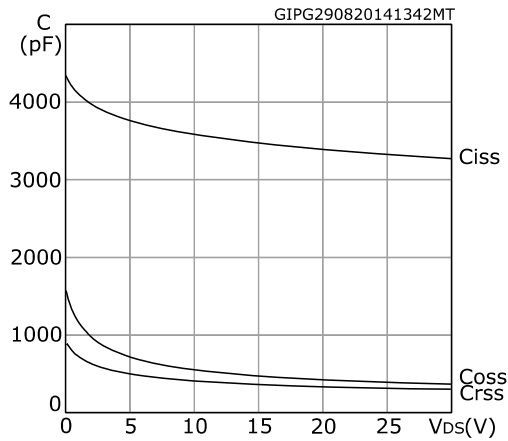


Figure 9: Normalized gate threshold voltage vs temperature

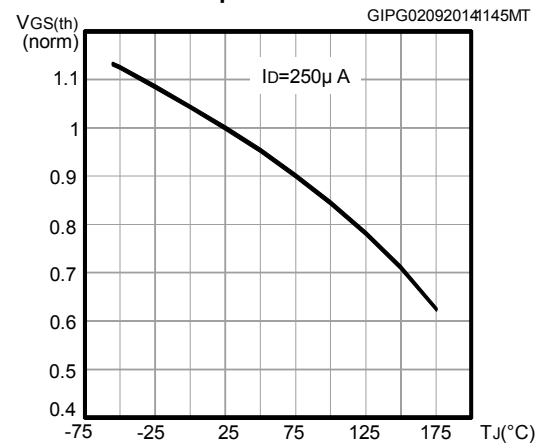


Figure 10: Normalized on-resistance vs temperature

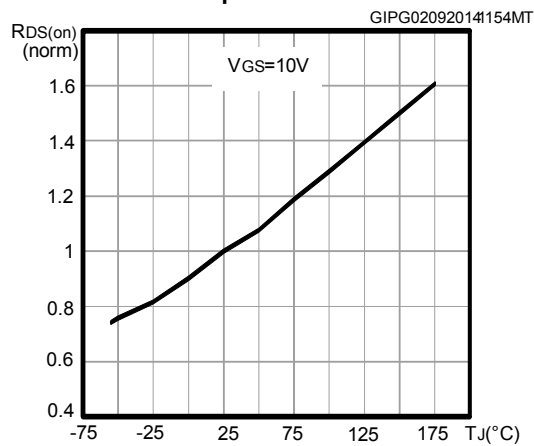


Figure 11: Normalized V(BR)DSS vs temperature

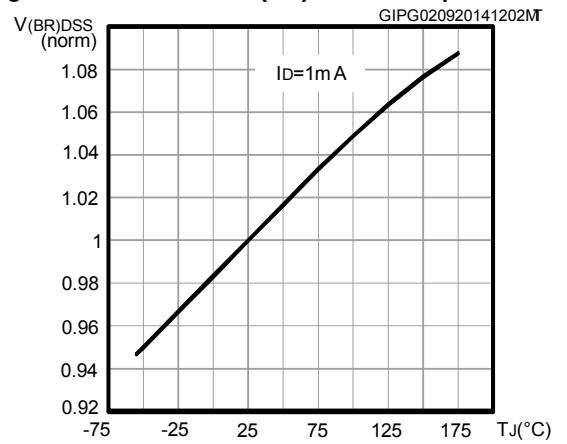
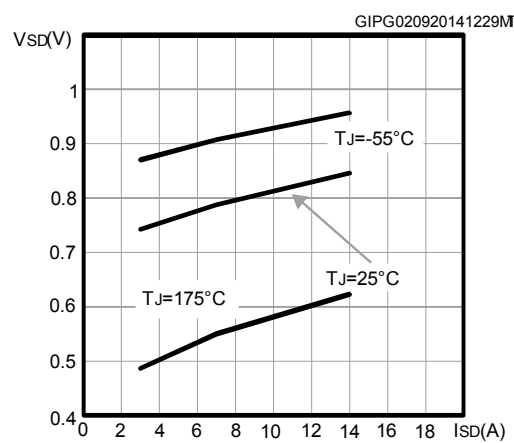


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Switching times test circuit for resistive load

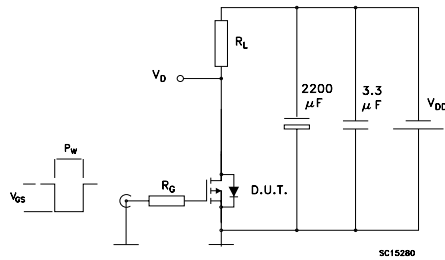


Figure 14: Gate charge test circuit

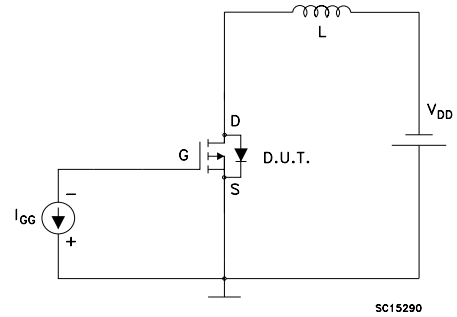
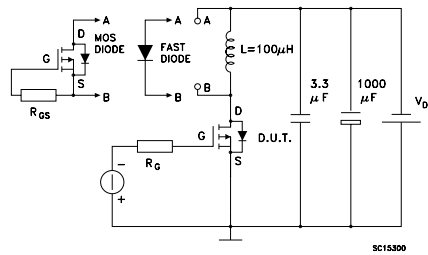


Figure 15: Source-drain diode forward characteristics



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

4.1 PowerFLAT 5x6 type R package information

Figure 16: PowerFLAT™ 5x6 type R package outline

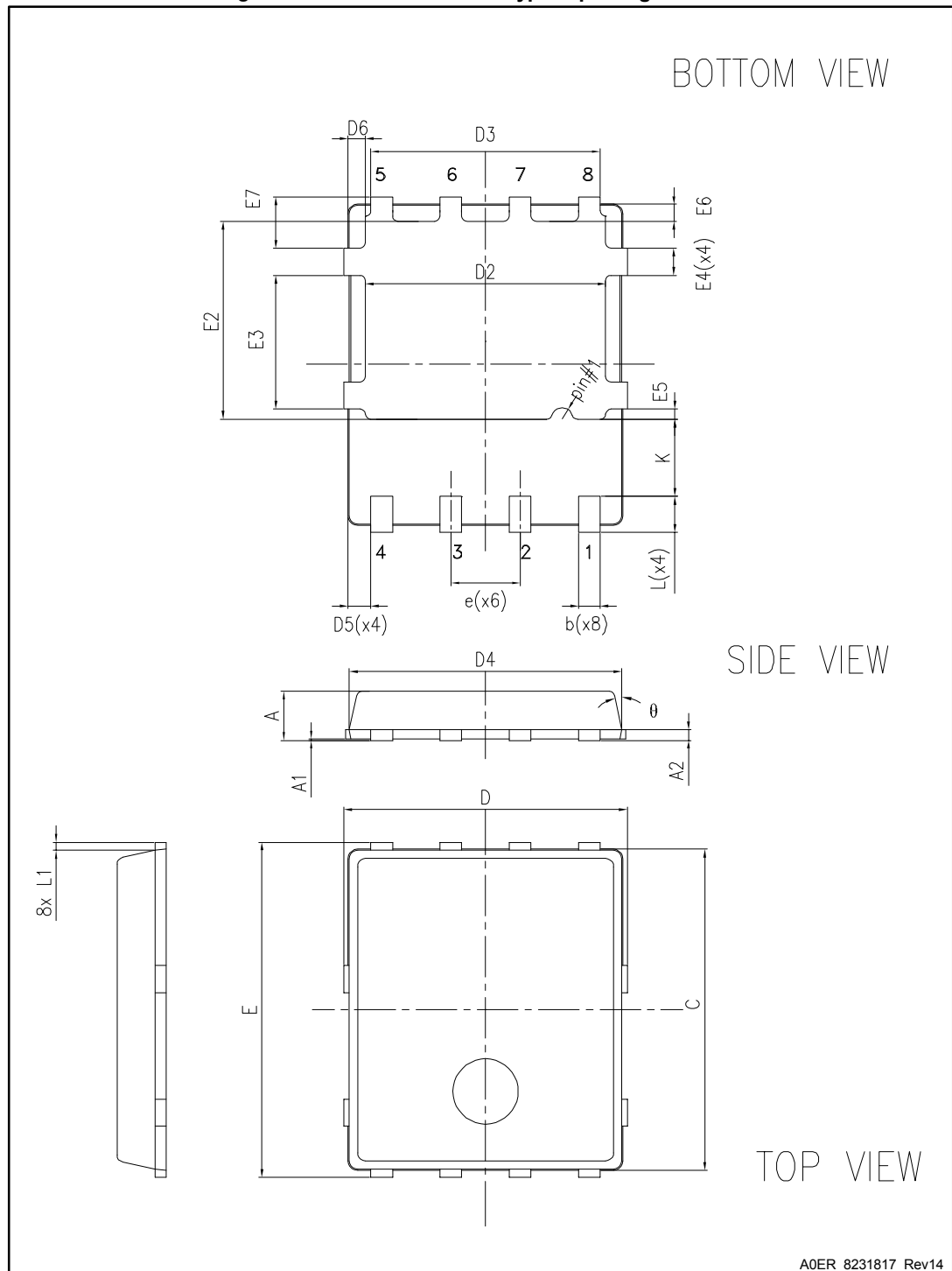
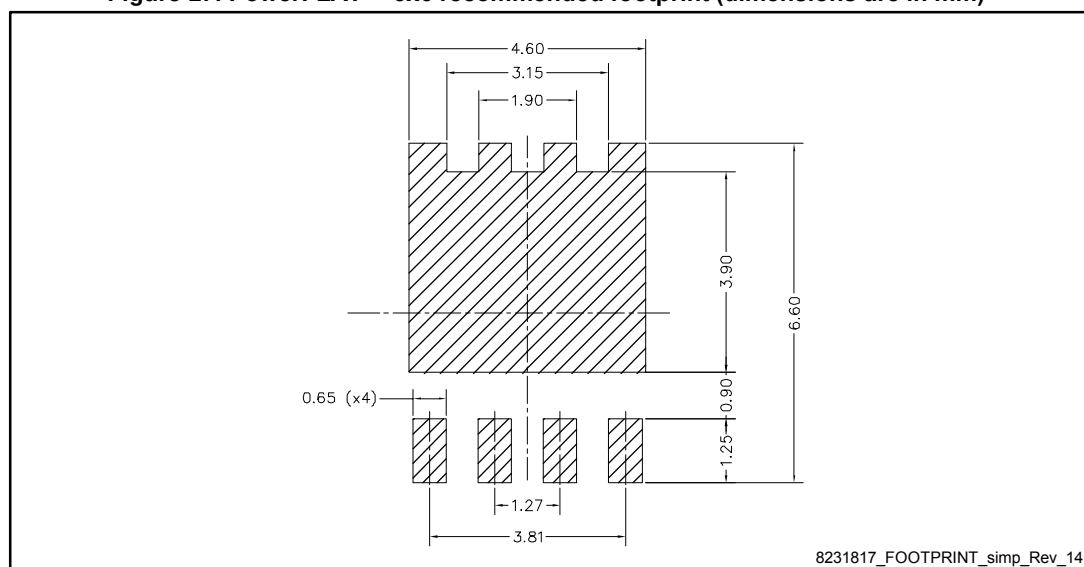


Table 9: PowerFLAT™ 5x6 type R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.20
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.20
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
e		1.27	
E	5.95	6.15	6.35
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.75	0.90	1.05
K	1.275		1.575
L	0.60		0.80
L1	0.05	0.15	0.25
θ		0°	12°

Figure 17: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



5 Packing information

Figure 18: PowerFLAT™ 5x6 tape (dimensions are in mm)

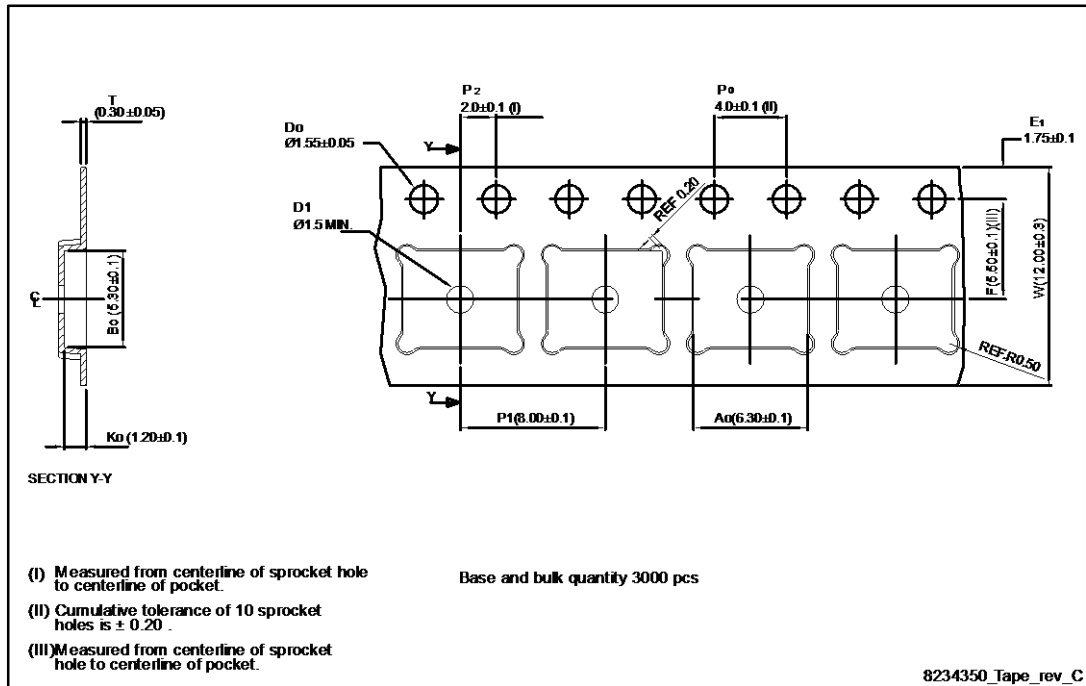


Figure 19: PowerFLAT™ 5x6 package orientation in carrier tape

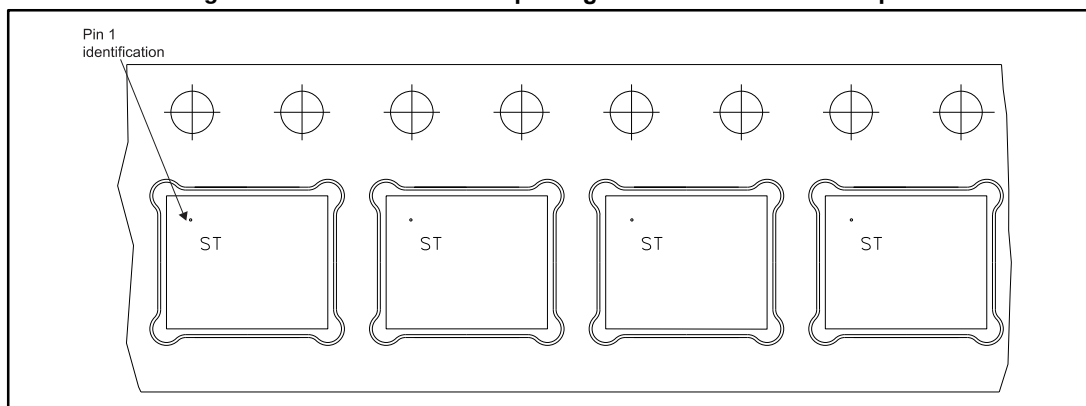
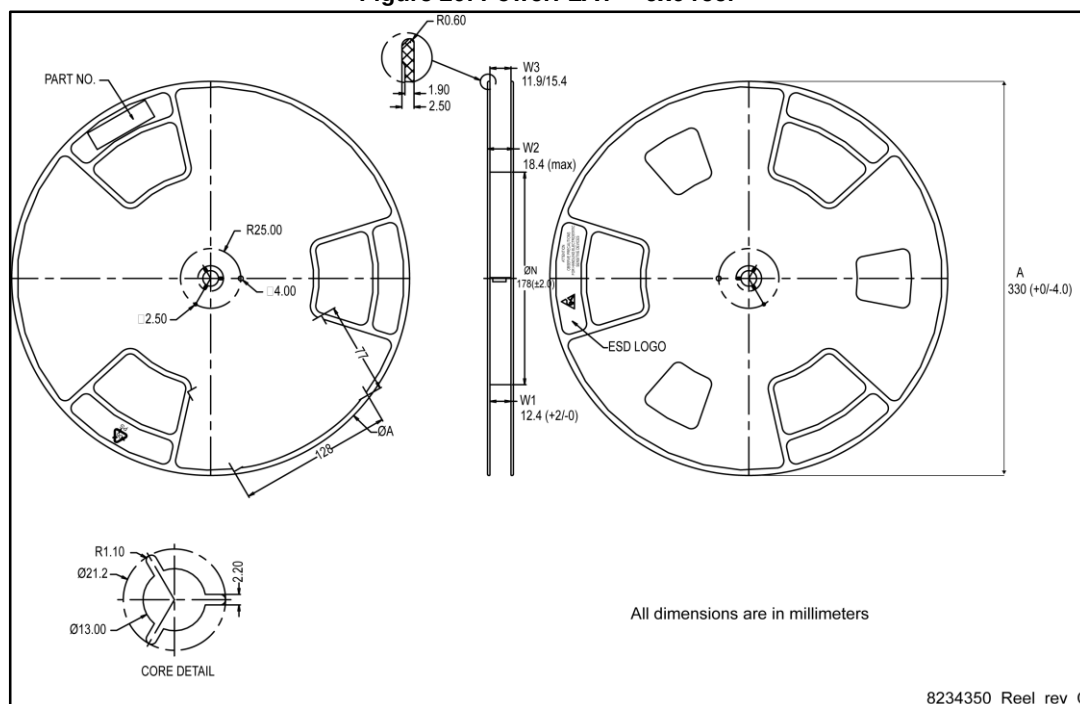


Figure 20: PowerFLAT™ 5x6 reel



6 Revision history

Table 10: Document revision history

Date	Revision	Changes
30-May-2014	1	First release.
05-Sep-2014	2	Updated the title, the features and the description in cover page. Updated Section 7: " <i>Electrical characteristics</i> ". Minor text changes.
11-Sep-2014	3	Updated Figure 6: " <i>Gate charge vs gate-source voltage</i> ". Minor text changes.
16-Dec-2014	4	Document status promoted from preliminary to production data.
07-Apr-2015	5	Updated Section 7.1: " <i>Electrical characteristics (curves)</i> " and Section 9.1: " <i>PowerFLAT 5x6 type R package information</i> "
20-Oct-2016	6	Updated Figure 2: "Safe operating area" . Minor text changes.

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