STL8P2UH7

P-channel 20 V, 0.0146 Ω typ., 8 A STripFET™ VII DeepGATE™ Power MOSFET in a PowerFLAT™ 2x2 package

Datasheet - target specification

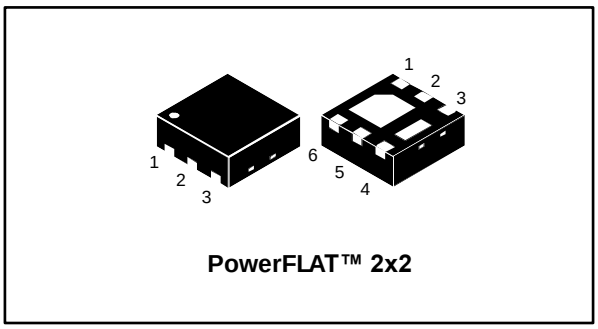
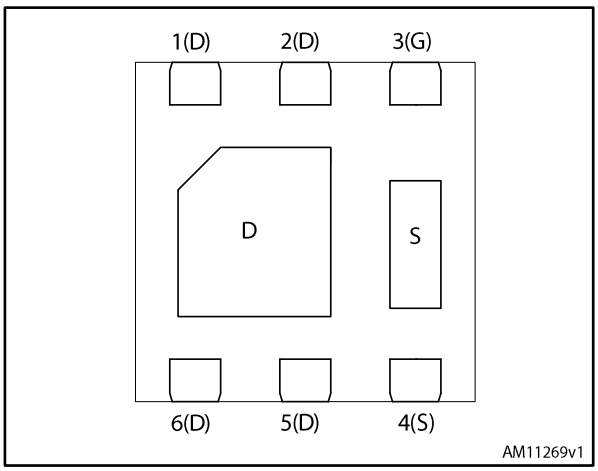


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$max	I_D
STL8P2UH7	20 V	0.018 Ω @ 4.5 V	8 A

- Extremely low on-resistance $R_{DS(on)}$
- Ultra logic level

Applications

- Switching applications

Description

This device exhibits low on-state resistance and capacitance for improved conduction and switching performance.

Table 1: Device summary

Order code	Marking	Package	Packaging
STL8P2UH7	8L2U	PowerFLAT™2x2	Tape and reel

For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	± 8	V
I_D (1)	Drain current (continuous) at T_{pcb} = 25 °C	8	A
I_D (1)	Drain current (continuous) at T_{pcb} = 100 °C	5.3	A
I_{DM}	Drain current (pulsed)	32	A
P_{TOT} (2)	Total dissipation at T_{pcb} = 25 °C	2.4	Ω
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature	150	°C

Notes:

(1)The value is rated according to Rthj-pcb

(2)Pulse width limited by safe operating area

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb max	52	°C/W

Notes:

(1)When mounted on 1inch² FR-4 board, 2 oz Cu

For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS} = 0	20			V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 30 V, V_{GS} = 0			1	µA
I_{GSS}	Gate-body leakage current	V_{GS} = ± 8 V, V_{DS} = 0			1	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	0.4		1	V
$R_{DS(on)}$	Static drain-source on- resistance	V_{GS} = 4.5 V, I_D = 4 A		0.0146	0.018	Ω
		V_{GS} = 2.5 V, I_D = 4 A		0.019	0.025	Ω
		V_{GS} = 1.8 V, I_D = 4 A		0.025	0.050	Ω
		V_{GS} = 1.5 V, I_D = 4 A		0.04	0.09	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 15 V, f = 1 MHz, V_{GS} = 0	-	2240	-	pF
C_{oss}	Output capacitance		-	240	-	pF
C_{rss}	Reverse transfer capacitance		-	210	-	pF
Q_g	Total gate charge	V_{DD} = 15 V, I_D = 6 A, V_{GS} = 4.5 V	-	28	-	nC
Q_{gs}	Gate-source charge		-	TBD	-	nC
Q_{gd}	Gate-drain charge		-	TBD	-	nC

For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 15 V, I_D = 8 A, R_G = 1 Ω, V_{GS} = 4.5 V	-	TBD	-	ns
t_r	Rise time		-	TBD	-	ns
$t_{d(off)}$	Turn-off delay time		-	TBD	-	ns
t_f	Fall time		-	TBD	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	-	8	A
I_{SDM} (1)	Source-drain current (pulsed)		-	-	32	A
V_{SD} (2)	Forward on voltage	I_{SD} = 1 A, $V_{G\,S}$= 0	-	-	1	V
t_{rr}	Reverse recovery time	V_{DD} = 16 V di/dt = 100 A/µs, I_{SD} = 1 A T_j = 150 °C	-	TBD		ns
Q_{rr}	Reverse recovery charge		-	TBD		nC
I_{RRM}	Reverse recovery current		-	TBD		A

Notes:

(1)Pulse width limited by safe operating area.

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

3 Test circuits

Figure 2: Switching times test circuit for resistive load

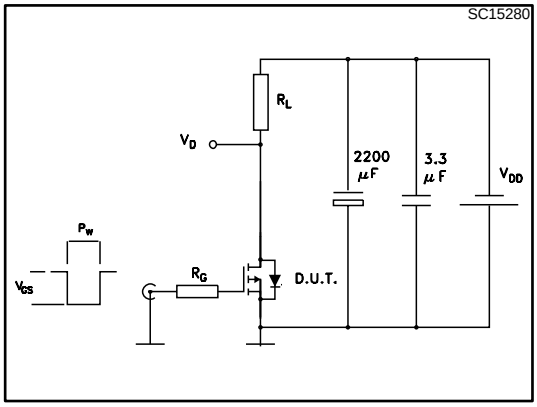


Figure 3: Gate charge test circuit

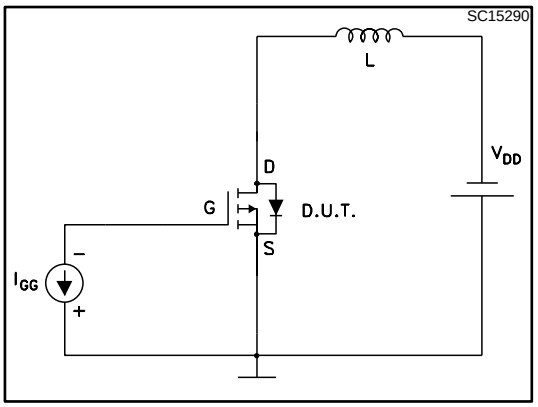
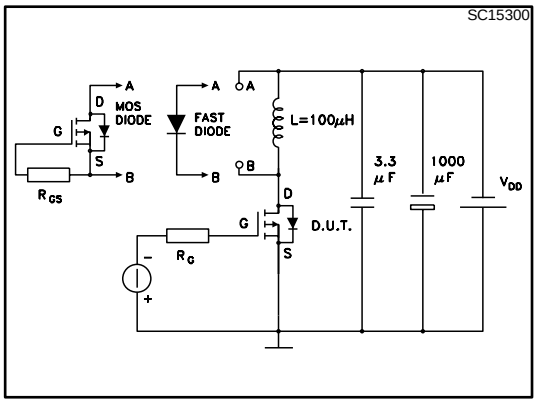


Figure 4: Test circuit for inductive load switching and diode recovery times



4 Package mechanical data

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4.1 PowerFLAT™ 2x2 package mechanical data

Table 8: PowerFLAT™ 2 x 2 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20	
b	0.25	0.30	0.35
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D2	0.90	1.00	1.10
E2	0.80	0.90	1.00
e	0.55	0.65	0.75
K	0.15	0.25	0.35
K1	0.20	0.30	0.40
K2	0.25	0.35	0.45
L	0.20	0.25	0.30
L1	0.65	0.75	0.85

Figure 5: Drawing dimension PowerFLAT™ 2 x 2

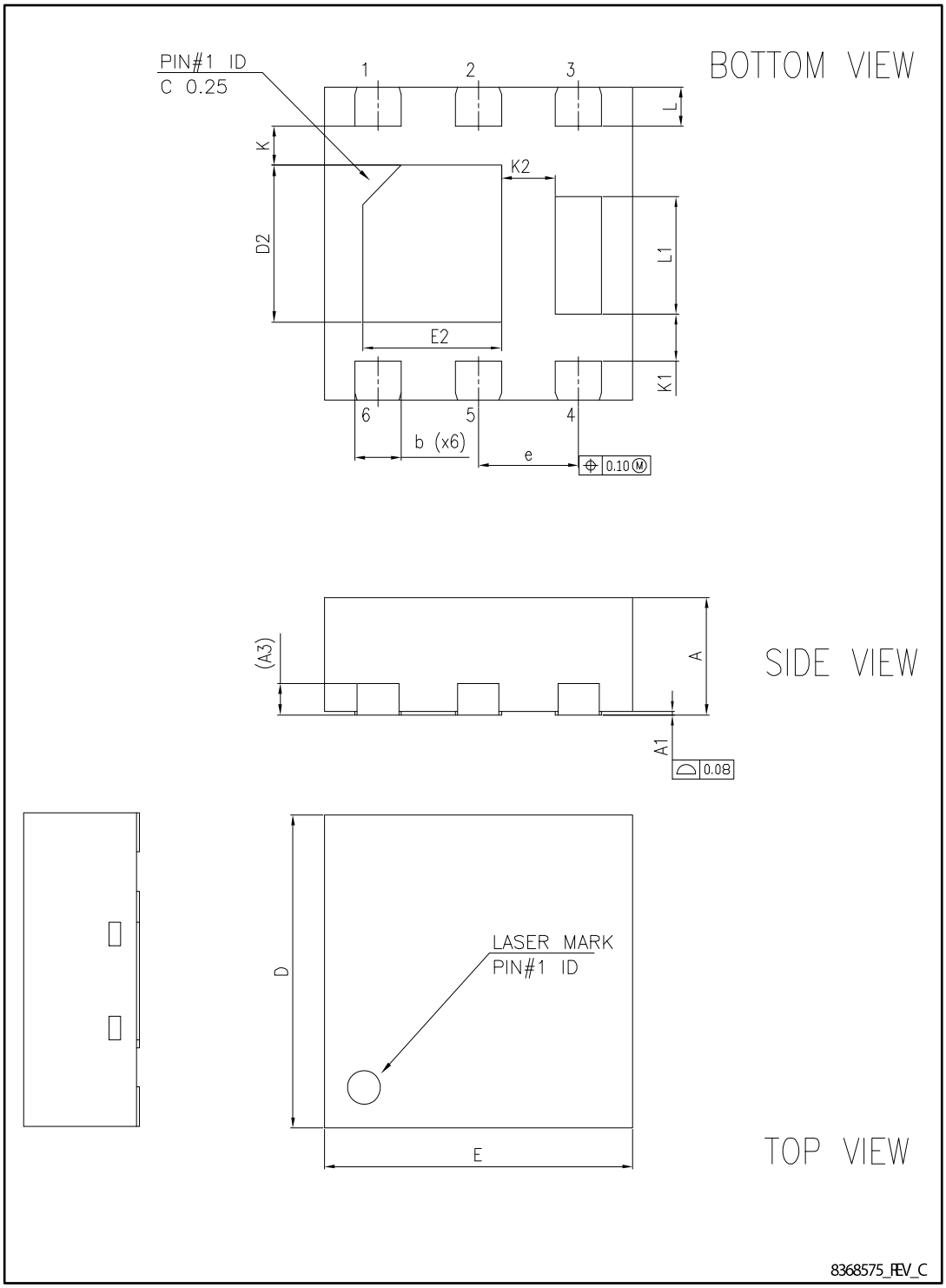
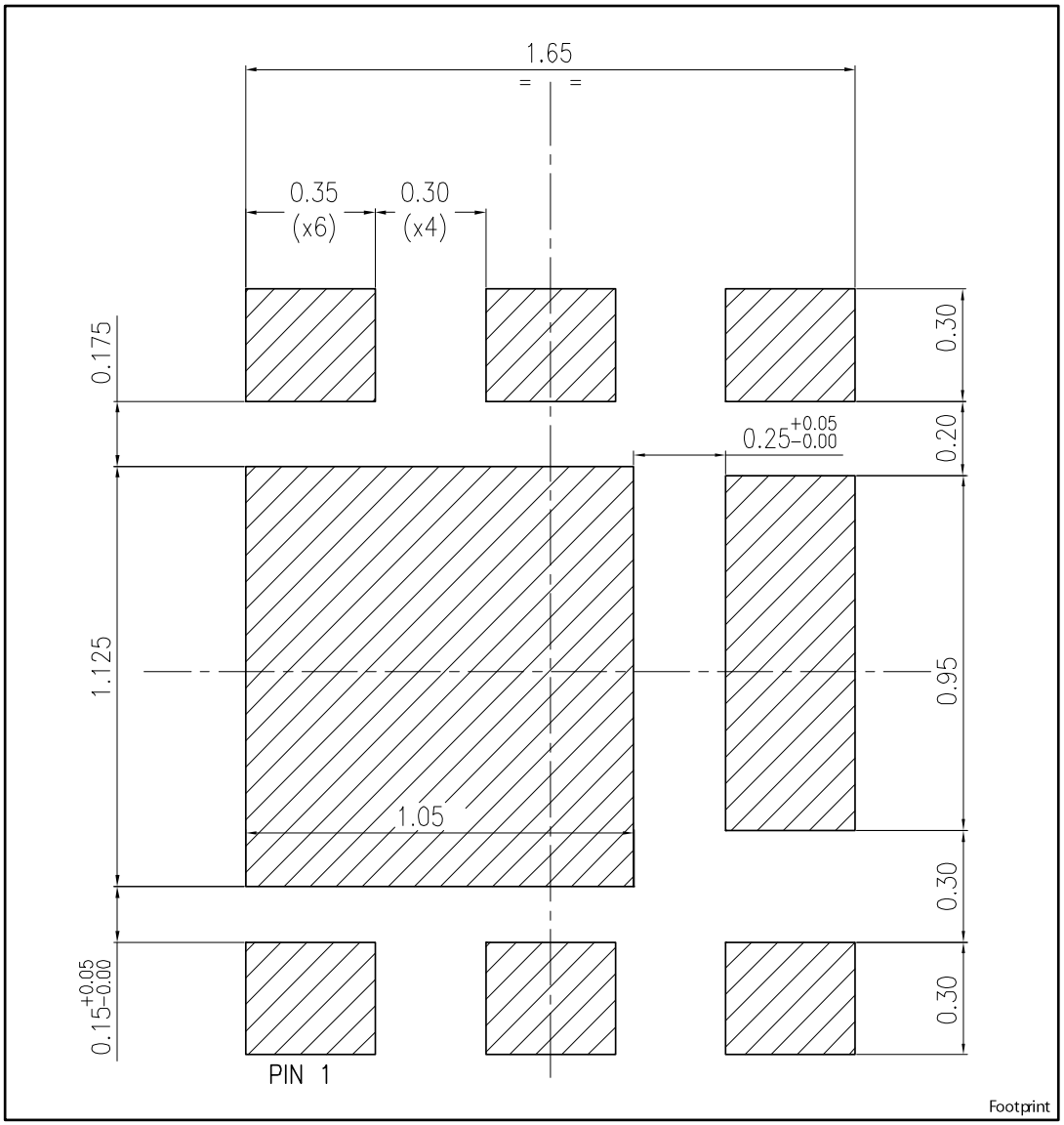


Figure 6: PowerFLAT™ 2 x 2 footprint



5 Revision history

Table 9: Document revision history

Date	Revision	Changes
09-Oct-2013	1	First release.

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