

ARM<sup>®</sup>-based Cortex<sup>®</sup>-M4 32b MCU+FPU, up to 256KB Flash+  
48KB SRAM, 4 ADCs, 2 DAC ch., 7 comp., 4 PGA, timers, 1.8 V

Datasheet - production data

## Features

- Core: ARM<sup>®</sup> Cortex<sup>®</sup>-M4 32-bit CPU with FPU (72 MHz max), single-cycle multiplication and HW division, 90 DMIPS (from CCM), DSP instruction and MPU (memory protection unit).
- Operating conditions:
  - VDD: 1.8V +/- 8%
  - VDDA voltage range: 1.65 to 3.6 V
- Memories
  - 256 Kbytes of Flash memory
  - Up to 40 Kbytes of SRAM, with HW parity check implemented on the first 16 Kbytes.
  - Routine bootster: 8 Kbytes of SRAM on instruction and data bus, with HW parity check (CCM: Core Coupled Memory)
- CRC calculation unit
- Reset and supply management
  - Low-power modes: Sleep, and Stop
  - VBAT supply for RTC and backup registers
- Clock management
  - 4 to 32 MHz crystal oscillator
  - 32 kHz oscillator for RTC with calibration
  - Internal 8 MHz RC with x 16 PLL option
  - Internal 40 kHz oscillator
- Up to 86 fast I/Os
  - All mappable on external interrupt vectors
  - Several 5 V-tolerant
- Interconnect matrix
- 12-channel DMA controller
- Up to four ADC 0.20  $\mu$ S (up to 38 channels) with selectable resolution of 12/10/8/6 bits, 0 to 3.6 V conversion range, separate analog supply from 1.8 to 3.6 V
- Up to two 12-bit DAC channels with analog supply from 2.4 to 3.6 V
- Seven fast rail-to-rail analog comparators with analog supply from 1.65 to 3.6 V
- Up to four operational amplifiers that can be used in PGA mode, all terminal accessible with analog supply from 2.4 to 3.6 V

LQFP48 (7 × 7 mm)  
LQFP64 (10 × 10 mm)  
LQFP100 (14 × 14 mm)



- Up to 24 capacitive sensing channels supporting touchkey, linear and rotary touch sensors
- Up to 13 timers
  - One 32-bit timer and two 16-bit timers with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
  - Up to two 16-bit 6-channel advanced-control timers, with up to 6 PWM channels, deadtime generation and emergency stop
  - One 16-bit timer with 2 IC/OCs, 1 OCN/PWM, deadtime generation and emergency stop
  - Two 16-bit timers with IC/OC/OCN/PWM, deadtime generation and emergency stop
  - 2 watchdog timers (independent, window)
  - SysTick timer: 24-bit downcounter
  - Up to two 16-bit basic timers to drive the DAC
- Calendar RTC with Alarm, periodic wakeup from Stop
- Communication interfaces
  - CAN interface (2.0B Active)
  - Two I2C Fast mode plus (1 Mbit/s) with 20 mA current sink, SMBus/PMBus, wakeup from STOP
  - Up to five USART/UARTs (ISO 7816 interface, LIN, IrDA, modem control)
  - Up to three SPIs, two with multiplexed I2S interface, 4 to 16 programmable bit frames
  - Infrared Transmitter
- Cortex<sup>®</sup>-M4 with FPU ETM, Serial wire debug, JTAG
- 96-bit unique ID

Table 1. Device summary

| Reference   | Part number                           |
|-------------|---------------------------------------|
| STM32F358xC | STM32F358CC, STM32F358RC, STM32F358VC |

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# 1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F358xC microcontrollers.

This STM32F358xC datasheet should be read in conjunction with the STM32F303xx, STM32F358xC and STM32F328x4/6/8 (RM0316) reference manual. The reference manual is available from the STMicroelectronics website [www.st.com](http://www.st.com).

For information on the Cortex®-M4 core with FPU please refer to:

- **Cortex®-M4 with FPU Technical Reference Manual**, available from ARM website [www.arm.com](http://www.arm.com).
- **STM32F3xxx and STM32F4xxx Cortex®-M4 programming manual (PM0214)** available from our website [www.st.com](http://www.st.com).



## 2 Description

The STM32F358xC family is based on the high-performance ARM® Cortex®-M4 32-bit RISC core with FPU operating at a frequency of up to 72 MHz, and embedding a floating point unit (FPU), a memory protection unit (MPU) and an embedded trace macrocell (ETM). The family incorporates high-speed embedded memories (up to 256 Kbytes of Flash memory, up to 48 Kbytes of SRAM) and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

The devices offer up to four fast 12-bit ADCs (5 Msps), up to seven comparators, up to four operational amplifiers, up to two DAC channels, a low-power RTC, up to five general-purpose 16-bit timers, one general-purpose 32-bit timer, and two timers dedicated to motor control. They also feature standard and advanced communication interfaces: up to two I<sup>2</sup>Cs, up to three SPIs (two SPIs are with multiplexed full-duplex I2Ss on STM32F358xC devices), three USARTs, up to two UARTs, and CAN. To achieve audio class accuracy, the I2S peripherals can be clocked via an external PLL.

The STM32F358xC family operates in the -40 to +85 °C and -40 to +105 °C temperature ranges. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F358xC family offers devices in three packages ranging from 48 pins to 100 pins.

The set of included peripherals changes with the device chosen.

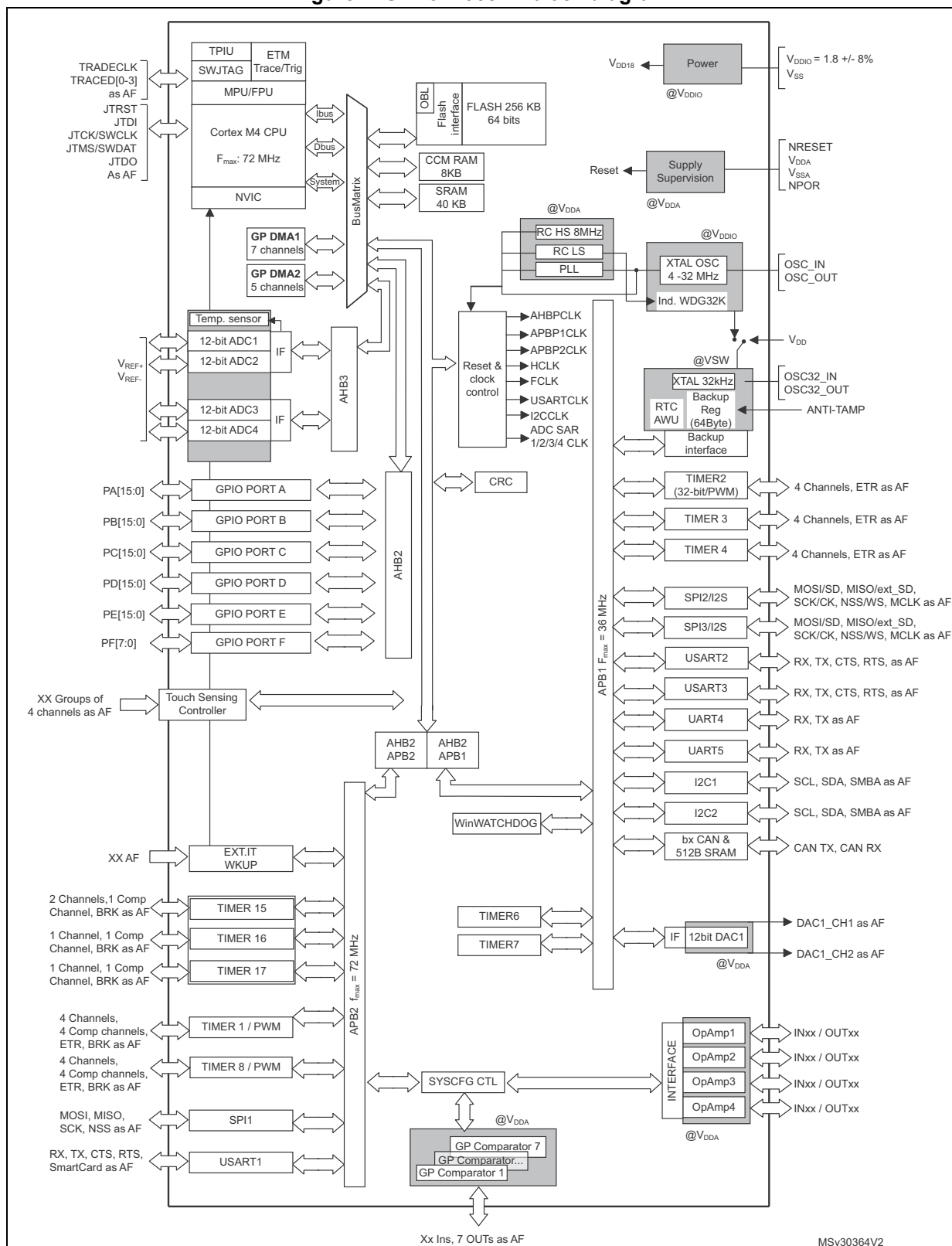
Table 2. STM32F358xC family device features and peripheral counts

| Peripheral                             |                                 | STM32F358Cx                                                                                              | STM32F358Rx | STM32F358Vx |
|----------------------------------------|---------------------------------|----------------------------------------------------------------------------------------------------------|-------------|-------------|
| Flash (Kbytes)                         |                                 | 256                                                                                                      | 256         | 256         |
| SRAM (Kbytes) on data bus              |                                 | 40                                                                                                       | 40          | 40          |
| CCM (Core Coupled Memory) RAM (Kbytes) |                                 | 8                                                                                                        |             |             |
| Timers                                 | Advanced control                | 2 (16-bit)                                                                                               |             |             |
|                                        | General purpose                 | 5 (16-bit)<br>1 (32-bit)                                                                                 |             |             |
|                                        | Basic                           | 2 (16-bit)                                                                                               |             |             |
| PWM channels (all) <sup>(1)</sup>      |                                 | 31                                                                                                       | 33          |             |
| PWM channels (except complementary)    |                                 | 22                                                                                                       | 24          |             |
| Comm. interfaces                       | SPI(I2S) <sup>(2)</sup>         | 3(2)                                                                                                     |             |             |
|                                        | I <sup>2</sup> C                | 2                                                                                                        |             |             |
|                                        | USART                           | 3                                                                                                        |             |             |
|                                        | UART                            | 2                                                                                                        |             |             |
|                                        | CAN                             | 1                                                                                                        |             |             |
| GPIOs                                  | Normal I/Os (TC, TTa)           | 19                                                                                                       | 26          | 44          |
|                                        | 5 volts Tolerant I/Os (FT, FTf) | 17                                                                                                       | 25          | 42          |
| DMA channels                           |                                 | 12                                                                                                       |             |             |
| 12-bit ADCs                            |                                 | 4                                                                                                        |             |             |
| Number of channels                     |                                 | 14                                                                                                       | 21          | 38          |
| 12-bit DAC channels                    |                                 | 2                                                                                                        |             |             |
| Analog comparator                      |                                 | 7                                                                                                        |             |             |
| Operational amplifiers                 |                                 | 4                                                                                                        |             |             |
| CPU frequency                          |                                 | 72 MHz                                                                                                   |             |             |
| Operating voltage                      |                                 | V <sub>DD</sub> = 1.8 V +/- 8%, V <sub>DDA</sub> = 1.65 V to 3.6 V                                       |             |             |
| Operating temperature                  |                                 | Ambient operating temperature: - 40 to 85 °C /<br>- 40 to 105 °C<br>Junction temperature: - 40 to 125 °C |             |             |
| Packages                               |                                 | LQFP48                                                                                                   | LQFP64      | LQFP100     |

1. This total number considers also the PWMs generated on the complementary output channels.

2. The SPI interfaces can work in an exclusive way in either the SPI mode or the I<sup>2</sup>S audio mode.

Figure 1. STM32F358xC block diagram



1. AF: alternate function on I/O pins.

## 3 Functional overview

### 3.1 ARM<sup>®</sup> Cortex<sup>®</sup>-M4 core with FPU with embedded Flash and SRAM

The ARM<sup>®</sup> Cortex<sup>®</sup>-M4 processor with FPU is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM<sup>®</sup> Cortex<sup>®</sup>-M4 32-bit RISC processor with FPU features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded ARM core, the STM32F358xC family is compatible with all ARM tools and software.

*Figure 1* shows the general block diagram of the STM32F358xC family devices.

### 3.2 Memory protection unit (MPU)

The memory protection unit (MPU) is used to separate the processing of tasks from the data protection. The MPU can manage up to 8 protection areas that can all be further divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The memory protection unit is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

### 3.3 Embedded Flash memory

All STM32F358xC devices feature up to 256 Kbytes of embedded Flash memory available for storing programs and data. The Flash memory access time is adjusted to the CPU clock frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).

### 3.4 Embedded SRAM

STM32F358xC devices feature up to 48 Kbytes of embedded SRAM with hardware parity

check. The memory can be accessed in read/write at CPU clock speed with 0 wait states, allowing the CPU to achieve 90 Dhrystone Mips at 72 MHz (when running code from the CCM (Core Coupled Memory) RAM).

- 8 Kbytes of CCM RAM on STM32F303xx devices mapped on both instruction and data bus, used to execute critical routines or to access data (parity check on all of CCM RAM).
- 40 Kbytes of SRAM mapped on the data bus (parity check on first 16 Kbytes of SRAM).

### 3.5 Boot modes

At startup, Boot0 pin and Boot1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10) or USART2 (PD5/PD6) or I2C1 (PB6/PB7).

### 3.6 Cyclic redundancy check (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

## 3.7 Power management

### 3.7.1 Power supply schemes

- $V_{SS}$ ,  $V_{DD} = 1.8 \text{ V} \pm 8\%$ : external power supply for I/Os and core. It is provided externally through  $V_{DD}$  pins.
- $V_{SSA}$ ,  $V_{DDA} = 1.65 \text{ to } 3.6 \text{ V}$ : external analog power supply for ADC, DACs, comparators, operational amplifiers, reset blocks, RCs and PLL. The minimum voltage to be applied to  $V_{DDA}$  differs from one analog peripheral to another. [Table 3](#) provides the summary of the  $V_{DDA}$  ranges for analog peripherals. The  $V_{DDA}$  voltage level must be always greater or equal to the  $V_{DD}$  voltage level and must be provided first.
- $V_{BAT} = 1.65 \text{ to } 3.6 \text{ V}$ : power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch which is guaranteed in the full range of  $V_{DD}$ ) when  $V_{DD}$  is not present.

**Table 3. External analog supply values for analog peripherals**

| Analog peripheral | Minimum $V_{DDA}$ supply | Maximum $V_{DDA}$ supply |
|-------------------|--------------------------|--------------------------|
| ADC               | 1.8 V                    | 3.6 V                    |
| COMP              | 1.65 V                   | 3.6 V                    |
| DAC / OPAMP       | 2.4 V                    | 3.6V                     |

### 3.7.2 Power supply supervision

The device power on reset is controlled through the external NPOR pin. The device remains in reset state when NPOR pin is held low.

To guarantee a proper power-on reset, the NPOR pin must be held low when  $V_{DDA}$  is applied. Then, when  $V_{DD}$  is stable, the reset state can be exited by:

- either putting the NPOR pin in high impedance. NPOR pin has an internal pull up.
- or forcing the pin to high level by connecting it to  $V_{DDA}$ .

### 3.7.3 Low-power modes

The STM32F358xC devices support two low-power modes to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- Sleep mode  
In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- Stop mode  
Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled.  
The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the RTC alarm, COMPx, I2Cx or U(S)ARTx.

*Note: The RTC, the IWDG and the corresponding clock sources are not stopped by entering Stop mode.*

### 3.8 Interconnect matrix

Several peripherals have direct connections between them. This allows autonomous communication between peripherals, saving CPU resources thus power supply consumption. In addition, these hardware connections allow fast and predictable latency.

**Table 4. STM32F358xC peripheral interconnect matrix**

| Interconnect source                                         | Interconnect destination     | Interconnect action                                            |
|-------------------------------------------------------------|------------------------------|----------------------------------------------------------------|
| TIMx                                                        | TIMx                         | Timers synchronization or chaining                             |
|                                                             | ADCx<br>DAC1                 | Conversion triggers                                            |
|                                                             | DMA                          | Memory to memory transfer trigger                              |
|                                                             | Comp <sub>x</sub>            | Comparator output blanking                                     |
| COMP <sub>x</sub>                                           | TIMx                         | Timer input: OCREF_CLR input, input capture                    |
| ADC <sub>x</sub>                                            | TIMx                         | Timer triggered by analog watchdog                             |
| GPIO<br>RTCCLK<br>HSE/32<br>MC0                             | TIM16                        | Clock source used as input channel for HSI and LSI calibration |
| CSS<br>CPU (hard fault)<br>COMP <sub>x</sub><br>PVD<br>GPIO | TIM1, TIM8,<br>TIM15, 16, 17 | Timer break                                                    |
| GPIO                                                        | TIMx                         | External trigger, timer break                                  |
|                                                             | ADC <sub>x</sub><br>DAC1     | Conversion external trigger                                    |
| DAC1                                                        | COMP <sub>x</sub>            | Comparator inverting input                                     |

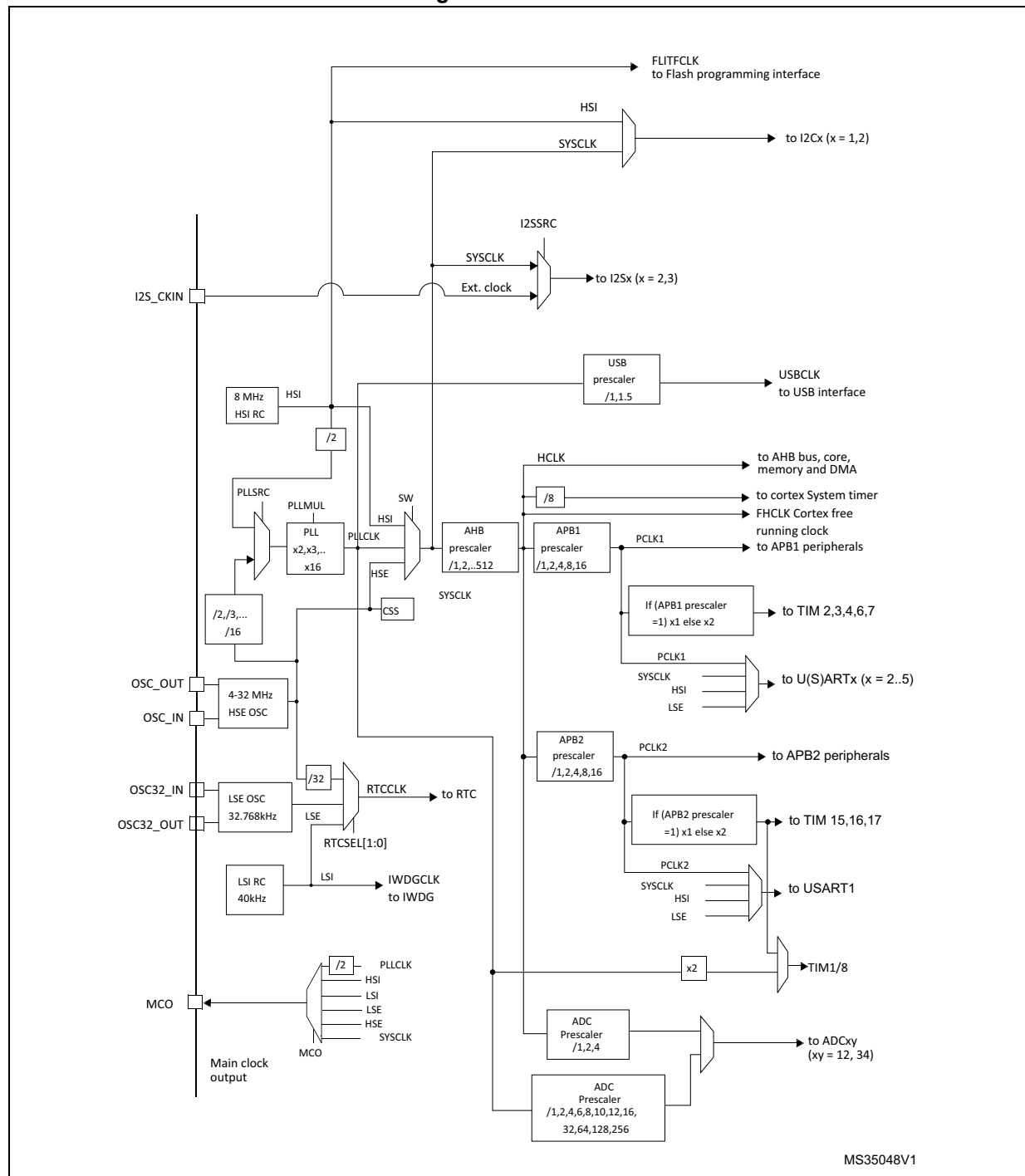
**Note:** For more details about the interconnect actions, please refer to the corresponding sections in the reference manual RM0316.

### 3.9 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz, while the maximum allowed frequency of the low speed APB domain is 36 MHz.

Figure 2. Clock tree



### 3.10 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allows I/O toggling up to 36 MHz.

### 3.11 Direct memory access (DMA)

The flexible general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each of the 12 DMA channels is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I<sup>2</sup>C, USART, general-purpose timers, DAC and ADC.

### 3.12 Interrupts and events

#### 3.12.1 Nested vectored interrupt controller (NVIC)

The STM32F358xC devices embed a nested vectored interrupt controller (NVIC) able to handle up to 66 maskable interrupt channels and 16 priority levels.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

### 3.13 Fast analog-to-digital converter (ADC)

Up to four fast analog-to-digital converters 5 MSPS, with selectable resolution between 12 and 6 bit, are embedded in the STM32F358xC family devices. The ADCs have up to 38 external channels. Some of the external channels are shared between ADC1&2 and between ADC3&4, performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADCs have also internal channels: Temperature sensor connected to ADC1 channel 16, VBAT/2 connected to ADC1 channel 17, Voltage reference  $V_{REFINT}$  connected to the 4 ADCs channel 18, VOPAMP1 connected to ADC1 channel 15, VOPAMP2 connected to ADC2 channel 17, VOPAMP3 connected to ADC3 channel 17, VOPAMP4 connected to ADC4 channel 17.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold
- Single-shunt phase current reading techniques.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers and the advanced-control timers can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

#### 3.13.1 Temperature sensor

The temperature sensor (TS) generates a voltage  $V_{SENSE}$  that varies linearly with temperature.

The temperature sensor is internally connected to the ADC\_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

#### 3.13.2 Internal voltage reference ( $V_{REFINT}$ )

The internal voltage reference ( $V_{REFINT}$ ) provides a stable (bandgap) voltage output for the ADC and Comparators.  $V_{REFINT}$  is internally connected to the ADC\_IN18 input channel. The precise voltage of  $V_{REFINT}$  is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

### 3.13.3 VBAT battery voltage monitoring

This embedded hardware feature allows the application to measure the VBAT battery voltage using the internal ADC channel ADC\_IN17. As the VBAT voltage may be higher than VDDA, and thus outside the ADC input range, the VBAT pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half the VBAT voltage.

### 3.13.4 OPAMP reference voltage (VOPAMP)

Every OPAMP reference voltage can be measured using a corresponding ADC internal channel: VOPAMP1 connected to ADC1 channel 15, VOPAMP2 connected to ADC2 channel 17, VOPAMP3 connected to ADC3 channel 17, VOPAMP4 connected to ADC4 channel 17.

## 3.14 Digital-to-analog converter (DAC)

Up to two 12-bit buffered DAC channels can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital interface supports the following features:

- Up to two DAC output channels on STM32F358xC devices
- 8-bit or 10-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability on STM32F358xC devices
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions on STM32F358xC devices
- DMA capability (for each channel on STM32F358xC devices)
- External triggers for conversion

## 3.15 Operational amplifier (OPAMP)

The STM32F358xC devices embed up to four operational amplifiers with external or internal follower routing and PGA capability (or even amplifier and filter capability with external components). When an operational amplifier is selected, an external ADC channel is used to enable output measurement.

The operational amplifier features:

- 8.2 MHz bandwidth
- 0.5 mA output capability
- Rail-to-rail input/output
- In PGA mode, the gain can be programmed to be 2, 4, 8 or 16.

### 3.16 Fast comparators (COMP)

The STM32F358xC devices embed seven fast rail-to-rail comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low-power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output pin
- Internal reference voltage or submultiple (1/4, 1/2, 3/4). Refer to [Table 26: Embedded internal reference voltage on page 57](#) for the value and precision of the internal reference voltage.

All comparators can wake up from STOP mode, generate interrupts and breaks for the timers and can be also combined per pair into a window comparator

### 3.17 Timers and watchdogs

The STM32F358xC devices include up to two advanced control timers, up to 6 general-purpose timers, two basic timers, two watchdog timers and a SysTick timer. The table below compares the features of the advanced control, general purpose and basic timers.

**Table 5. Timer feature comparison**

| Timer type      | Timer        | Counter resolution | Counter type      | Prescaler factor                | DMA request generation | Capture/compare Channels | Complementary outputs |
|-----------------|--------------|--------------------|-------------------|---------------------------------|------------------------|--------------------------|-----------------------|
| Advanced        | TIM1, TIM8   | 16-bit             | Up, Down, Up/Down | Any integer between 1 and 65536 | Yes                    | 4                        | Yes                   |
| General-purpose | TIM2         | 32-bit             | Up, Down, Up/Down | Any integer between 1 and 65536 | Yes                    | 4                        | No                    |
| General-purpose | TIM3, TIM4   | 16-bit             | Up, Down, Up/Down | Any integer between 1 and 65536 | Yes                    | 4                        | No                    |
| General-purpose | TIM15        | 16-bit             | Up                | Any integer between 1 and 65536 | Yes                    | 2                        | 1                     |
| General-purpose | TIM16, TIM17 | 16-bit             | Up                | Any integer between 1 and 65536 | Yes                    | 1                        | 1                     |
| Basic           | TIM6, TIM7   | 16-bit             | Up                | Any integer between 1 and 65536 | Yes                    | 0                        | No                    |

*Note:* TIM1/8 can have PLL as clock source, and therefore can be clocked at 144 MHz.

### 3.17.1 Advanced timers (TIM1, TIM8)

The advanced-control timers (TIM1 on all devices and TIM8 on STM32F358xC devices) can each be seen as a three-phase PWM multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIM timers (described in [Section 3.17.2](#) using the same architecture, so the advanced-control timers can work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

### 3.17.2 General-purpose timers (TIM2, TIM3, TIM4, TIM15, TIM16, TIM17)

There are up to six synchronizable general-purpose timers embedded in the STM32F358xC devices (see [Table 5](#) for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2, 3, and TIM4

These are full-featured general-purpose timers:

- TIM2 has a 32-bit auto-reload up/downcounter and 32-bit prescaler
- TIM3 and 4 have 16-bit auto-reload up/downcounters and 16-bit prescalers.

These timers all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.

The counters can be frozen in debug mode.

All have independent DMA request generation and support quadrature encoders.

- TIM15, 16 and 17

These three timers general-purpose timers with mid-range features:

They have 16-bit auto-reload upcounters and 16-bit prescalers.

- TIM15 has 2 channels and 1 complementary channel
- TIM16 and TIM17 have 1 channel and 1 complementary channel

All channels can be used for input capture/output compare, PWM or one-pulse mode output.

The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.

The counters can be frozen in debug mode.

### 3.17.3 Basic timers (TIM6, TIM7)

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

### 3.17.4 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop mode. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

### 3.17.5 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

### 3.17.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

## 3.18 Real-time clock (RTC) and backup registers

The RTC and the 16 backup registers are supplied through  $V_{DD}$  a switch that takes power from either the VDD supply when present or the VBAT pin. The backup registers are sixteen 32-bit registers used to store 64 bytes of user application data when  $V_{DD}$  power is not present.

They are not reset by a system or power reset.

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Automatic correction for 28, 29 (leap year), 30 and 31 days of the month.
- Two programmable alarms with wake up from Stop mode capability.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop mode on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop mode on timestamp event detection.

- 17-bit Auto-reload counter for periodic interrupt with wakeup from STOP capability.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32.

### 3.19 Inter-integrated circuit interface (I<sup>2</sup>C)

Up to two I<sup>2</sup>C bus interfaces can operate in multimaster and slave modes. They can support standard (up to 100 KHz), fast (up to 400 KHz) and fast mode + (up to 1 MHz) modes. Both support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). They also include programmable analog and digital noise filters.

**Table 6. Comparison of I2C analog and digital filters**

|                                  | Analog filter                                         | Digital filter                                                                     |
|----------------------------------|-------------------------------------------------------|------------------------------------------------------------------------------------|
| Pulse width of suppressed spikes | ≥ 50 ns                                               | Programmable length from 1 to 15 I2C peripheral clocks                             |
| Benefits                         | Available in Stop mode                                | 1. Extra filtering capability vs. standard requirements.<br>2. Stable length       |
| Drawbacks                        | Variations depending on temperature, voltage, process | Wakeup from Stop on address match is not available when digital filter is enabled. |

In addition, they provide hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. They also have a clock domain independent from the CPU clock, allowing the I2Cx (x=1,2) to wake up the MCU from Stop mode on address match. The I2C interfaces can be served by the DMA controller. Refer to [Table 7](#) for the features available in I2C1 and I2C2.

**Table 7. STM32F358xC I<sup>2</sup>C implementation**

| I2C features <sup>(1)</sup>                                 | I2C1 | I2C2 |
|-------------------------------------------------------------|------|------|
| 7-bit addressing mode                                       | X    | X    |
| 10-bit addressing mode                                      | X    | X    |
| Standard mode (up to 100 kbit/s)                            | X    | X    |
| Fast mode (up to 400 kbit/s)                                | X    | X    |
| Fast Mode Plus with 20mA output drive I/Os (up to 1 Mbit/s) | X    | X    |
| Independent clock                                           | X    | X    |
| SMBus                                                       | X    | X    |
| Wakeup from STOP                                            | X    | X    |

1. X = supported.

### 3.20 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32F358xC devices have three embedded universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3).

The USART interfaces are able to communicate at speeds of up to 9 Mbits/s.

They provide hardware management of the CTS and RTS signals, they support IrDA SIR ENDEC, the multiprocessor communication mode, the single-wire half-duplex communication mode and have LIN Master/Slave capability. The USART interfaces can be served by the DMA controller.

### 3.21 Universal asynchronous receiver transmitter (UART)

The STM32F358xC devices have 2 embedded universal asynchronous receiver transmitters (UART4, and UART5). The UART interfaces support IrDA SIR ENDEC, multiprocessor communication mode and single-wire half-duplex communication mode. The UART4 interface can be served by the DMA controller.

Refer to [Table 8](#) for the features available in all U(S)ARTs interfaces.

**Table 8. USART features**

| USART modes/features <sup>(1)</sup>         | USART1 | USART2 | USART3 | UART4 | UART5 |
|---------------------------------------------|--------|--------|--------|-------|-------|
| Hardware flow control for modem             | X      | X      | X      | -     | -     |
| Continuous communication using DMA          | X      | X      | X      | X     | -     |
| Multiprocessor communication                | X      | X      | X      | X     | X     |
| Synchronous mode                            | X      | X      | X      | -     | -     |
| Smartcard mode                              | X      | X      | X      | -     | -     |
| Single-wire half-duplex communication       | X      | X      | X      | X     | X     |
| IrDA SIR ENDEC block                        | X      | X      | X      | X     | X     |
| LIN mode                                    | X      | X      | X      | X     | X     |
| Dual clock domain and wakeup from Stop mode | X      | X      | X      | X     | X     |
| Receiver timeout interrupt                  | X      | X      | X      | X     | X     |
| Modbus communication                        | X      | X      | X      | X     | X     |
| Auto baud rate detection                    | X      | X      | X      | -     | -     |
| Driver Enable                               | X      | X      | X      | -     | -     |

1. X = supported.

### 3.22 Serial peripheral interface (SPI)/Inter-integrated sound interfaces (I2S)

Up to three SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

Two standard I2S interfaces (multiplexed with SPI2 and SPI3) supporting four different audio standards can operate as master or slave at half-duplex and full duplex communication modes. They can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by 8-bit programmable linear prescaler. When operating in master mode it can output a clock for an external audio component at 256 times the sampling frequency.

Refer to [Table 9](#) for the features available in SPI1, SPI2 and SPI3.

**Table 9. STM32F358xC SPI/I2S implementation**

| SPI features <sup>(1)</sup> | SPI1 | SPI2 | SPI3 |
|-----------------------------|------|------|------|
| Hardware CRC calculation    | X    | X    | X    |
| Rx/Tx FIFO                  | X    | X    | X    |
| NSS pulse mode              | X    | X    | X    |
| I2S mode                    | -    | X    | X    |
| TI mode                     | X    | X    | X    |

1. X = supported.

### 3.23 Controller area network (CAN)

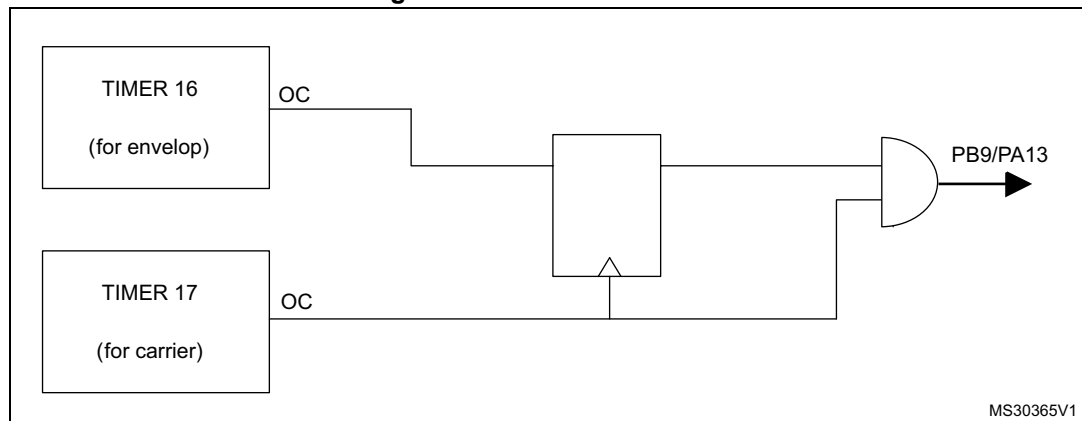
The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

### 3.24 Infrared Transmitter

The STM32F358xC devices provide an infrared transmitter solution. The solution is based on internal connections between TIM16 and TIM17 as shown in the figure below. TIM17 is used to provide the carrier frequency and TIM16 provides the main signal to be sent. The infrared output signal is available on PB9 or PA13.

To generate the infrared remote control signals, TIM16 channel 1 and TIM17 channel 1 must be properly configured to generate correct waveforms. All standard IR pulse modulation modes can be obtained by programming the two timers output compare channels.

Figure 3. Infrared transmitter



### 3.25 Touch sensing controller (TSC)

The STM32F358xC devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 24 capacitive sensing channels distributed over 8 analog I/O groups.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic, ...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

Table 10. Capacitive sensing GPIOs available on STM32F358xC devices

| Group | Capacitive sensing signal name | Pin name | Group | Capacitive sensing signal name | Pin name |
|-------|--------------------------------|----------|-------|--------------------------------|----------|
| 1     | TSC_G1_IO1                     | PA0      | 5     | TSC_G5_IO1                     | PB3      |
|       | TSC_G1_IO2                     | PA1      |       | TSC_G5_IO2                     | PB4      |
|       | TSC_G1_IO3                     | PA2      |       | TSC_G5_IO3                     | PB6      |
|       | TSC_G1_IO4                     | PA3      |       | TSC_G5_IO4                     | PB7      |
| 2     | TSC_G2_IO1                     | PA4      | 6     | TSC_G6_IO1                     | PB11     |
|       | TSC_G2_IO2                     | PA5      |       | TSC_G6_IO2                     | PB12     |
|       | TSC_G2_IO3                     | PA6      |       | TSC_G6_IO3                     | PB13     |
|       | TSC_G2_IO4                     | PA7      |       | TSC_G6_IO4                     | PB14     |
| 3     | TSC_G3_IO1                     | PC5      | 7     | TSC_G7_IO1                     | PE2      |
|       | TSC_G3_IO2                     | PB0      |       | TSC_G7_IO2                     | PE3      |
|       | TSC_G3_IO3                     | PB1      |       | TSC_G7_IO3                     | PE4      |
| 4     | TSC_G4_IO1                     | PA9      |       | TSC_G7_IO4                     | PE5      |
|       | TSC_G4_IO2                     | PA10     | 8     | TSC_G8_IO1                     | PD12     |
|       | TSC_G4_IO3                     | PA13     |       | TSC_G8_IO2                     | PD13     |
|       | TSC_G4_IO4                     | PA14     |       | TSC_G8_IO3                     | PD14     |
|       |                                |          |       | TSC_G8_IO4                     | PD15     |

Table 11. No. of capacitive sensing channels available on STM32F358xC devices

| Analog I/O group                      | Number of capacitive sensing channels |              |              |
|---------------------------------------|---------------------------------------|--------------|--------------|
|                                       | STM32F358xVx                          | STM32F358xRx | STM32F358xCx |
| G1                                    | 3                                     | 3            | 3            |
| G2                                    | 3                                     | 3            | 3            |
| G3                                    | 2                                     | 2            | 1            |
| G4                                    | 3                                     | 3            | 3            |
| G5                                    | 3                                     | 3            | 3            |
| G6                                    | 3                                     | 3            | 3            |
| G7                                    | 3                                     | 0            | 0            |
| G8                                    | 3                                     | 0            | 0            |
| Number of capacitive sensing channels | 23                                    | 17           | 16           |

## **3.26 Development support**

### **3.26.1 Serial wire JTAG debug port (SWJ-DP)**

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

### **3.26.2 Embedded trace macrocell™**

The ARM embedded trace macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F358xC through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using a high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

# 4 Pinouts and pin description

Figure 4. STM32F358xC LQFP48 pinout

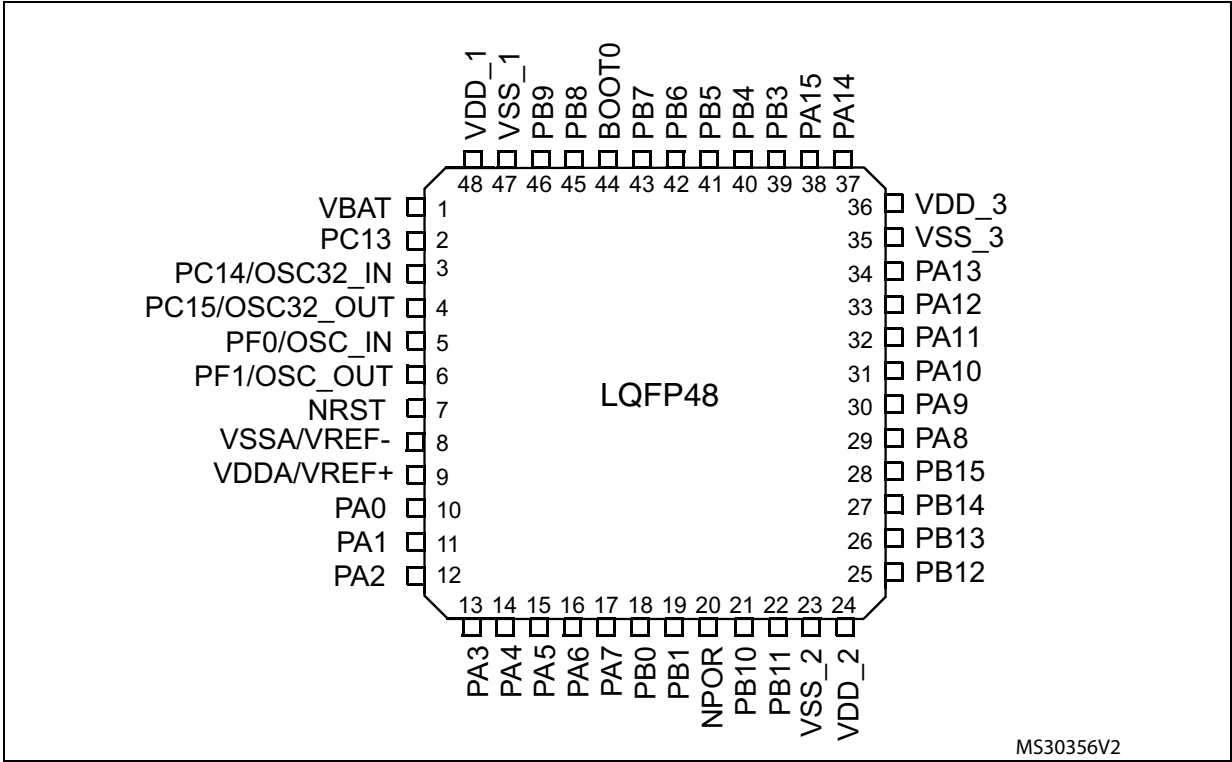
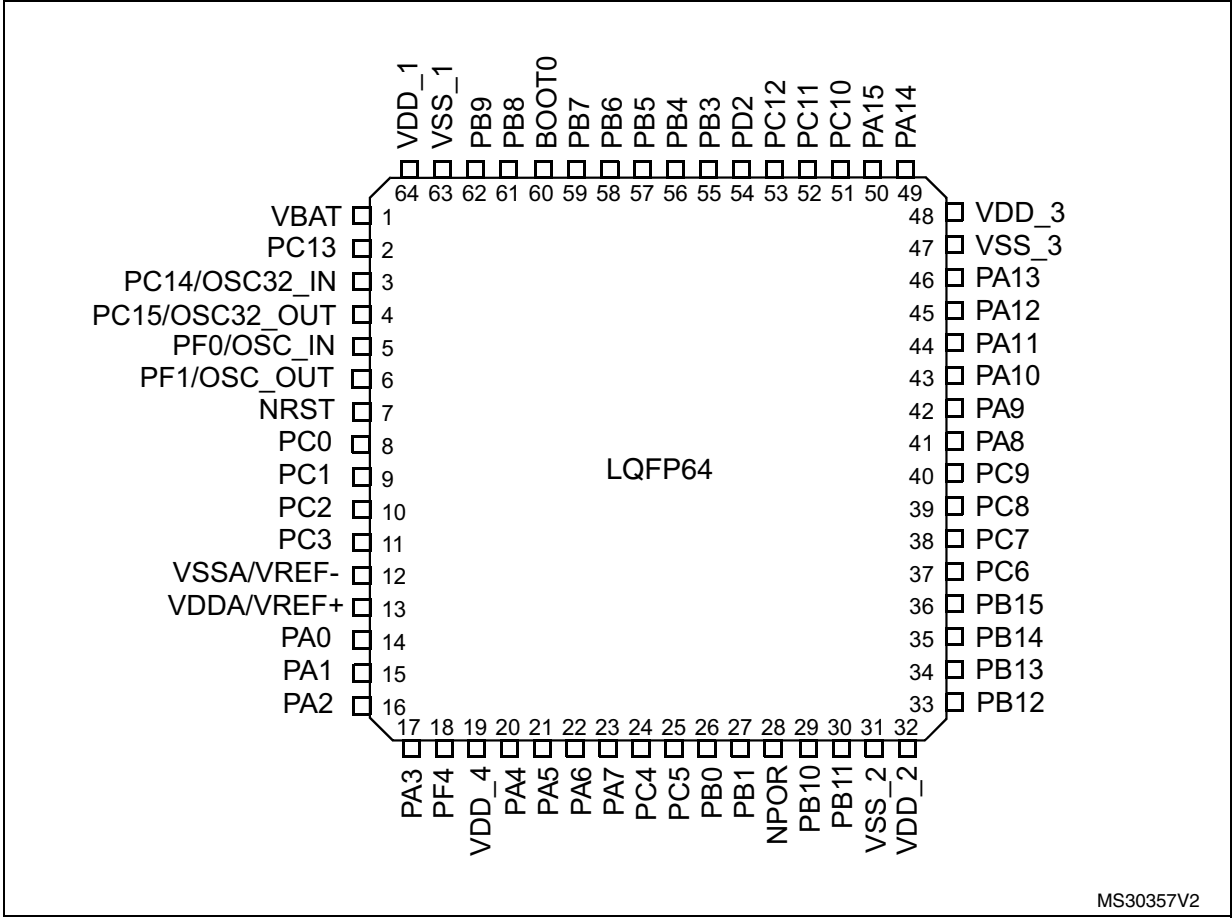
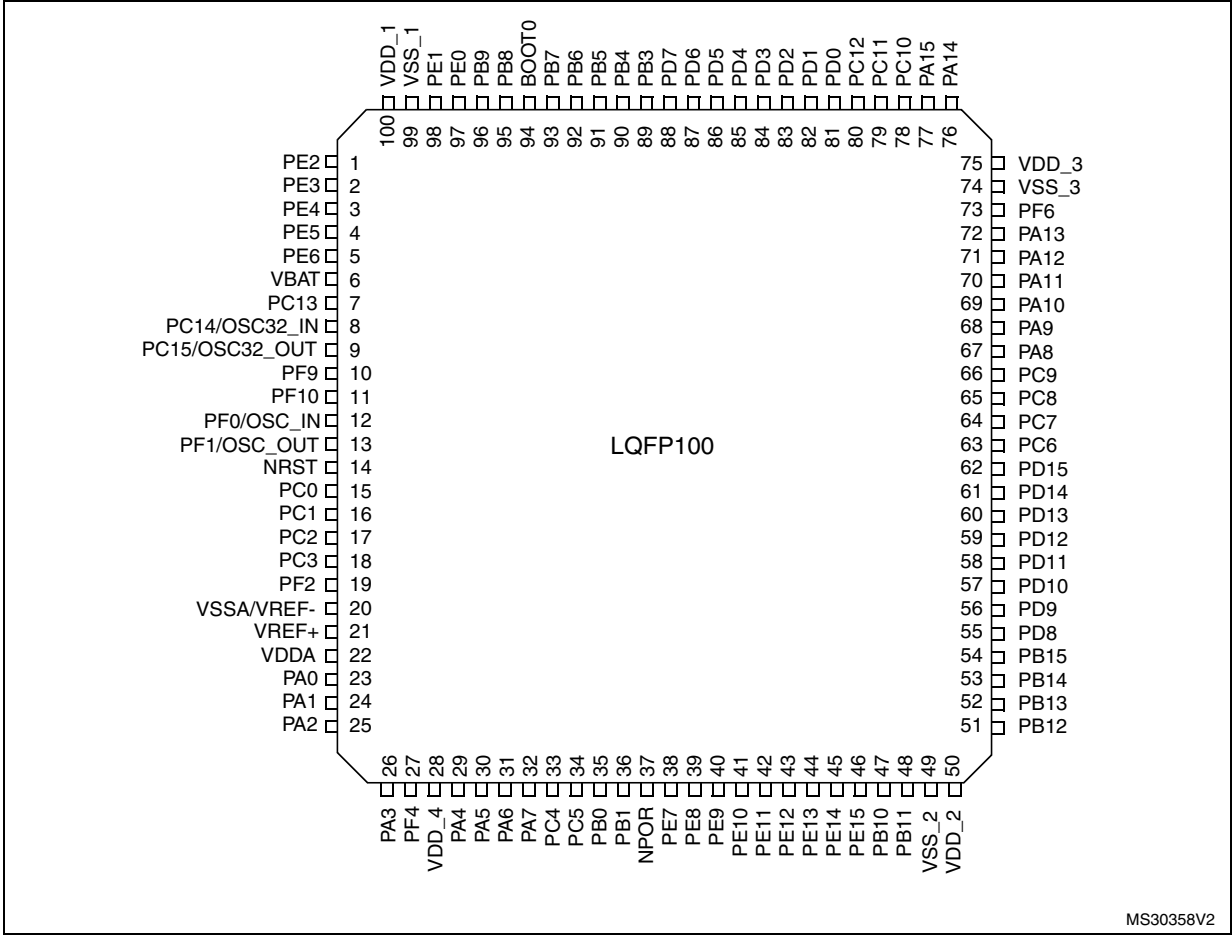


Figure 5. STM32F358xC LQFP64 pinout



MS30357V2

Figure 6. STM32F358xC LQFP100 pinout



MS30358V2

Table 12. Legend/abbreviations used in the pinout table

| Name          |                      | Abbreviation                                                                                                                          | Definition                                                                         |
|---------------|----------------------|---------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------|
| Pin name      |                      | Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name |                                                                                    |
| Pin type      |                      | S                                                                                                                                     | Supply pin                                                                         |
|               |                      | I                                                                                                                                     | Input only pin                                                                     |
|               |                      | I/O                                                                                                                                   | Input / output pin                                                                 |
| I/O structure |                      | FT                                                                                                                                    | 5 V tolerant I/O                                                                   |
|               |                      | FTf                                                                                                                                   | 5 V tolerant I/O, FM+ capable                                                      |
|               |                      | TTa                                                                                                                                   | 3.3 V tolerant I/O directly connected to ADC                                       |
|               |                      | TC                                                                                                                                    | Standard 3.3V I/O                                                                  |
|               |                      | B                                                                                                                                     | Dedicated BOOT0 pin                                                                |
|               |                      | RST                                                                                                                                   | Bidirectional reset pin with embedded weak pull-up resistor                        |
|               |                      | POR                                                                                                                                   | External power on reset pin with embedded weak pull-up resistor, powered from VDDA |
| Notes         |                      | Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset                                      |                                                                                    |
| Pin functions | Alternate functions  | Functions selected through GPIOx_AFR registers                                                                                        |                                                                                    |
|               | Additional functions | Functions directly selected/enabled through peripheral registers                                                                      |                                                                                    |

Table 13. STM32F358xC pin definitions

| Pin number |        |        | Pin name<br>(function<br>after<br>reset)       | Pin type | I/O structure | Notes | Pin functions                                           |                                      |
|------------|--------|--------|------------------------------------------------|----------|---------------|-------|---------------------------------------------------------|--------------------------------------|
| LQFP100    | LQFP64 | LQFP48 |                                                |          |               |       | Alternate functions                                     | Additional functions                 |
| 1          | -      | -      | PE2                                            | I/O      | FT            | (1)   | TRACECK, TIM3_CH1,<br>TSC_G7_IO1, EVENTOUT              | -                                    |
| 2          | -      | -      | PE3                                            | I/O      | FT            | (1)   | TRACED0, TIM3_CH2,<br>TSC_G7_IO2, EVENTOUT              | -                                    |
| 3          | -      | -      | PE4                                            | I/O      | FT            | (1)   | TRACED1, TIM3_CH3,<br>TSC_G7_IO3, EVENTOUT              | -                                    |
| 4          | -      | -      | PE5                                            | I/O      | FT            | (1)   | TRACED2, TIM3_CH4,<br>TSC_G7_IO4, EVENTOUT              | -                                    |
| 5          | -      | -      | PE6                                            | I/O      | FT            | (1)   | TRACED3, EVENTOUT                                       | WKUP3, RTC_TAMP3                     |
| 6          | 1      | 1      | V <sub>BAT</sub>                               | S        | -             | -     | Backup power supply                                     |                                      |
| 7          | 2      | 2      | PC13 <sup>(2)</sup>                            | I/O      | TC            | -     | TIM1_CH1N                                               | WKUP2, RTC_TAMP1,<br>RTC_TS, RTC_OUT |
| 8          | 3      | 3      | PC14 <sup>(2)</sup><br>OSC32_IN<br>(PC14)      | I/O      | TC            | -     | -                                                       | OSC32_IN                             |
| 9          | 4      | 4      | PC15 <sup>(2)</sup><br>OSC32_<br>OUT<br>(PC15) | I/O      | TC            | -     | -                                                       | OSC32_OUT                            |
| 10         | -      | -      | PF9                                            | I/O      | FT            | (1)   | TIM15_CH1, SPI2_SCK,<br>EVENTOUT                        | -                                    |
| 11         | -      | -      | PF10                                           | I/O      | FT            | (1)   | TIM15_CH2, SPI2_SCK,<br>EVENTOUT                        | -                                    |
| 12         | 5      | 5      | PF0-<br>OSC_IN<br>(PF0)                        | I/O      | FTf           | -     | TIM1_CH3N, I2C2_SDA,                                    | OSC_IN                               |
| 13         | 6      | 6      | PF1-<br>OSC_OUT<br>(PF1)                       | I/O      | FTf           | -     | I2C2_SCL                                                | OSC_OUT                              |
| 14         | 7      | 7      | NRST                                           | I/O      | RST           | -     | Device reset input / internal reset output (active low) |                                      |
| 15         | 8      | -      | PC0                                            | I/O      | TTa           | (1)   | EVENTOUT                                                | ADC12_IN6, COMP7_INM                 |
| 16         | 9      | -      | PC1                                            | I/O      | TTa           | (1)   | EVENTOUT                                                | ADC12_IN7, COMP7_INP                 |
| 17         | 10     | -      | PC2                                            | I/O      | TTa           | (1)   | COMP7_OUT, EVENTOUT                                     | ADC12_IN8                            |
| 18         | 11     | -      | PC3                                            | I/O      | TTa           | (1)   | TIM1_BKIN2, EVENTOUT                                    | ADC12_IN9                            |
| 19         | -      | -      | PF2                                            | I/O      | TTa           | (1)   | EVENTOUT                                                | ADC12_IN10                           |
| 20         | 12     | 8      | VSSA/<br>VREF-                                 | S        | -             | -     | Analog ground/Negative reference voltage                |                                      |

Table 13. STM32F358xC pin definitions (continued)

| Pin number |        |        | Pin name<br>(function<br>after<br>reset) | Pin type | I/O structure | Notes | Pin functions                                                                                  |                                                                                                                                                             |
|------------|--------|--------|------------------------------------------|----------|---------------|-------|------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LQFP100    | LQFP64 | LQFP48 |                                          |          |               |       | Alternate functions                                                                            | Additional functions                                                                                                                                        |
| 21         | -      | -      | VREF+                                    | S        | -             | -     | Positive reference voltage                                                                     |                                                                                                                                                             |
| 22         | -      | -      | VDDA                                     | S        | -             | -     | Analog power supply                                                                            |                                                                                                                                                             |
| -          | 13     | 9      | VDDA/<br>VREF+                           | S        | -             | -     | Analog power supply/Positive reference voltage                                                 |                                                                                                                                                             |
| 23         | 14     | 10     | PA0                                      | I/O      | TTa           | -     | USART2_CTS,<br>TIM2_CH1_ETR, TIM8_BKIN,<br>TIM8_ETR, TSC_G1_IO1,<br>COMP1_OUT, EVENTOUT        | ADC1_IN1, COMP1_INM,<br>RTC_TAMP2, WKUP1,<br>COMP7_INP                                                                                                      |
| 24         | 15     | 11     | PA1                                      | I/O      | TTa           | -     | USART2_RTS_DE,<br>TIM2_CH2, TSC_G1_IO2,<br>TIM15_CH1N, RTC_REFIN,<br>EVENTOUT                  | ADC1_IN2, COMP1_INP,<br>OPAMP1_VINP,<br>OPAMP3_VINP                                                                                                         |
| 25         | 16     | 12     | PA2                                      | I/O      | TTa           | (3)   | USART2_TX, TIM2_CH3,<br>TIM15_CH1, TSC_G1_IO3,<br>COMP2_OUT, EVENTOUT                          | ADC1_IN3, COMP2_INM,<br>OPAMP1_VOUT                                                                                                                         |
| 26         | 17     | 13     | PA3                                      | I/O      | TTa           | -     | USART2_RX, TIM2_CH4,<br>TIM15_CH2, TSC_G1_IO4,<br>EVENTOUT                                     | ADC1_IN4, OPAMP1_VINP,<br>COMP2_INP,<br>OPAMP1_VINM                                                                                                         |
| 27         | 18     | -      | PF4                                      | I/O      | TTa           | (1)   | COMP1_OUT, EVENTOUT                                                                            | ADC1_IN5                                                                                                                                                    |
| 28         | 19     | -      | VDD_4                                    | S        | -             | -     | -                                                                                              | -                                                                                                                                                           |
| 29         | 20     | 14     | PA4                                      | I/O      | TTa           | (3)   | SPI1_NSS, SPI3_NSS,<br>I2S3_WS, USART2_CK,<br>TSC_G2_IO1, TIM3_CH2,<br>EVENTOUT                | ADC2_IN1, DAC1_OUT1,<br>OPAMP4_VINP,<br>COMP1_INM, COMP2_INM,<br>COMP3_INM, COMP4_INM,<br>COMP5_INM,<br>COMP6_INM, COMP7_INM                                |
| 30         | 21     | 15     | PA5                                      | I/O      | TTa           | (3)   | SPI1_SCK, TIM2_CH1_ETR,<br>TSC_G2_IO2, EVENTOUT                                                | ADC2_IN2, DAC1_OUT2<br>OPAMP1_VINP,<br>OPAMP2_VINM,<br>OPAMP3_VINP,<br>COMP1_INM, COMP2_INM,<br>COMP3_INM,<br>COMP4_INM, COMP5_INM,<br>COMP6_INM, COMP7_INM |
| 31         | 22     | 16     | PA6                                      | I/O      | TTa           | (3)   | SPI1_MISO, TIM3_CH1,<br>TIM8_BKIN, TIM1_BKIN,<br>TIM16_CH1, COMP1_OUT,<br>TSC_G2_IO3, EVENTOUT | ADC2_IN3, OPAMP2_VOUT                                                                                                                                       |

Table 13. STM32F358xC pin definitions (continued)

| Pin number |        |        | Pin name<br>(function<br>after<br>reset) | Pin type | I/O structure | Notes | Pin functions                                                                                  |                                                      |
|------------|--------|--------|------------------------------------------|----------|---------------|-------|------------------------------------------------------------------------------------------------|------------------------------------------------------|
| LQFP100    | LQFP64 | LQFP48 |                                          |          |               |       | Alternate functions                                                                            | Additional functions                                 |
| 32         | 23     | 17     | PA7                                      | I/O      | TTa           | -     | SPI1_MOSI, TIM3_CH2,<br>TIM17_CH1, TIM1_CH1N,<br>TIM8_CH1N, TSC_G2_IO4,<br>COMP2_OUT, EVENTOUT | ADC2_IN4, COMP2_INP,<br>OPAMP2_VINP,<br>OPAMP1_VINP  |
| 33         | 24     | -      | PC4                                      | I/O      | TTa           | (1)   | USART1_TX, EVENTOUT                                                                            | ADC2_IN5                                             |
| 34         | 25     | -      | PC5                                      | I/O      | TTa           | (1)   | USART1_RX, TSC_G3_IO1,<br>EVENTOUT                                                             | ADC2_IN11, OPAMP2_VINM,<br>OPAMP1_VINM               |
| 35         | 26     | 18     | PB0                                      | I/O      | TTa           | -     | TIM3_CH3, TIM1_CH2N,<br>TIM8_CH2N, TSC_G3_IO2,<br>EVENTOUT                                     | ADC3_IN12, COMP4_INP,<br>OPAMP3_VINP,<br>OPAMP2_VINP |
| 36         | 27     | 19     | PB1                                      | I/O      | TTa           | (3)   | TIM3_CH4, TIM1_CH3N,<br>TIM8_CH3N, COMP4_OUT,<br>TSC_G3_IO3, EVENTOUT                          | ADC3_IN1, OPAMP3_VOUT                                |
| 37         | 28     | 20     | NPOR                                     | I        | POR           | (4)   | Device power-on reset input                                                                    |                                                      |
| 38         | -      | -      | PE7                                      | I/O      | TTa           | (1)   | TIM1_ETR, EVENTOUT                                                                             | ADC3_IN13, COMP4_INP                                 |
| 39         | -      | -      | PE8                                      | I/O      | TTa           | (1)   | TIM1_CH1N, EVENTOUT                                                                            | COMP4_INM, ADC34_IN6                                 |
| 40         | -      | -      | PE9                                      | I/O      | TTa           | (1)   | TIM1_CH1, EVENTOUT                                                                             | ADC3_IN2                                             |
| 41         | -      | -      | PE10                                     | I/O      | TTa           | (1)   | TIM1_CH2N, EVENTOUT                                                                            | ADC3_IN14                                            |
| 42         | -      | -      | PE11                                     | I/O      | TTa           | (1)   | TIM1_CH2, EVENTOUT                                                                             | ADC3_IN15                                            |
| 43         | -      | -      | PE12                                     | I/O      | TTa           | (1)   | TIM1_CH3N, EVENTOUT                                                                            | ADC3_IN16                                            |
| 44         | -      | -      | PE13                                     | I/O      | TTa           | (1)   | TIM1_CH3, EVENTOUT                                                                             | ADC3_IN3                                             |
| 45         | -      | -      | PE14                                     | I/O      | TTa           | (1)   | TIM1_CH4, TIM1_BKIN2,<br>EVENTOUT                                                              | ADC4_IN1                                             |
| 46         | -      | -      | PE15                                     | I/O      | TTa           | (1)   | USART3_RX, TIM1_BKIN,<br>EVENTOUT                                                              | ADC4_IN2                                             |
| 47         | 29     | 21     | PB10                                     | I/O      | TTa           | -     | USART3_TX, TIM2_CH3,<br>TSC_SYNC, EVENTOUT                                                     | COMP5_INM,<br>OPAMP4_VINM,<br>OPAMP3_VINM            |
| 48         | 30     | 22     | PB11                                     | I/O      | TTa           | -     | USART3_RX, TIM2_CH4,<br>TSC_G6_IO1, EVENTOUT                                                   | COMP6_INP, OPAMP4_VINP                               |
| 49         | 31     | 23     | VSS_2                                    | S        | -             | -     | Digital ground                                                                                 |                                                      |
| 50         | 32     | 24     | VDD_2                                    | S        | -             | -     | Digital power supply                                                                           |                                                      |
| 51         | 33     | 25     | PB12                                     | I/O      | TTa           | (3)   | SPI2_NSS, I2S2_WS,<br>I2C2_SMBA, USART3_CK,<br>TIM1_BKIN, TSC_G6_IO2,<br>EVENTOUT              | ADC4_IN3, COMP3_INM,<br>OPAMP4_VOUT,                 |

Table 13. STM32F358xC pin definitions (continued)

| Pin number |        |        | Pin name<br>(function<br>after<br>reset) | Pin type | I/O structure | Notes | Pin functions                                                                             |                                                     |
|------------|--------|--------|------------------------------------------|----------|---------------|-------|-------------------------------------------------------------------------------------------|-----------------------------------------------------|
| LQFP100    | LQFP64 | LQFP48 |                                          |          |               |       | Alternate functions                                                                       | Additional functions                                |
| 52         | 34     | 26     | PB13                                     | I/O      | TTa           | -     | SPI2_SCK, I2S2_CK,<br>USART3_CTS, TIM1_CH1N,<br>TSC_G6_IO3, EVENTOUT                      | ADC3_IN5, COMP5_INP,<br>OPAMP4_VINP,<br>OPAMP3_VINP |
| 53         | 35     | 27     | PB14                                     | I/O      | TTa           | -     | SPI2_MISO, I2S2ext_SD,<br>USART3_RTS_DE,<br>TIM1_CH2N, TIM15_CH1,<br>TSC_G6_IO4, EVENTOUT | COMP3_INP, ADC4_IN4,<br>OPAMP2_VINP                 |
| 54         | 36     | 28     | PB15                                     | I/O      | TTa           | -     | SPI2_MOSI, I2S2_SD,<br>TIM1_CH3N, RTC_REFIN,<br>TIM15_CH1N, TIM15_CH2,<br>EVENTOUT        | ADC4_IN5, COMP6_INM                                 |
| 55         | -      | -      | PD8                                      | I/O      | TTa           | (1)   | USART3_TX, EVENTOUT                                                                       | ADC4_IN12, OPAMP4_VINM                              |
| 56         | -      | -      | PD9                                      | I/O      | TTa           | (1)   | USART3_RX, EVENTOUT                                                                       | ADC4_IN13                                           |
| 57         | -      | -      | PD10                                     | I/O      | TTa           | (1)   | USART3_CK, EVENTOUT                                                                       | ADC34_IN7, COMP6_INM                                |
| 58         | -      | -      | PD11                                     | I/O      | TTa           | (1)   | USART3_CTS, EVENTOUT                                                                      | ADC34_IN8, COMP6_INP,<br>OPAMP4_VINP                |
| 59         | -      | -      | PD12                                     | I/O      | TTa           | (1)   | USART3_RTS_DE,<br>TIM4_CH1, TSC_G8_IO1,<br>EVENTOUT                                       | ADC34_IN9, COMP5_INP                                |
| 60         | -      | -      | PD13                                     | I/O      | TTa           | (1)   | TIM4_CH2, TSC_G8_IO2,<br>EVENTOUT                                                         | ADC34_IN10, COMP5_INM                               |
| 61         | -      | -      | PD14                                     | I/O      | TTa           | (1)   | TIM4_CH3, TSC_G8_IO3,<br>EVENTOUT                                                         | COMP3_INP, ADC34_IN11,<br>OPAMP2_VINP               |
| 62         | -      | -      | PD15                                     | I/O      | TTa           | (1)   | SPI2_NSS, TIM4_CH4,<br>TSC_G8_IO4, EVENTOUT                                               | COMP3_INM                                           |
| 63         | 37     | -      | PC6                                      | I/O      | FT            | (1)   | I2S2_MCK, COMP6_OUT,<br>TIM8_CH1, TIM3_CH1,<br>EVENTOUT                                   | -                                                   |
| 64         | 38     | -      | PC7                                      | I/O      | FT            | (1)   | I2S3_MCK, TIM8_CH2,<br>TIM3_CH2, COMP5_OUT,<br>EVENTOUT                                   | -                                                   |
| 65         | 39     | -      | PC8                                      | I/O      | FT            | (1)   | TIM8_CH3, TIM3_CH3,<br>COMP3_OUT, EVENTOUT                                                | -                                                   |
| 66         | 40     | -      | PC9                                      | I/O      | FT            | (1)   | TIM8_CH4, TIM8_BKIN2,<br>TIM3_CH4, I2S_CKIN,<br>EVENTOUT                                  | -                                                   |

Table 13. STM32F358xC pin definitions (continued)

| Pin number |        |        | Pin name<br>(function<br>after<br>reset) | Pin type | I/O structure | Notes | Pin functions                                                                                                   |                      |
|------------|--------|--------|------------------------------------------|----------|---------------|-------|-----------------------------------------------------------------------------------------------------------------|----------------------|
| LQFP100    | LQFP64 | LQFP48 |                                          |          |               |       | Alternate functions                                                                                             | Additional functions |
| 67         | 41     | 29     | PA8                                      | I/O      | FT            | -     | I2C2_SMBA, I2S2_MCK,<br>USART1_CK, TIM1_CH1,<br>TIM4_ETR, MCO,<br>COMP3_OUT, EVENTOUT                           | -                    |
| 68         | 42     | 30     | PA9                                      | I/O      | FTf           | -     | I2C2_SCL, I2S3_MCK,<br>USART1_TX, TIM1_CH2,<br>TIM2_CH3, TIM15_BKIN,<br>TSC_G4_IO1, COMP5_OUT,<br>EVENTOUT      | -                    |
| 69         | 43     | 31     | PA10                                     | I/O      | FTf           | -     | I2C2_SDA, USART1_RX,<br>TIM1_CH3, TIM2_CH4,<br>TIM8_BKIN, TIM17_BKIN,<br>TSC_G4_IO2, COMP6_OUT,<br>EVENTOUT     | -                    |
| 70         | 44     | 32     | PA11                                     | I/O      | FT            | -     | USART1_CTS, CAN_RX,<br>TIM1_CH1N, TIM1_CH4,<br>TIM1_BKIN2, TIM4_CH1,<br>COMP1_OUT, EVENTOUT                     | -                    |
| 71         | 45     | 33     | PA12                                     | I/O      | FT            | -     | USART1_RTS_DE, CAN_TX,<br>TIM1_CH2N, TIM1_ETR,<br>TIM4_CH2, TIM16_CH1,<br>COMP2_OUT, EVENTOUT                   | -                    |
| 72         | 46     | 34     | PA13                                     | I/O      | FT            | -     | USART3_CTS, TIM4_CH3,<br>TIM16_CH1N, TSC_G4_IO3,<br>IR_OUT, SWDIO-JTMS,<br>EVENTOUT                             | -                    |
| 73         | -      | -      | PF6                                      | I/O      | FTf           | (1)   | I2C2_SCL, USART3_RTS_DE,<br>TIM4_CH4, EVENTOUT                                                                  | -                    |
| 74         | 47     | 35     | VSS_3                                    | S        | -             | -     | Ground                                                                                                          |                      |
| 75         | 48     | 36     | VDD_3                                    | S        | -             | -     | Digital power supply                                                                                            |                      |
| 76         | 49     | 37     | PA14                                     | I/O      | FTf           | -     | I2C1_SDA, USART2_TX,<br>TIM8_CH2, TIM1_BKIN,<br>TSC_G4_IO4, SWCLK-JTCK,<br>EVENTOUT                             | -                    |
| 77         | 50     | 38     | PA15                                     | I/O      | FTf           | -     | I2C1_SCL, SPI1_NSS,<br>SPI3_NSS, I2S3_WS, JTDI,<br>USART2_RX, TIM1_BKIN,<br>TIM2_CH1_ETR, TIM8_CH1,<br>EVENTOUT | -                    |

Table 13. STM32F358xC pin definitions (continued)

| Pin number |        |        | Pin name<br>(function<br>after<br>reset) | Pin type | I/O structure | Notes | Pin functions                                                                                                                        |                      |
|------------|--------|--------|------------------------------------------|----------|---------------|-------|--------------------------------------------------------------------------------------------------------------------------------------|----------------------|
| LQFP100    | LQFP64 | LQFP48 |                                          |          |               |       | Alternate functions                                                                                                                  | Additional functions |
| 78         | 51     | -      | PC10                                     | I/O      | FT            | (1)   | SPI3_SCK, I2S3_CK,<br>USART3_TX, UART4_TX,<br>TIM8_CH1N, EVENTOUT                                                                    | -                    |
| 79         | 52     | -      | PC11                                     | I/O      | FT            | (1)   | SPI3_MISO, I2S3ext_SD,<br>USART3_RX, UART4_RX,<br>TIM8_CH2N, EVENTOUT                                                                | -                    |
| 80         | 53     | -      | PC12                                     | I/O      | FT            | (1)   | SPI3_MOSI, I2S3_SD,<br>USART3_CK, UART5_TX,<br>TIM8_CH3N, EVENTOUT                                                                   | -                    |
| 81         | -      | -      | PD0                                      | I/O      | FT            | (1)   | CAN_RX, EVENTOUT                                                                                                                     | -                    |
| 82         | -      | -      | PD1                                      | I/O      | FT            | (1)   | CAN_TX, TIM8_CH4,<br>TIM8_BKIN2, EVENTOUT                                                                                            | -                    |
| 83         | 54     | -      | PD2                                      | I/O      | FT            | (1)   | UART5_RX, TIM3_ETR,<br>TIM8_BKIN, EVENTOUT                                                                                           | -                    |
| 84         | -      | -      | PD3                                      | I/O      | FT            | (1)   | USART2_CTS,<br>TIM2_CH1_ETR, EVENTOUT                                                                                                | -                    |
| 85         | -      | -      | PD4                                      | I/O      | FT            | (1)   | USART2_RTS_DE,<br>TIM2_CH2, EVENTOUT                                                                                                 | -                    |
| 86         | -      | -      | PD5                                      | I/O      | FT            | (1)   | USART2_TX, EVENTOUT                                                                                                                  | -                    |
| 87         | -      | -      | PD6                                      | I/O      | FT            | (1)   | USART2_RX, TIM2_CH4,<br>EVENTOUT                                                                                                     | -                    |
| 88         | -      | -      | PD7                                      | I/O      | FT            | (1)   | USART2_CK, TIM2_CH3,<br>EVENTOUT                                                                                                     | -                    |
| 89         | 55     | 39     | PB3                                      | I/O      | FT            | -     | SPI3_SCK, I2S3_CK,<br>SPI1_SCK, USART2_TX,<br>TIM2_CH2, TIM3_ETR,<br>TIM4_ETR, TIM8_CH1N,<br>TSC_G5_IO1, JTDO-<br>TRACESWO, EVENTOUT | -                    |
| 90         | 56     | 40     | PB4                                      | I/O      | FT            | -     | SPI3_MISO, I2S3ext_SD,<br>SPI1_MISO, USART2_RX,<br>TIM3_CH1, TIM16_CH1,<br>TIM17_BKIN, TIM8_CH2N,<br>TSC_G5_IO2, NJTRST,<br>EVENTOUT | -                    |
| 91         | 57     | 41     | PB5                                      | I/O      | FT            | -     | SPI3_MOSI, SPI1_MOSI,<br>I2S3_SD, I2C1_SMBA,<br>USART2_CK, TIM16_BKIN,<br>TIM3_CH2, TIM8_CH3N,<br>TIM17_CH1, EVENTOUT                | -                    |

Table 13. STM32F358xC pin definitions (continued)

| Pin number |        |        | Pin name<br>(function<br>after<br>reset) | Pin type | I/O structure | Notes | Pin functions                                                                                               |                      |
|------------|--------|--------|------------------------------------------|----------|---------------|-------|-------------------------------------------------------------------------------------------------------------|----------------------|
| LQFP100    | LQFP64 | LQFP48 |                                          |          |               |       | Alternate functions                                                                                         | Additional functions |
| 92         | 58     | 42     | PB6                                      | I/O      | FTf           | -     | I2C1_SCL, USART1_TX,<br>TIM16_CH1N, TIM4_CH1,<br>TIM8_CH1, TSC_G5_IO3,<br>TIM8_ETR, TIM8_BKIN2,<br>EVENTOUT | -                    |
| 93         | 59     | 43     | PB7                                      | I/O      | FTf           | -     | I2C1_SDA, USART1_RX,<br>TIM3_CH4, TIM4_CH2,<br>TIM17_CH1N, TIM8_BKIN,<br>TSC_G5_IO4, EVENTOUT               | -                    |
| 94         | 60     | 44     | BOOT0                                    | I        | B             | -     | Boot memory selection                                                                                       |                      |
| 95         | 61     | 45     | PB8                                      | I/O      | FTf           | -     | I2C1_SCL, CAN_RX,<br>TIM16_CH1, TIM4_CH3,<br>TIM8_CH2, TIM1_BKIN,<br>TSC_SYNC, COMP1_OUT,<br>EVENTOUT       | -                    |
| 96         | 62     | 46     | PB9                                      | I/O      | FTf           | -     | I2C1_SDA, CAN_TX,<br>TIM17_CH1, TIM4_CH4,<br>TIM8_CH3, IR_OUT,<br>COMP2_OUT, EVENTOUT                       | -                    |
| 97         | -      | -      | PE0                                      | I/O      | FT            | (1)   | USART1_TX, TIM4_ETR,<br>TIM16_CH1, EVENTOUT                                                                 | -                    |
| 98         | -      | -      | PE1                                      | I/O      | FT            | (1)   | USART1_RX, TIM17_CH1,<br>EVENTOUT                                                                           | -                    |
| 99         | 63     | 47     | VSS_1                                    | S        | -             | -     | Ground                                                                                                      |                      |
| 100        | 64     | 48     | VDD_1                                    | S        | -             | -     | Digital power supply                                                                                        |                      |

- Function availability depends on the chosen device.  
When using the small packages (48 and 64 pin packages), the GPIO pins which are not present on these packages, must not be configured in analog mode.
- PC13, PC14 and PC15 are supplied through the power switch. Since the switch sinks only a limited amount of current (3 mA), the use of GPIO PC13 to PC15 in output mode is limited:
  - The speed should not exceed 2 MHz with a maximum load of 30 pF
  - These GPIOs must not be used as current sources (e.g. to drive an LED).

After the first backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the Backup registers which is not reset by the main reset. For details on how to manage these GPIOs, refer to the Battery backup domain and BKP register description sections in the reference manual.

- These GPIOs offer a reduced touch sensing sensitivity. It is thus recommended to use them as sampling capacitor I/O
- This pin is powered by VDDA.

Table 14. Alternate functions for port A

| Port & Pin Name | AF0       | AF1          | AF2      | AF3        | AF4       | AF5       | AF6               | AF7           | AF8       | AF9        | AF10     | AF11      | AF12       | AF14 | AF15      |
|-----------------|-----------|--------------|----------|------------|-----------|-----------|-------------------|---------------|-----------|------------|----------|-----------|------------|------|-----------|
| PA0             | -         | TIM2_CH1_ETR | -        | TSC_G1_IO1 | -         | -         | -                 | USART2_CTS    | COMP1_OUT | TIM8_BKIN  | TIM8_ETR | -         | -          | -    | EVENT OUT |
| PA1             | RTC_REFIN | TIM2_CH2     | -        | TSC_G1_IO2 | -         | -         | -                 | USART2_RTS_DE | -         | TIM15_CH1N | -        | -         | -          | -    | EVENT OUT |
| PA2             | -         | TIM2_CH3     | -        | TSC_G1_IO3 | -         | -         | -                 | USART2_TX     | COMP2_OUT | TIM15_CH1  | -        | -         | -          | -    | EVENT OUT |
| PA3             | -         | TIM2_CH4     | -        | TSC_G1_IO4 | -         | -         | -                 | USART2_RX     | -         | TIM15_CH2  | -        | -         | -          | -    | EVENT OUT |
| PA4             | -         |              | TIM3_CH2 | TSC_G2_IO1 | -         | SPI1_NSS  | SPI3_NSS, I2S3_WS | USART2_CK     | -         | -          | -        | -         | -          | -    | EVENT OUT |
| PA5             | -         | TIM2_CH1_ETR | -        | TSC_G2_IO2 | -         | SPI1_SCK  | -                 | -             | -         | -          | -        | -         | -          | -    | EVENT OUT |
| PA6             | -         | TIM16_CH1    | TIM3_CH1 | TSC_G2_IO3 | TIM8_BKIN | SPI1_MISO | TIM1_BKIN         | -             | COMP1_OUT | -          | -        | -         | -          | -    | EVENT OUT |
| PA7             | -         | TIM17_CH1    | TIM3_CH2 | TSC_G2_IO4 | TIM8_CH1N | SPI1_MOSI | TIM1_CH1N         | -             | COMP2_OUT | -          | -        | -         | -          | -    | EVENT OUT |
| PA8             | MCO       | -            | -        | -          | I2C2_SMBA | I2S2_MCK  | TIM1_CH1          | USART1_CK     | COMP3_OUT | -          | TIM4_ETR | -         | -          | -    | EVENT OUT |
| PA9             | -         | -            | -        | TSC_G4_IO1 | I2C2_SCL  | I2S3_MCK  | TIM1_CH2          | USART1_TX     | COMP5_OUT | TIM15_BKIN | TIM2_CH3 | -         | -          | -    | EVENT OUT |
| PA10            | -         | TIM17_BKIN   | -        | TSC_G4_IO2 | I2C2_SDA  | -         | TIM1_CH3          | USART1_RX     | COMP6_OUT | -          | TIM2_CH4 | TIM8_BKIN | -          | -    | EVENT OUT |
| PA11            | -         | -            | -        | -          | -         | -         | TIM1_CH1N         | USART1_CTS    | COMP1_OUT | CAN_RX     | TIM4_CH1 | TIM1_CH4  | TIM1_BKIN2 | -    | EVENT OUT |



Table 14. Alternate functions for port A (continued)

| Port & Pin Name | AF0        | AF1          | AF2      | AF3        | AF4      | AF5      | AF6               | AF7           | AF8       | AF9       | AF10     | AF11     | AF12 | AF14 | AF15      |
|-----------------|------------|--------------|----------|------------|----------|----------|-------------------|---------------|-----------|-----------|----------|----------|------|------|-----------|
| PA12            | -          | TIM16_CH1    | -        | -          | -        | -        | TIM1_CH2N         | USART1_RTS_DE | COMP2_OUT | CAN_TX    | TIM4_CH2 | TIM1_ETR | -    | -    | EVENT OUT |
| PA13            | SWDIO-JTMS | TIM16_CH1N   | -        | TSC_G4_IO3 | -        | IR_OUT   | -                 | USART3_CTS    | -         | -         | TIM4_CH3 | -        | -    | -    | EVENT OUT |
| PA14            | SWCLK-JTCK | -            | -        | TSC_G4_IO4 | I2C1_SDA | TIM8_CH2 | TIM1_BKIN         | USART2_TX     | -         | -         | -        | -        | -    | -    | EVENT OUT |
| PA15            | JTDI       | TIM2_CH1_ETR | TIM8_CH1 | -          | I2C1_SCL | SPI1_NSS | SPI3_NSS, I2S3_WS | USART2_RX     | -         | TIM1_BKIN | -        | -        | -    | -    | EVENT OUT |

Table 15. Alternate functions for port B

| Port & Pin Name | AF0            | AF1        | AF2      | AF3        | AF4       | AF5               | AF6                   | AF7        | AF8       | AF9    | AF10       | AF12      | AF15      |
|-----------------|----------------|------------|----------|------------|-----------|-------------------|-----------------------|------------|-----------|--------|------------|-----------|-----------|
| PB0             | -              | -          | TIM3_CH3 | TSC_G3_IO2 | TIM8_CH2N | -                 | TIM1_CH2N             | -          | -         | -      | -          | -         | EVENT OUT |
| PB1             | -              | -          | TIM3_CH4 | TSC_G3_IO3 | TIM8_CH3N | -                 | TIM1_CH3N             | -          | COMP4_OUT | -      | -          | -         | EVENT OUT |
| PB3             | JTDO-TRACES WO | TIM2_CH2   | TIM4_ETR | TSC_G5_IO1 | TIM8_CH1N | SPI1_SCK          | SPI3_SCK, I2S3_CK     | USART2_TX  | -         | -      | TIM3_ETR   | -         | EVENT OUT |
| PB4             | NJTRST         | TIM16_CH1  | TIM3_CH1 | TSC_G5_IO2 | TIM8_CH2N | SPI1_MISO         | SPI3_MISO, I2S3ext_SD | USART2_RX  | -         | -      | TIM17_BKIN | -         | EVENT OUT |
| PB5             | -              | TIM16_BKIN | TIM3_CH2 | TIM8_CH3N  | I2C1_SMBA | SPI1_MOSI         | SPI3_MOSI, I2S3_SD    | USART2_CK  | -         | -      | TIM17_CH1  | -         | EVENT OUT |
| PB6             | -              | TIM16_CH1N | TIM4_CH1 | TSC_G5_IO3 | I2C1_SCL  | TIM8_CH1          | TIM8_ETR              | USART1_TX  | -         | -      | TIM8_BKIN2 | -         | EVENT OUT |
| PB7             | -              | TIM17_CH1N | TIM4_CH2 | TSC_G5_IO4 | I2C1_SDA  | TIM8_BKIN         | -                     | USART1_RX  | -         | -      | TIM3_CH4   | -         | EVENT OUT |
| PB8             | -              | TIM16_CH1  | TIM4_CH3 | TSC_SYNC   | I2C1_SCL  | -                 | -                     | -          | COMP1_OUT | CAN_RX | TIM8_CH2   | TIM1_BKIN | EVENT OUT |
| PB9             | -              | TIM17_CH1  | TIM4_CH4 | -          | I2C1_SDA  | -                 | IR_OUT                | -          | COMP2_OUT | CAN_TX | TIM8_CH3   | -         | EVENT OUT |
| PB10            | -              | TIM2_CH3   | -        | TSC_SYNC   | -         | -                 | -                     | USART3_TX  | -         | -      | -          | -         | EVENT OUT |
| PB11            | -              | TIM2_CH4   | -        | TSC_G6_IO1 | -         | -                 | -                     | USART3_RX  | -         | -      | -          | -         | EVENT OUT |
| PB12            | -              | -          | -        | TSC_G6_IO2 | I2C2_SMBA | SPI2_NSS, I2S2_WS | TIM1_BKIN             | USART3_CK  | -         | -      | -          | -         | EVENT OUT |
| PB13            | -              | -          | -        | TSC_G6_IO3 | -         | SPI2_SCK, I2S2_CK | TIM1_CH1N             | USART3_CTS | -         | -      | -          | -         | EVENT OUT |

**Table 15. Alternate functions for port B (continued)**

| Port & Pin Name | AF0           | AF1           | AF2            | AF3            | AF4           | AF5                      | AF6           | AF7               | AF8 | AF9 | AF10 | AF12 | AF15         |
|-----------------|---------------|---------------|----------------|----------------|---------------|--------------------------|---------------|-------------------|-----|-----|------|------|--------------|
| PB14            | -             | TIM15_<br>CH1 | -              | TSC_<br>G6_IO4 | -             | SPI2_MISO,<br>I2S2ext_SD | TIM1_<br>CH2N | USART3_<br>RTS_DE | -   | -   | -    | -    | EVENT<br>OUT |
| PB15            | RTC_<br>REFIN | TIM15_<br>CH2 | TIM15_<br>CH1N | -              | TIM1_<br>CH3N | SPI2_MOSI,<br>I2S2_SD    | -             | -                 | -   | -   | -    | -    | EVENT<br>OUT |

Table 16. Alternate functions for port C

| Port & Pin Name | AF1      | AF2      | AF3        | AF4       | AF5      | AF6                   | AF7       |
|-----------------|----------|----------|------------|-----------|----------|-----------------------|-----------|
| PC0             | EVENTOUT | -        | -          | -         | -        | -                     | -         |
| PC1             | EVENTOUT | -        | -          | -         | -        | -                     | -         |
| PC2             | EVENTOUT | -        | COMP7_OUT  | -         | -        | -                     | -         |
| PC3             | EVENTOUT | -        | -          | -         | -        | TIM1_BKIN2            | -         |
| PC4             | EVENTOUT | -        | -          | -         | -        | -                     | USART1_TX |
| PC5             | EVENTOUT |          | TSC_G3_IO1 | -         | -        | -                     | USART1_RX |
| PC6             | EVENTOUT | TIM3_CH1 | -          | TIM8_CH1  | -        | I2S2_MCK              | COMP6_OUT |
| PC7             | EVENTOUT | TIM3_CH2 | -          | TIM8_CH2  | -        | I2S3_MCK              | COMP5_OUT |
| PC8             | EVENTOUT | TIM3_CH3 | -          | TIM8_CH3  | -        | -                     | COMP3_OUT |
| PC9             | EVENTOUT | TIM3_CH4 | -          | TIM8_CH4  | I2S_CKIN | TIM8_BKIN2            | -         |
| PC10            | EVENTOUT | -        | -          | TIM8_CH1N | UART4_TX | SPI3_SCK, I2S3_CK     | USART3_TX |
| PC11            | EVENTOUT | -        | -          | TIM8_CH2N | UART4_RX | SPI3_MISO, I2S3ext_SD | USART3_RX |
| PC12            | EVENTOUT | -        | -          | TIM8_CH3N | UART5_TX | SPI3_MOSI, I2S3_SD    | USART3_CK |
| PC13            | -        | -        | -          | TIM1_CH1N | -        | -                     | -         |
| PC14            | -        | -        | -          | -         | -        | -                     | -         |
| PC15            | -        | -        | -          | -         | -        | -                     | -         |



Table 17. Alternate functions for port D

| Port & Pin Name | AF1      | AF2          | AF3        | AF4       | AF5      | AF6        | AF7           |
|-----------------|----------|--------------|------------|-----------|----------|------------|---------------|
| PD0             | EVENTOUT | -            | -          | -         | -        | -          | CAN_RX        |
| PD1             | EVENTOUT |              | -          | TIM8_CH4  | -        | TIM8_BKIN2 | -             |
| PD2             | EVENTOUT | TIM3_ETR     | -          | TIM8_BKIN | UART5_RX | -          | -             |
| PD3             | EVENTOUT | TIM2_CH1_ETR | -          | -         | -        | -          | USART2_CTS    |
| PD4             | EVENTOUT | TIM2_CH2     | -          | -         | -        | -          | USART2_RTS_DE |
| PD5             | EVENTOUT | -            | -          | -         | -        | -          | USART2_TX     |
| PD6             | EVENTOUT | TIM2_CH4     | -          | -         | -        | -          | USART2_RX     |
| PD7             | EVENTOUT | TIM2_CH3     | -          | -         | -        | -          | USART2_CK     |
| PD8             | EVENTOUT | -            | -          | -         | -        |            | USART3_TX     |
| PD9             | EVENTOUT | -            | -          | -         | -        | -          | USART3_RX     |
| PD10            | EVENTOUT | -            | -          | -         | -        | -          | USART3_CK     |
| PD11            | EVENTOUT | -            | -          | -         | -        | -          | USART3_CTS    |
| PD12            | EVENTOUT | TIM4_CH1     | TSC_G8_IO1 | -         | -        | -          | USART3_RTS_DE |
| PD13            | EVENTOUT | TIM4_CH2     | TSC_G8_IO2 | -         | -        | -          | -             |
| PD14            | EVENTOUT | TIM4_CH3     | TSC_G8_IO3 | -         | -        | -          | -             |
| PD15            | EVENTOUT | TIM4_CH4     | TSC_G8_IO4 | -         | -        | SPI2_NSS   | -             |

Table 18. Alternate functions for port E

| Port &<br>Pin Name | AF0     | AF1      | AF2       | AF3        | AF4       | AF6        | AF7       |
|--------------------|---------|----------|-----------|------------|-----------|------------|-----------|
| PE0                | -       | EVENTOUT | TIM4_ETR  | -          | TIM16_CH1 | -          | USART1_TX |
| PE1                | -       | EVENTOUT | -         | -          | TIM17_CH1 | -          | USART1_RX |
| PE2                | TRACECK | EVENTOUT | TIM3_CH1  | TSC_G7_IO1 | -         | -          | -         |
| PE3                | TRACED0 | EVENTOUT | TIM3_CH2  | TSC_G7_IO2 | -         | -          | -         |
| PE4                | TRACED1 | EVENTOUT | TIM3_CH3  | TSC_G7_IO3 | -         | -          | -         |
| PE5                | TRACED2 | EVENTOUT | TIM3_CH4  | TSC_G7_IO4 | -         | -          | -         |
| PE6                | TRACED3 | EVENTOUT | -         | -          | -         | -          | -         |
| PE7                | -       | EVENTOUT | TIM1_ETR  | -          | -         | -          | -         |
| PE8                | -       | EVENTOUT | TIM1_CH1N | -          | -         | -          | -         |
| PE9                | -       | EVENTOUT | TIM1_CH1  | -          | -         | -          | -         |
| PE10               | -       | EVENTOUT | TIM1_CH2N | -          | -         | -          | -         |
| PE11               | -       | EVENTOUT | TIM1_CH2  | -          | -         | -          | -         |
| PE12               | -       | EVENTOUT | TIM1_CH3N | -          | -         | -          | -         |
| PE13               | -       | EVENTOUT | TIM1_CH3  | -          | -         | -          | -         |
| PE14               | -       | EVENTOUT | TIM1_CH4  | -          | -         | TIM1_BKIN2 | -         |
| PE15               | -       | EVENTOUT | TIM1_BKIN | -          | -         | -          | USART3_RX |

Table 19. Alternate functions for port F

| Port &<br>Pin Name | AF1      | AF2       | AF3       | AF4      | AF5      | AF6       | AF7           |
|--------------------|----------|-----------|-----------|----------|----------|-----------|---------------|
| PF0                | -        | -         | -         | I2C2_SDA | -        | TIM1_CH3N | -             |
| PF1                | -        | -         | -         | I2C2_SCL | -        | -         | -             |
| PF2                | EVENTOUT | -         | -         | -        | -        | -         | -             |
| PF4                | EVENTOUT | COMP1_OUT | -         | -        | -        | -         |               |
| PF6                | EVENTOUT | TIM4_CH4  |           | I2C2_SCL | -        | -         | USART3_RTS_DE |
| PF9                | EVENTOUT | -         | TIM15_CH1 | -        | SPI2_SCK | -         | -             |
| PF10               | EVENTOUT | -         | TIM15_CH2 | -        | SPI2_SCK | -         | -             |

## 5 Memory mapping

### Figure 7. STM32F358xC memory map

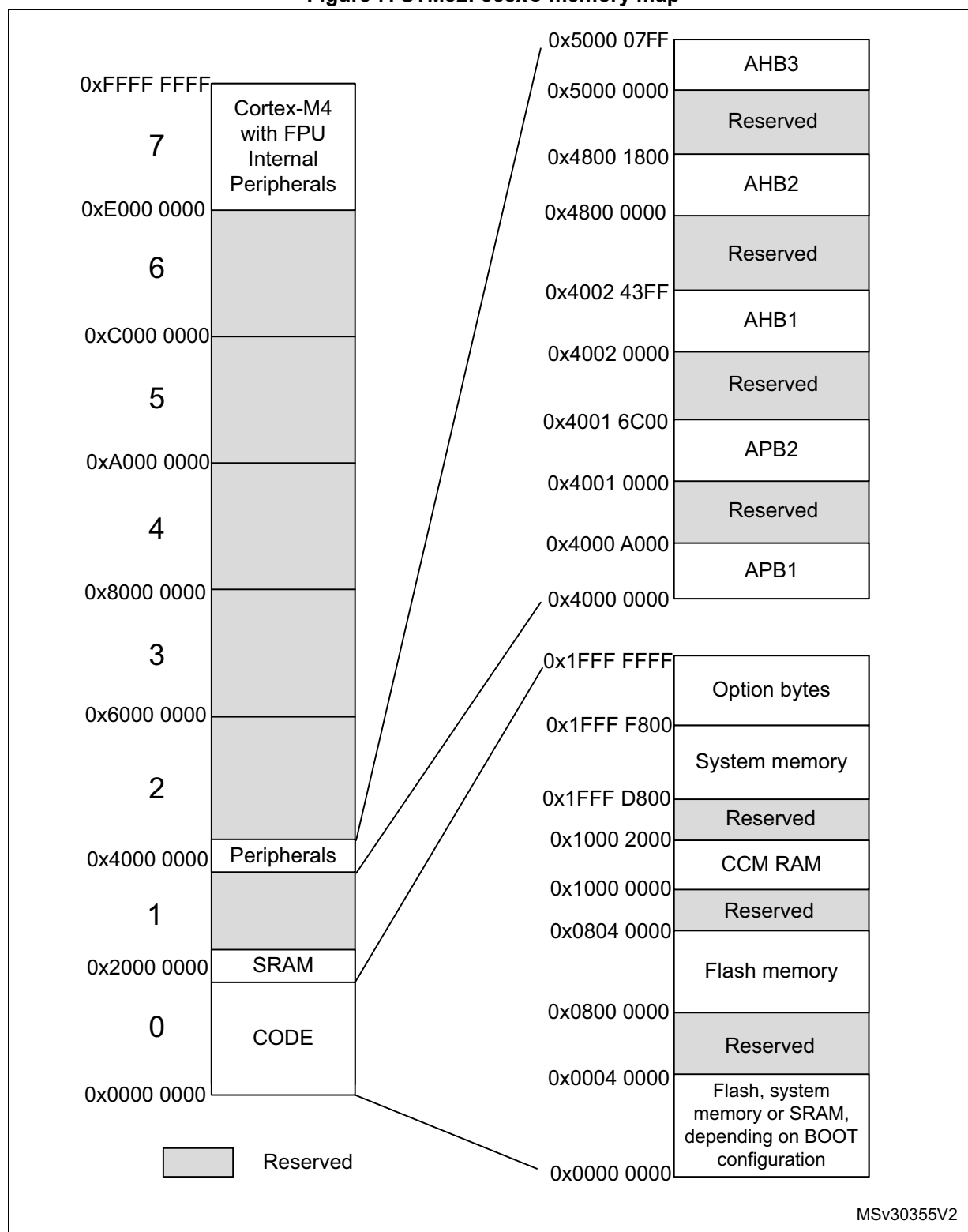


Table 20. STM32F358xC memory map and peripheral register boundary addresses

| Bus  | Boundary address          | Size (bytes) | Peripheral            |
|------|---------------------------|--------------|-----------------------|
| AHB3 | 0x5000 0400 - 0x5000 07FF | 1 K          | ADC3 - ADC4           |
|      | 0x5000 0000 - 0x5000 03FF | 1 K          | ADC1 - ADC2           |
|      | 0x4800 1800 - 0x4FFF FFFF | ~132 M       | Reserved              |
| AHB2 | 0x4800 1400 - 0x4800 17FF | 1 K          | GPIOF                 |
|      | 0x4800 1000 - 0x4800 13FF | 1 K          | GPIOE                 |
|      | 0x4800 0C00 - 0x4800 0FFF | 1 K          | GPIOD                 |
|      | 0x4800 0800 - 0x4800 0BFF | 1 K          | GPIOC                 |
|      | 0x4800 0400 - 0x4800 07FF | 1 K          | GPIOB                 |
|      | 0x4800 0000 - 0x4800 03FF | 1 K          | GPIOA                 |
|      | 0x4002 4400 - 0x47FF FFFF | ~128 M       | Reserved              |
| AHB1 | 0x4002 4000 - 0x4002 43FF | 1 K          | TSC                   |
|      | 0x4002 3400 - 0x4002 3FFF | 3 K          | Reserved              |
|      | 0x4002 3000 - 0x4002 33FF | 1 K          | CRC                   |
|      | 0x4002 2400 - 0x4002 2FFF | 3 K          | Reserved              |
|      | 0x4002 2000 - 0x4002 23FF | 1 K          | Flash interface       |
|      | 0x4002 1400 - 0x4002 1FFF | 3 K          | Reserved              |
|      | 0x4002 1000 - 0x4002 13FF | 1 K          | RCC                   |
|      | 0x4002 0800 - 0x4002 0FFF | 2 K          | Reserved              |
|      | 0x4002 0400 - 0x4002 07FF | 1 K          | DMA2                  |
|      | 0x4002 0000 - 0x4002 03FF | 1 K          | DMA1                  |
|      | 0x4001 8000 - 0x4001 FFFF | 32 K         | Reserved              |
| APB2 | 0x4001 4C00 - 0x4001 7FFF | 13 K         | Reserved              |
|      | 0x4001 4800 - 0x4001 4BFF | 1 K          | TIM17                 |
|      | 0x4001 4400 - 0x4001 47FF | 1 K          | TIM16                 |
|      | 0x4001 4000 - 0x4001 43FF | 1 K          | TIM15                 |
|      | 0x4001 3C00 - 0x4001 3FFF | 1 K          | Reserved              |
|      | 0x4001 3800 - 0x4001 3BFF | 1 K          | USART1                |
|      | 0x4001 3400 - 0x4001 37FF | 1 K          | TIM8                  |
|      | 0x4001 3000 - 0x4001 33FF | 1 K          | SPI1                  |
|      | 0x4001 2C00 - 0x4001 2FFF | 1 K          | TIM1                  |
|      | 0x4001 0800 - 0x4001 2BFF | 9 K          | Reserved              |
|      | 0x4001 0400 - 0x4001 07FF | 1 K          | EXTI                  |
|      | 0x4001 0000 - 0x4001 03FF | 1 K          | SYSCFG + COMP + OPAMP |

Table 20. STM32F358xC memory map and peripheral register boundary addresses (continued)

| Bus  | Boundary address          | Size (bytes) | Peripheral |
|------|---------------------------|--------------|------------|
|      | 0x4000 8000 - 0x4000 FFFF | 32 K         | Reserved   |
| APB1 | 0x4000 7800 - 0x4000 7FFF | 2 K          | Reserved   |
|      | 0x4000 7400 - 0x4000 77FF | 1 K          | DAC (dual) |
|      | 0x4000 7000 - 0x4000 73FF | 1 K          | PWR        |
|      | 0x4000 6C00 - 0x4000 6FFF | 1 K          | Reserved   |
|      | 0x4000 6800 - 0x4000 6BFF | 1 K          | Reserved   |
|      | 0x4000 6400 - 0x4000 67FF | 1 K          | bxCAN      |
|      | 0x4000 5C00 - 0x4000 63FF | 2 K          | Reserved   |
|      | 0x4000 5800 - 0x4000 5BFF | 1 K          | I2C2       |
|      | 0x4000 5400 - 0x4000 57FF | 1 K          | I2C1       |
|      | 0x4000 5000 - 0x4000 53FF | 1 K          | UART5      |
|      | 0x4000 4C00 - 0x4000 4FFF | 1 K          | UART4      |
|      | 0x4000 4800 - 0x4000 4BFF | 1 K          | USART3     |
|      | 0x4000 4400 - 0x4000 47FF | 1 K          | USART2     |
|      | 0x4000 4000 - 0x4000 43FF | 1 K          | I2S3ext    |
|      | 0x4000 3C00 - 0x4000 3FFF | 1 K          | SPI3/I2S3  |
|      | 0x4000 3800 - 0x4000 3BFF | 1 K          | SPI2/I2S2  |
|      | 0x4000 3400 - 0x4000 37FF | 1 K          | I2S2ext    |
|      | 0x4000 3000 - 0x4000 33FF | 1 K          | IWDG       |
|      | 0x4000 2C00 - 0x4000 2FFF | 1 K          | WWDG       |
|      | 0x4000 2800 - 0x4000 2BFF | 1 K          | RTC        |
|      | 0x4000 1800 - 0x4000 27FF | 4 K          | Reserved   |
|      | 0x4000 1400 - 0x4000 17FF | 1 K          | TIM7       |
|      | 0x4000 1000 - 0x4000 13FF | 1 K          | TIM6       |
|      | 0x4000 0C00 - 0x4000 0FFF | 1 K          | Reserved   |
|      | 0x4000 0800 - 0x4000 0BFF | 1 K          | TIM4       |
|      | 0x4000 0400 - 0x4000 07FF | 1 K          | TIM3       |
|      | 0x4000 0000 - 0x4000 03FF | 1 K          | TIM2       |

## 6 Electrical characteristics

### 6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to  $V_{SS}$ .

#### 6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at  $T_A = 25\text{ }^{\circ}\text{C}$  and  $T_A = T_{A\text{max}}$  (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation ( $\text{mean} \pm 3\sigma$ ).

#### 6.1.2 Typical values

Unless otherwise specified, typical data are based on  $T_A = 25\text{ }^{\circ}\text{C}$ ,  $V_{DD} = 1.8\text{ V}$ ,  $V_{DDA} = 3.3\text{ V}$ . They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated ( $\text{mean} \pm 2\sigma$ ).

#### 6.1.3 Typical curves

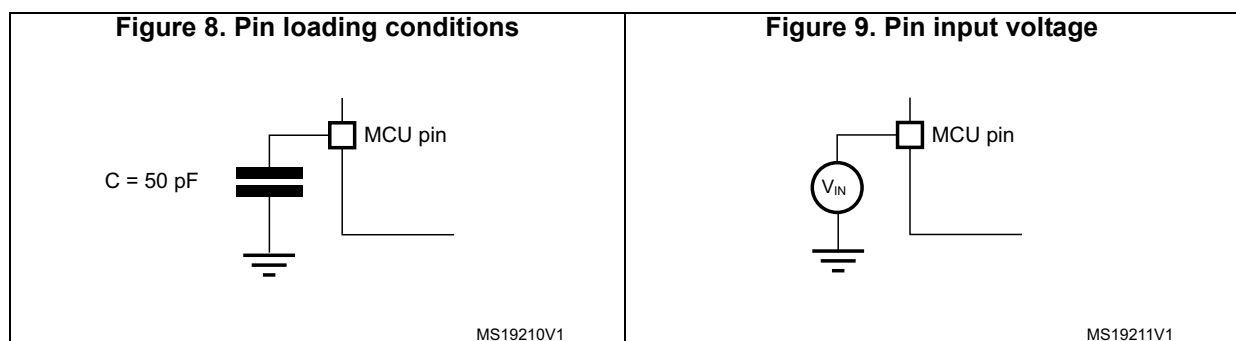
Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

#### 6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 8](#).

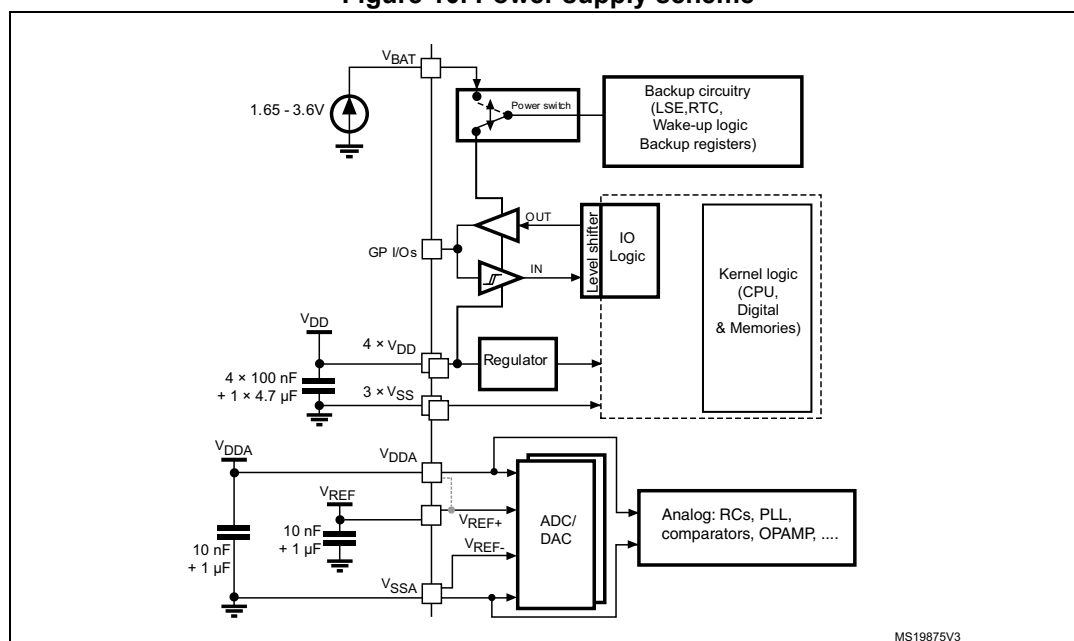
#### 6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 9](#).



### 6.1.6 Power supply scheme

Figure 10. Power supply scheme

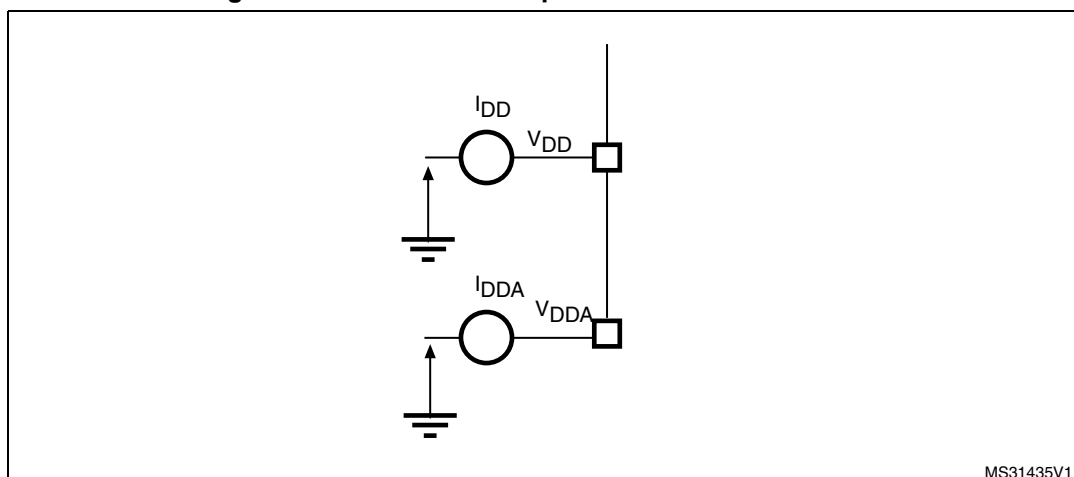


1. Dotted lines represent the internal connections on low pin count packages, joining the dedicated supply pins.

**Caution:** Each power supply pair ( $V_{DD}/V_{SS}$ ,  $V_{DDA}/V_{SSA}$  etc..) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

### 6.1.7 Current consumption measurement

Figure 11. Current consumption measurement scheme



## 6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 21: Voltage characteristics](#), [Table 22: Current characteristics](#), and [Table 23: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 21. Voltage characteristics<sup>(1)</sup>**

| Symbol                            | Ratings                                                             | Min                                                                        | Max             | Unit |
|-----------------------------------|---------------------------------------------------------------------|----------------------------------------------------------------------------|-----------------|------|
| $V_{DD}-V_{SS}$                   | External digital supply voltage (including $V_{DD}$ and $V_{BAT}$ ) | -0.3                                                                       | 1.95            | V    |
| $V_{DDA}-V_{SS}$                  | External analog supply voltage                                      | -0.3                                                                       | 4.0             |      |
| $V_{DD}-V_{DDA}$                  | Allowed voltage difference for $V_{DD} > V_{DDA}$                   | -                                                                          | 0.4             |      |
| $V_{REF+}-V_{DDA}$ <sup>(2)</sup> | Allowed voltage difference for $V_{REF+} > V_{DDA}$                 | -                                                                          | 0.4             |      |
| $V_{IN}$ <sup>(3)</sup>           | Input voltage on FT and FTf pins                                    | $V_{SS} - 0.3$                                                             | $V_{DD} + 4.0$  |      |
|                                   | Input voltage on TTa pins                                           | $V_{SS} - 0.3$                                                             | 4.0             |      |
|                                   | Input voltage on any other pin                                      | $V_{SS} - 0.3$                                                             | 4.0             |      |
|                                   | Input voltage on POR pin                                            | $V_{SS} - 0.3$                                                             | $V_{DDA} + 4.0$ |      |
|                                   | Input Voltage on B Pin                                              | 0                                                                          | 9               |      |
| $ \Delta V_{DDx} $                | Variations between different $V_{DD}$ power pins                    | -                                                                          | 50              | mV   |
| $ V_{SSx}-V_{SS} $                | Variations between all the different ground pins                    | -                                                                          | 50              |      |
| $V_{ESD(HBM)}$                    | Electrostatic discharge voltage (human body model)                  | see <a href="#">Section 6.3.11: Electrical sensitivity characteristics</a> |                 | -    |

1. All main power ( $V_{DD}$ ,  $V_{DDA}$ ) and ground ( $V_{SS}$ ,  $V_{SSA}$ ) pins must always be connected to the external power supply, in the permitted range. The following relationship must be respected between  $V_{DDA}$  and  $V_{DD}$ :  
 $V_{DDA}$  must power on before or at the same time as  $V_{DD}$  in the power up sequence.  
 $V_{DDA}$  must be greater than or equal to  $V_{DD}$ .
2.  $V_{REF+}$  must be always lower or equal than  $V_{DDA}$  ( $V_{REF+} \leq V_{DDA}$ ). If unused then it must be connected to  $V_{DDA}$ .
3.  $V_{IN}$  maximum must always be respected. Refer to [Table 22: Current characteristics](#) for the maximum allowed injected current values.

Table 22. Current characteristics

| Symbol                | Ratings                                                                        | Max.  | Unit |
|-----------------------|--------------------------------------------------------------------------------|-------|------|
| $\Sigma I_{VDD}$      | Total current into sum of all VDD_x power lines (source)                       | 160   | mA   |
| $\Sigma I_{VSS}$      | Total current out of sum of all VSS_x ground lines (sink)                      | -160  |      |
| $I_{VDD}$             | Maximum current into each VDD_x power line (source) <sup>(1)</sup>             | 100   |      |
| $I_{VSS}$             | Maximum current out of each VSS_x ground line (sink) <sup>(1)</sup>            | -100  |      |
| $I_{IO(PIN)}$         | Output current sunk by any I/O and control pin                                 | 25    |      |
|                       | Output current source by any I/O and control pin                               | -25   |      |
| $\Sigma I_{IO(PIN)}$  | Total output current sunk by sum of all IOs and control pins <sup>(2)</sup>    | 80    |      |
|                       | Total output current sourced by sum of all IOs and control pins <sup>(2)</sup> | -80   |      |
| $I_{INJ(PIN)}$        | Injected current on FT, FTf, POR and B pins <sup>(3)</sup>                     | -5/+0 |      |
|                       | Injected current on TC and RST pin <sup>(4)</sup>                              | ± 5   |      |
|                       | Injected current on TTa pins <sup>(5)</sup>                                    | ± 5   |      |
| $\Sigma I_{INJ(PIN)}$ | Total injected current (sum of all I/O and control pins) <sup>(6)</sup>        | ± 25  |      |

1. All main power (VDD, VDDA) and ground (VSS and VSSA) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by  $V_{IN} > V_{DD}$  while a negative injection is induced by  $V_{IN} < V_{SS}$ .  $I_{INJ(PIN)}$  must never be exceeded. Refer to [Table 21: Voltage characteristics](#) for the maximum allowed input voltage values.
5. A positive injection is induced by  $V_{IN} > V_{DDA}$  while a negative injection is induced by  $V_{IN} < V_{SS}$ .  $I_{INJ(PIN)}$  must never be exceeded. Refer also to [Table 21: Voltage characteristics](#) for the maximum allowed input voltage values. Negative injection disturbs the analog performance of the device. See note <sup>(2)</sup> below [Table 66](#).
6. When several inputs are submitted to a current injection, the maximum  $\Sigma I_{INJ(PIN)}$  is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 23. Thermal characteristics

| Symbol    | Ratings                      | Value       | Unit |
|-----------|------------------------------|-------------|------|
| $T_{STG}$ | Storage temperature range    | -65 to +150 | °C   |
| $T_J$     | Maximum junction temperature | 150         | °C   |

## 6.3 Operating conditions

### 6.3.1 General operating conditions

Table 24. General operating conditions

| Symbol      | Parameter                                                                                                   | Conditions                                             | Min   | Max           | Unit |
|-------------|-------------------------------------------------------------------------------------------------------------|--------------------------------------------------------|-------|---------------|------|
| $f_{HCLK}$  | Internal AHB clock frequency                                                                                |                                                        | 0     | 72            | MHz  |
| $f_{PCLK1}$ | Internal APB1 clock frequency                                                                               |                                                        | 0     | 36            |      |
| $f_{PCLK2}$ | Internal APB2 clock frequency                                                                               |                                                        | 0     | 72            |      |
| $V_{DD}$    | Standard operating voltage                                                                                  |                                                        | 1.65  | 1.95          | V    |
| $V_{DDA}$   | Analog operating voltage (OPAMP and DAC not used)                                                           | Must have a potential equal to or higher than $V_{DD}$ | 1.65  | 3.6           | V    |
|             | Analog operating voltage (OPAMP and DAC used)                                                               |                                                        | 2.4   | 3.6           |      |
|             | Analog operating voltage (ADC used)                                                                         |                                                        | 1.8 V | 3.6 V         |      |
| $V_{BAT}$   | Backup operating voltage                                                                                    |                                                        | 1.65  | 3.6           | V    |
| $V_{IN}$    | I/O input voltage                                                                                           | TC I/O                                                 | -0.3  | $V_{DD}+0.3$  | V    |
|             |                                                                                                             | TTa I/O and POR I/O pins                               | -0.3  | $V_{DDA}+0.3$ |      |
|             |                                                                                                             | FT, FTf I/O pins                                       | -0.3  | 5.2           |      |
|             |                                                                                                             | BOOT0                                                  | 0     | 5.2           |      |
| $P_D$       | Power dissipation at $T_A = 85\text{ °C}$ for suffix 6 or $T_A = 105\text{ °C}$ for suffix 7 <sup>(1)</sup> | LQFP100                                                | -     | 488           | mW   |
|             |                                                                                                             | LQFP64                                                 | -     | 444           |      |
|             |                                                                                                             | LQFP48                                                 | -     | 364           |      |
| $T_A$       | Ambient temperature for 6 suffix version                                                                    | Maximum power dissipation                              | -40   | 85            | °C   |
|             |                                                                                                             | Low-power dissipation <sup>(2)</sup>                   | -40   | 105           |      |
|             | Ambient temperature for 7 suffix version                                                                    | Maximum power dissipation                              | -40   | 105           | °C   |
|             |                                                                                                             | Low-power dissipation <sup>(2)</sup>                   | -40   | 125           |      |
| $T_J$       | Junction temperature range                                                                                  | 6 suffix version                                       | -40   | 105           | °C   |
|             |                                                                                                             | 7 suffix version                                       | -40   | 125           |      |

1. If  $T_A$  is lower, higher  $P_D$  values are allowed as long as  $T_J$  does not exceed  $T_{Jmax}$  (see [Table 23: Thermal characteristics](#)).

2. In low-power dissipation state,  $T_A$  can be extended to this range as long as  $T_J$  does not exceed  $T_{Jmax}$  (see [Table 23: Thermal characteristics](#)).

### 6.3.2 Operating conditions at power-up / power-down

The parameters given in [Table 25](#) are derived from tests performed under the ambient temperature condition summarized in [Table 24](#).

**Table 25. Operating conditions at power-up / power-down**

| Symbol     | Parameter                | Conditions | Min | Max      | Unit            |
|------------|--------------------------|------------|-----|----------|-----------------|
| $t_{VDD}$  | $V_{DD}$ rise time rate  | -          | 0   | $\infty$ | $\mu\text{s/V}$ |
|            | $V_{DD}$ fall time rate  |            | 20  | $\infty$ |                 |
| $t_{VDDA}$ | $V_{DDA}$ rise time rate | -          | 0   | $\infty$ |                 |
|            | $V_{DDA}$ fall time rate |            | 20  | $\infty$ |                 |

### 6.3.3 Embedded reference voltage

The parameters given in [Table 26](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 24](#).

**Table 26. Embedded internal reference voltage**

| Symbol                           | Parameter                                                     | Conditions                                                         | Min  | Typ | Max                 | Unit                    |
|----------------------------------|---------------------------------------------------------------|--------------------------------------------------------------------|------|-----|---------------------|-------------------------|
| $V_{REFINT}$                     | Internal reference voltage                                    | $-40\text{ }^{\circ}\text{C} < T_A < +105\text{ }^{\circ}\text{C}$ | 1.16 | 1.2 | 1.25                | V                       |
|                                  |                                                               | $-40\text{ }^{\circ}\text{C} < T_A < +85\text{ }^{\circ}\text{C}$  | 1.16 | 1.2 | 1.24 <sup>(1)</sup> | V                       |
| $T_{S\_vrefint}$                 | ADC sampling time when reading the internal reference voltage | -                                                                  | 2.2  | -   | -                   | $\mu\text{s}$           |
| $V_{RERINT}$                     | Internal reference voltage spread over the temperature range  | $V_{DD} = 1.8\text{ V} \pm 10\text{ mV}$                           | -    | -   | 10 <sup>(2)</sup>   | mV                      |
| $T_{Coeff}$                      | Temperature coefficient                                       | -                                                                  | -    | -   | 100 <sup>(2)</sup>  | ppm/ $^{\circ}\text{C}$ |
| $T_{REFINT\_RDY}$ <sup>(3)</sup> | Internal reference voltage temporization                      | -                                                                  | 1.5  | 2.5 | 4.5                 | ms                      |

1. Data based on characterization results, not tested in production.
2. Guaranteed by design, not tested in production.
3. Guaranteed by design, not tested in production. Latency between the time when pin NPOR is set to 1 by the application and the time when  $V_{REFINTRDYF}$  is set to 1 by the hardware.

**Table 27. Internal reference voltage calibration values**

| Calibration value name | Description                                                                           | Memory address            |
|------------------------|---------------------------------------------------------------------------------------|---------------------------|
| $V_{REFINT\_CAL}$      | Raw data acquired at temperature of 30 $^{\circ}\text{C}$<br>$V_{DDA} = 3.3\text{ V}$ | 0x1FFF F7BA - 0x1FFF F7BB |

### 6.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in [Figure 11: Current consumption measurement scheme](#).

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

#### Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at  $V_{DD}$  or  $V_{SS}$  (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the  $f_{HCLK}$  frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states from 48 to 72 MHz)
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled  $f_{PCLK2} = f_{HCLK}$  and  $f_{PCLK1} = f_{HCLK}/2$
- When  $f_{HCLK} > 8$  MHz, the PLL is ON and the PLL input is equal to HSI/2 (4 MHz) or HSE (8 MHz) in bypass mode.

The parameters given in [Table 28](#) to [Table 37](#) are derived from tests performed under ambient temperature and supply voltage conditions summarized in [Table 24](#).

**Table 28. Typical and maximum current consumption from V<sub>DD</sub> supply  
at V<sub>DD</sub> = 1.8 V**

| Symbol          | Parameter                                        | Conditions                  | f <sub>HCLK</sub> | All peripherals enabled |                                     |       |                     | All peripherals disabled |                                     |       |                     | Unit |
|-----------------|--------------------------------------------------|-----------------------------|-------------------|-------------------------|-------------------------------------|-------|---------------------|--------------------------|-------------------------------------|-------|---------------------|------|
|                 |                                                  |                             |                   | Typ                     | Max @ T <sub>A</sub> <sup>(1)</sup> |       |                     | Typ                      | Max @ T <sub>A</sub> <sup>(1)</sup> |       |                     |      |
|                 |                                                  |                             |                   |                         | 25 °C                               | 85 °C | 105 °C              |                          | 25 °C                               | 85 °C | 105 °C              |      |
| I <sub>DD</sub> | Supply current in Run mode, executing from Flash | External clock (HSE bypass) | 72 MHz            | 60.4                    | 65.4                                | 66.6  | 67.8                | 27.3                     | 29.6                                | 30.3  | 31.0                | mA   |
|                 |                                                  |                             | 64 MHz            | 54.1                    | 58.6                                | 59.8  | 60.9                | 24.5                     | 26.5                                | 27.3  | 27.9                |      |
|                 |                                                  |                             | 48 MHz            | 41.5                    | 45.0                                | 46.1  | 47.0                | 18.8                     | 20.4                                | 21.0  | 21.7                |      |
|                 |                                                  |                             | 32 MHz            | 28.2                    | 30.6                                | 31.6  | 32.4                | 12.9                     | 14.0                                | 14.5  | 15.1                |      |
|                 |                                                  |                             | 24 MHz            | 21.5                    | 23.4                                | 24.2  | 24.9                | 9.8                      | 10.8                                | 11.3  | 11.8                |      |
|                 |                                                  |                             | 8 MHz             | 7.2                     | 8.0                                 | 8.6   | 9.1                 | 3.3                      | 3.8                                 | 4.1   | 4.8                 |      |
|                 |                                                  |                             | 1 MHz             | 1.1                     | 1.4                                 | 1.6   | 2.4                 | 0.6                      | 0.8                                 | 1.1   | 1.9                 |      |
|                 |                                                  | Internal clock (HSI)        | 64 MHz            | 49.4                    | 53.6                                | 54.6  | 55.7                | 24.3                     | 26.3                                | 27.0  | 27.6                |      |
|                 |                                                  |                             | 48 MHz            | 37.9                    | 41.2                                | 42.1  | 43.0                | 18.6                     | 20.3                                | 20.8  | 21.4                |      |
|                 |                                                  |                             | 32 MHz            | 25.8                    | 28.1                                | 29.0  | 29.7                | 12.7                     | 13.9                                | 14.4  | 14.9                |      |
|                 |                                                  |                             | 24 MHz            | 19.7                    | 21.4                                | 22.3  | 22.9                | 6.6                      | 7.3                                 | 7.8   | 8.3                 |      |
|                 |                                                  |                             | 8 MHz             | 6.8                     | 7.5                                 | 8.0   | 8.6                 | 3.3                      | 3.7                                 | 4.1   | 4.8                 |      |
|                 | Supply current in Run mode, executing from RAM   | External clock (HSE bypass) | 72 MHz            | 61.3                    | 66,5 <sup>(2)</sup>                 | 67.6  | 68,9 <sup>(2)</sup> | 28.3                     | 30,6 <sup>(2)</sup>                 | 31.5  | 32,2 <sup>(2)</sup> |      |
|                 |                                                  |                             | 64 MHz            | 54.9                    | 59.5                                | 60.6  | 61.9                | 25.3                     | 27.4                                | 28.1  | 28.8                |      |
|                 |                                                  |                             | 48 MHz            | 41.7                    | 45.3                                | 46.4  | 47.3                | 19.1                     | 20.7                                | 21.3  | 22.0                |      |
|                 |                                                  |                             | 32 MHz            | 28.2                    | 30.7                                | 31.7  | 32.4                | 12.8                     | 14.0                                | 14.6  | 15.1                |      |
|                 |                                                  |                             | 24 MHz            | 21.3                    | 23.2                                | 24.0  | 24.7                | 9.7                      | 10.6                                | 11.1  | 11.6                |      |
|                 |                                                  |                             | 8 MHz             | 7.0                     | 7.8                                 | 8.3   | 8.9                 | 3.1                      | 3.4                                 | 4.0   | 4.6                 |      |
|                 |                                                  |                             | 1 MHz             | 0.7                     | 0.9                                 | 1.3   | 2.1                 | 0.2                      | 0.4                                 | 0.8   | 1.5                 |      |
|                 |                                                  | Internal clock (HSI)        | 64 MHz            | 50.0                    | 54.2                                | 55.4  | 56.5                | 24.9                     | 27.0                                | 27.7  | 28.3                |      |
|                 |                                                  |                             | 48 MHz            | 38.0                    | 41.3                                | 42.3  | 43.2                | 18.7                     | 20.4                                | 21.0  | 21.6                |      |
|                 |                                                  |                             | 32 MHz            | 25.7                    | 27.9                                | 28.8  | 29.6                | 12.6                     | 13.7                                | 14.2  | 14.8                |      |
|                 |                                                  |                             | 24 MHz            | 19.4                    | 21.1                                | 22.0  | 22.6                | 6.3                      | 7.0                                 | 7.4   | 8.0                 |      |
|                 |                                                  |                             | 8 MHz             | 6.4                     | 7.2                                 | 7.7   | 8.2                 | 3.0                      | 3.3                                 | 3.9   | 4.4                 |      |

**Table 28. Typical and maximum current consumption from V<sub>DD</sub> supply at V<sub>DD</sub> = 1.8 V (continued)**

| Symbol          | Parameter                                                 | Conditions                  | f <sub>HCLK</sub> | All peripherals enabled |                                     |       |        | All peripherals disabled |                                     |       |        | Unit |
|-----------------|-----------------------------------------------------------|-----------------------------|-------------------|-------------------------|-------------------------------------|-------|--------|--------------------------|-------------------------------------|-------|--------|------|
|                 |                                                           |                             |                   | Typ                     | Max @ T <sub>A</sub> <sup>(1)</sup> |       |        | Typ                      | Max @ T <sub>A</sub> <sup>(1)</sup> |       |        |      |
|                 |                                                           |                             |                   |                         | 25 °C                               | 85 °C | 105 °C |                          | 25 °C                               | 85 °C | 105 °C |      |
| I <sub>DD</sub> | Supply current in Sleep mode, executing from Flash or RAM | External clock (HSE bypass) | 72 MHz            | 44.2                    | 48.2                                | 49.4  | 50.5   | 6.6                      | 7.2                                 | 7.8   | 8.4    | mA   |
|                 |                                                           |                             | 64 MHz            | 39.5                    | 43.1                                | 44.3  | 45.2   | 5.8                      | 6.5                                 | 7.0   | 7.6    |      |
|                 |                                                           |                             | 48 MHz            | 29.9                    | 32.7                                | 33.8  | 34.6   | 4.4                      | 4.9                                 | 5.5   | 6.0    |      |
|                 |                                                           |                             | 32 MHz            | 20.2                    | 22.1                                | 23.0  | 23.7   | 3.0                      | 3.3                                 | 3.9   | 4.5    |      |
|                 |                                                           |                             | 24 MHz            | 15.2                    | 16.7                                | 17.5  | 18.2   | 2.3                      | 2.5                                 | 3.0   | 3.7    |      |
|                 |                                                           |                             | 8 MHz             | 4.9                     | 5.6                                 | 6.1   | 6.7    | 0.6                      | 0.8                                 | 1.2   | 2.0    |      |
|                 |                                                           |                             | 1 MHz             | 0.5                     | 0.7                                 | 1.0   | 1.8    | 0.1                      | 0.0                                 | 0.4   | 1.2    |      |
|                 |                                                           | Internal clock (HSI)        | 64 MHz            | 34.5                    | 37.7                                | 38.9  | 39.7   | 5.5                      | 6.2                                 | 6.6   | 7.2    |      |
|                 |                                                           |                             | 48 MHz            | 26.1                    | 28.6                                | 29.7  | 30.4   | 4.1                      | 4.6                                 | 5.1   | 5.7    |      |
|                 |                                                           |                             | 32 MHz            | 17.6                    | 19.3                                | 20.2  | 20.8   | 2.7                      | 3.0                                 | 3.5   | 4.2    |      |
|                 |                                                           |                             | 24 MHz            | 13.3                    | 14.7                                | 15.4  | 16.0   | 1.3                      | 1.6                                 | 2.0   | 2.7    |      |
|                 |                                                           |                             | 8 MHz             | 4.4                     | 4.9                                 | 5.5   | 6.1    | 0.5                      | 0.7                                 | 1.0   | 1.9    |      |

1. Data based on characterization results, not tested in production unless otherwise specified.

2. Data based on characterization results and tested in production with code executing from RAM.

**Table 29. Typical and maximum current consumption from the V<sub>DDA</sub> supply**

| Symbol           | Parameter                                                          | Conditions<br>(1) | f <sub>HCLK</sub> | V <sub>DDA</sub> = 2.4 V |                                     |       |        | V <sub>DDA</sub> = 3.6 V |                                     |       |        | Unit |
|------------------|--------------------------------------------------------------------|-------------------|-------------------|--------------------------|-------------------------------------|-------|--------|--------------------------|-------------------------------------|-------|--------|------|
|                  |                                                                    |                   |                   | Typ                      | Max @ T <sub>A</sub> <sup>(2)</sup> |       |        | Typ                      | Max @ T <sub>A</sub> <sup>(2)</sup> |       |        |      |
|                  |                                                                    |                   |                   |                          | 25 °C                               | 85 °C | 105 °C |                          | 25 °C                               | 85 °C | 105 °C |      |
| I <sub>DDA</sub> | Supply current in Run/Sleep mode, code executing from Flash or RAM | HSE bypass        | 72 MHz            | 225                      | 276                                 | 289   | 297    | 245                      | 302                                 | 319   | 329    | μA   |
|                  |                                                                    |                   | 64 MHz            | 198                      | 249                                 | 261   | 268    | 216                      | 270                                 | 284   | 293    |      |
|                  |                                                                    |                   | 48 MHz            | 149                      | 195                                 | 204   | 211    | 159                      | 209                                 | 222   | 230    |      |
|                  |                                                                    |                   | 32 MHz            | 102                      | 145                                 | 152   | 157    | 110                      | 154                                 | 162   | 169    |      |
|                  |                                                                    |                   | 24 MHz            | 80                       | 119                                 | 124   | 128    | 86                       | 126                                 | 131   | 135    |      |
|                  |                                                                    |                   | 8 MHz             | 2                        | 3                                   | 4     | 6      | 3                        | 4                                   | 5     | 9      |      |
|                  |                                                                    |                   | 1 MHz             | 2                        | 3                                   | 5     | 7      | 3                        | 4                                   | 6     | 9      |      |
|                  |                                                                    | HSI clock         | 64 MHz            | 270                      | 323                                 | 337   | 344    | 299                      | 354                                 | 371   | 381    |      |
|                  |                                                                    |                   | 48 MHz            | 220                      | 269                                 | 280   | 286    | 244                      | 293                                 | 309   | 318    |      |
|                  |                                                                    |                   | 32 MHz            | 173                      | 218                                 | 228   | 233    | 193                      | 239                                 | 251   | 257    |      |
|                  |                                                                    |                   | 24 MHz            | 151                      | 194                                 | 200   | 204    | 169                      | 211                                 | 219   | 225    |      |
|                  |                                                                    |                   | 8 MHz             | 73                       | 97                                  | 99    | 103    | 88                       | 105                                 | 110   | 116    |      |

1. Current consumption from the V<sub>DDA</sub> supply is independent of whether the peripherals are on or off. Furthermore when the PLL is off, I<sub>DDA</sub> is independent from the frequency.

2. Data based on characterization results, not tested in production.

**Table 30. Typical and maximum  $V_{DD}$  consumption in Stop mode**

| Symbol   | Parameter                   | Conditions          | Typ@ $V_{DD}$ ( $V_{DD}=V_{DDA}=1.8V$ ) | Max <sup>(1)</sup>               |                                  |                                   | Unit          |
|----------|-----------------------------|---------------------|-----------------------------------------|----------------------------------|----------------------------------|-----------------------------------|---------------|
|          |                             |                     |                                         | $T_A=25\text{ }^{\circ}\text{C}$ | $T_A=85\text{ }^{\circ}\text{C}$ | $T_A=105\text{ }^{\circ}\text{C}$ |               |
| $I_{DD}$ | Supply current in Stop mode | All oscillators OFF | 6.6                                     | 31.1 <sup>(2)</sup>              | 560.5                            | 1225.8 <sup>(2)</sup>             | $\mu\text{A}$ |

1. Data based on characterization results, not tested in production unless otherwise specified.

2. Data based on characterization results and tested in production.

**Table 31. Typical and maximum  $V_{DDA}$  consumption in Stop mode**

| Symbol    | Parameter                   | Conditions          | Typ@ $V_{DDA}$ ( $V_{DD} = 1.8V$ ) |       |       |       |       |       |       | Max <sup>(1)</sup>               |                                  |                                   | Unit          |
|-----------|-----------------------------|---------------------|------------------------------------|-------|-------|-------|-------|-------|-------|----------------------------------|----------------------------------|-----------------------------------|---------------|
|           |                             |                     | 1.8 V                              | 2.0 V | 2.4 V | 2.7 V | 3.0 V | 3.3 V | 3.6 V | $T_A=25\text{ }^{\circ}\text{C}$ | $T_A=85\text{ }^{\circ}\text{C}$ | $T_A=105\text{ }^{\circ}\text{C}$ |               |
| $I_{DDA}$ | Supply current in Stop mode | All oscillators OFF | 0.76                               | 0.78  | 0.80  | 0.83  | 0.87  | 0.94  | 1.01  | 3.2                              | 5.3                              | 7.9                               | $\mu\text{A}$ |

1. Data based on characterization results and tested in production.

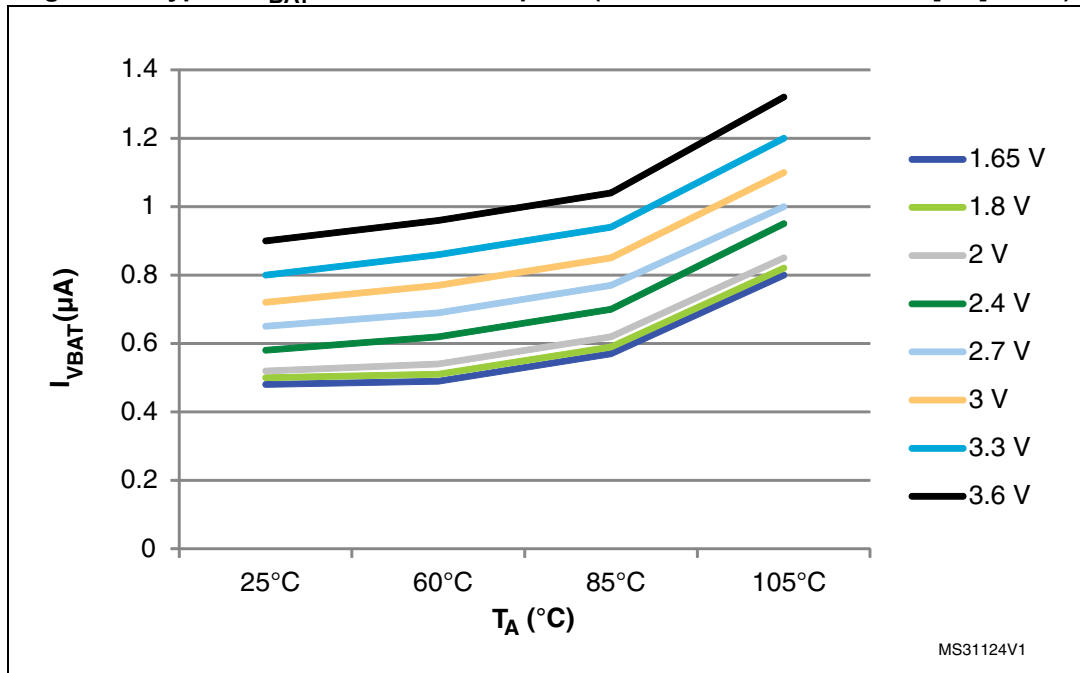
**Note:** The total current consumption is the sum of  $I_{DD}$  and  $I_{DDA}$

**Table 32. Typical and maximum current consumption from  $V_{BAT}$  supply**

| Symbol         | Parameter                    | Conditions <sup>(1)</sup>                                               | Typ @ $V_{BAT}$ |      |      |      |      |      |      |      | Max<br>@ $V_{BAT} = 3.6\text{ V}^{(2)}$ |                                  |                                   | Unit          |
|----------------|------------------------------|-------------------------------------------------------------------------|-----------------|------|------|------|------|------|------|------|-----------------------------------------|----------------------------------|-----------------------------------|---------------|
|                |                              |                                                                         | 1.65V           | 1.8V | 2V   | 2.4V | 2.7V | 3V   | 3.3V | 3.6V | $T_A=25\text{ }^{\circ}\text{C}$        | $T_A=85\text{ }^{\circ}\text{C}$ | $T_A=105\text{ }^{\circ}\text{C}$ |               |
| $I_{DD\_VBAT}$ | Backup domain supply current | LSE & RTC ON; "Xtal mode" lower driving capability; LSEDRV[1:0] = '00'  | 0.48            | 0.50 | 0.52 | 0.58 | 0.65 | 0.72 | 0.80 | 0.90 | 1.1                                     | 1.5                              | 2.0                               | $\mu\text{A}$ |
|                |                              | LSE & RTC ON; "Xtal mode" higher driving capability; LSEDRV[1:0] = '11' | 0.83            | 0.86 | 0.90 | 0.98 | 1.03 | 1.10 | 1.20 | 1.30 | 1.5                                     | 2.2                              | 2.9                               |               |

1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a CL of 6 pF for typical values.

2. Data based on characterization results, not tested in production.

Figure 12. Typical  $V_{BAT}$  current consumption (LSE and RTC ON/LSEDRV[1:0] = '00')

### Typical current consumption

The MCU is placed under the following conditions:

- $V_{DD} = 1.8$  V,  $V_{DDA} = 3.3$  V
- All I/O pins available on each package are in analog input configuration
- The Flash access time is adjusted to  $f_{HCLK}$  frequency (0 wait states from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states from 48 MHz to 72 MHz), and Flash prefetch is ON
- When the peripherals are enabled,  $f_{APB1} = f_{AHB}/2$ ,  $f_{APB2} = f_{AHB}$
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8, 16 and 64 is used for the frequencies 4 MHz, 2 MHz, 1 MHz, 500 kHz and 125 kHz respectively.

Table 33. Typical current consumption in Run mode, code with data processing running from Flash

| Symbol                              | Parameter                                               | Conditions                                                      | f <sub>HCLK</sub> | Typ                 |                      | Unit |
|-------------------------------------|---------------------------------------------------------|-----------------------------------------------------------------|-------------------|---------------------|----------------------|------|
|                                     |                                                         |                                                                 |                   | Peripherals enabled | Peripherals disabled |      |
| I <sub>DD</sub>                     | Supply current in Run mode from V <sub>DD</sub> supply  | Running from HSE crystal clock 8 MHz, code executing from Flash | 72 MHz            | 58.6                | 26.5                 | mA   |
|                                     |                                                         |                                                                 | 64 MHz            | 52.6                | 23.7                 |      |
|                                     |                                                         |                                                                 | 48 MHz            | 40.6                | 18.5                 |      |
|                                     |                                                         |                                                                 | 32 MHz            | 27.6                | 12.7                 |      |
|                                     |                                                         |                                                                 | 24 MHz            | 21.1                | 9.9                  |      |
|                                     |                                                         |                                                                 | 16 MHz            | 14.3                | 6.8                  |      |
|                                     |                                                         |                                                                 | 8 MHz             | 7.2                 | 3.5                  |      |
|                                     |                                                         |                                                                 | 4 MHz             | 4.1                 | 2.1                  |      |
|                                     |                                                         |                                                                 | 2 MHz             | 2.3                 | 1.3                  |      |
|                                     |                                                         |                                                                 | 1 MHz             | 1.5                 | 0.9                  |      |
|                                     |                                                         |                                                                 | 500 kHz           | 1.0                 | 0.7                  |      |
|                                     |                                                         |                                                                 | 125 kHz           | 0.7                 | 0.5                  |      |
| I <sub>DDA</sub> <sup>(1) (2)</sup> | Supply current in Run mode from V <sub>DDA</sub> supply | Running from HSE crystal clock 8 MHz, code executing from Flash | 72 MHz            | 239.0               |                      | μA   |
|                                     |                                                         |                                                                 | 64 MHz            | 210.3               |                      |      |
|                                     |                                                         |                                                                 | 48 MHz            | 157.0               |                      |      |
|                                     |                                                         |                                                                 | 32 MHz            | 108.1               |                      |      |
|                                     |                                                         |                                                                 | 24 MHz            | 84.4                |                      |      |
|                                     |                                                         |                                                                 | 16 MHz            | 60.8                |                      |      |
|                                     |                                                         |                                                                 | 8 MHz             | 1.0                 |                      |      |
|                                     |                                                         |                                                                 | 4 MHz             | 1.0                 |                      |      |
|                                     |                                                         |                                                                 | 2 MHz             | 1.0                 |                      |      |
|                                     |                                                         |                                                                 | 1 MHz             | 1.0                 |                      |      |
|                                     |                                                         |                                                                 | 500 kHz           | 1.0                 |                      |      |
|                                     |                                                         |                                                                 | 125 kHz           | 1.0                 |                      |      |

1.  $V_{DDA}$  monitoring is ON.

2. When peripherals are enabled, the power consumption of the analog part of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.

Table 34. Typical current consumption in Sleep mode, code running from Flash or RAM

| Symbol                              | Parameter                                                 | Conditions                                                             | f <sub>HCLK</sub> | Typ                 |                      | Unit |
|-------------------------------------|-----------------------------------------------------------|------------------------------------------------------------------------|-------------------|---------------------|----------------------|------|
|                                     |                                                           |                                                                        |                   | Peripherals enabled | Peripherals disabled |      |
| I <sub>DD</sub>                     | Supply current in Sleep mode from V <sub>DD</sub> supply  | Running from HSE crystal clock 8 MHz, code executing from Flash or RAM | 72 MHz            | 42.5                | 6.5                  | mA   |
|                                     |                                                           |                                                                        | 64 MHz            | 38.0                | 5.8                  |      |
|                                     |                                                           |                                                                        | 48 MHz            | 28.8                | 4.4                  |      |
|                                     |                                                           |                                                                        | 32 MHz            | 19.4                | 3.0                  |      |
|                                     |                                                           |                                                                        | 24 MHz            | 14.6                | 2.3                  |      |
|                                     |                                                           |                                                                        | 16 MHz            | 9.8                 | 1.6                  |      |
|                                     |                                                           |                                                                        | 8 MHz             | 4.8                 | 0.8                  |      |
|                                     |                                                           |                                                                        | 4 MHz             | 2.9                 | 0.6                  |      |
|                                     |                                                           |                                                                        | 2 MHz             | 1.7                 | 0.5                  |      |
|                                     |                                                           |                                                                        | 1 MHz             | 1.2                 | 0.5                  |      |
|                                     |                                                           |                                                                        | 500 kHz           | 0.9                 | 0.5                  |      |
|                                     |                                                           |                                                                        | 125 kHz           | 0.7                 | 0.5                  |      |
| I <sub>DDA</sub> <sup>(1) (2)</sup> | Supply current in Sleep mode from V <sub>DDA</sub> supply | Running from HSE crystal clock 8 MHz, code executing from Flash or RAM | 72 MHz            | 239.0               |                      | μA   |
|                                     |                                                           |                                                                        | 64 MHz            | 210.3               |                      |      |
|                                     |                                                           |                                                                        | 48 MHz            | 157.0               |                      |      |
|                                     |                                                           |                                                                        | 32 MHz            | 108.1               |                      |      |
|                                     |                                                           |                                                                        | 24 MHz            | 84.4                |                      |      |
|                                     |                                                           |                                                                        | 16 MHz            | 60.8                |                      |      |
|                                     |                                                           |                                                                        | 8 MHz             | 1.0                 |                      |      |
|                                     |                                                           |                                                                        | 4 MHz             | 1.0                 |                      |      |
|                                     |                                                           |                                                                        | 2 MHz             | 1.0                 |                      |      |
|                                     |                                                           |                                                                        | 1 MHz             | 1.0                 |                      |      |
|                                     |                                                           |                                                                        | 500 kHz           | 1.0                 |                      |      |
|                                     |                                                           |                                                                        | 125 kHz           | 1.0                 |                      |      |

1.  $V_{DDA}$  monitoring is ON

2. When peripherals are enabled, the power consumption of the analog part of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.

## I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

### I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in [Table 52: I/O static characteristics](#).

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

**Caution:** Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

### I/O dynamic current consumption

In addition to the internal peripheral current consumption (see [Table 36: Peripheral current consumption](#)), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

$I_{SW}$  is the current sunk by a switching I/O to charge/discharge the capacitive load

$V_{DD}$  is the MCU supply voltage

$f_{SW}$  is the I/O switching frequency

$C$  is the total capacitance seen by the I/O pin:  $C = C_{INT} + C_{EXT} + C_S$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 35. Switching output I/O current consumption

| Symbol          | Parameter               | Conditions <sup>(1)</sup>                                                            | I/O toggling frequency (f <sub>SW</sub> ) | Typ  | Unit |
|-----------------|-------------------------|--------------------------------------------------------------------------------------|-------------------------------------------|------|------|
| I <sub>SW</sub> | I/O current consumption | $V_{DD} = 1.8\text{ V}$<br>$C_{ext} = 0\text{ pF}$<br>$C = C_{INT} + C_{EXT} + C_S$  | 2 MHz                                     | 0.10 | mA   |
|                 |                         |                                                                                      | 4 MHz                                     | 0.17 |      |
|                 |                         |                                                                                      | 8 MHz                                     | 0.40 |      |
|                 |                         |                                                                                      | 18 MHz                                    | 0.78 |      |
|                 |                         |                                                                                      | 36 MHz                                    | 1.51 |      |
|                 |                         |                                                                                      | 48 MHz                                    | 2.06 |      |
|                 |                         | $V_{DD} = 1.8\text{ V}$<br>$C_{ext} = 10\text{ pF}$<br>$C = C_{INT} + C_{EXT} + C_S$ | 2 MHz                                     | 0.14 |      |
|                 |                         |                                                                                      | 4 MHz                                     | 0.25 |      |
|                 |                         |                                                                                      | 8 MHz                                     | 0.57 |      |
|                 |                         |                                                                                      | 18 MHz                                    | 1.16 |      |
|                 |                         |                                                                                      | 36 MHz                                    | 2.45 |      |
|                 |                         |                                                                                      | 48 MHz                                    | 3.03 |      |
|                 |                         | $V_{DD} = 1.8\text{ V}$<br>$C_{ext} = 22\text{ pF}$<br>$C = C_{INT} + C_{EXT} + C_S$ | 2 MHz                                     | 0.19 |      |
|                 |                         |                                                                                      | 4 MHz                                     | 0.36 |      |
|                 |                         |                                                                                      | 8 MHz                                     | 0.75 |      |
|                 |                         |                                                                                      | 18 MHz                                    | 1.59 |      |
|                 |                         |                                                                                      | 36 MHz                                    | 3.25 |      |
|                 |                         | $V_{DD} = 1.8\text{ V}$<br>$C_{ext} = 33\text{ pF}$<br>$C = C_{INT} + C_{EXT} + C_S$ | 2 MHz                                     | 0.23 |      |
|                 |                         |                                                                                      | 4 MHz                                     | 0.45 |      |
|                 |                         |                                                                                      | 8 MHz                                     | 0.94 |      |
|                 |                         |                                                                                      | 18 MHz                                    | 1.97 |      |
|                 |                         |                                                                                      | 36 MHz                                    | 3.62 |      |
|                 |                         | $V_{DD} = 1.8\text{ V}$<br>$C_{ext} = 47\text{ pF}$<br>$C = C_{INT} + C_{EXT} + C_S$ | 2 MHz                                     | 0.28 |      |
|                 |                         |                                                                                      | 4 MHz                                     | 0.55 |      |
|                 |                         |                                                                                      | 8 MHz                                     | 1.15 |      |
|                 |                         |                                                                                      | 18 MHz                                    | 2.42 |      |

1. CS = 5 pF (estimated value).

**On-chip peripheral current consumption**

The MCU is placed under the following conditions:

- all I/O pins are in analog input configuration
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature at 25°C and  $V_{DD} = 1.8\text{ V}$ ,  $V_{DDA} = 3.3\text{ V}$ .

**Table 36. Peripheral current consumption**

| Peripheral                 | Typical consumption <sup>(1)</sup> | Unit              |
|----------------------------|------------------------------------|-------------------|
|                            | $I_{DD}$                           |                   |
| BusMatrix <sup>(2)</sup>   | 12.6                               | $\mu\text{A/MHz}$ |
| DMA1                       | 7.6                                |                   |
| DMA2                       | 6.1                                |                   |
| CRC                        | 2.1                                |                   |
| GPIOA                      | 10.0                               |                   |
| GPIOB                      | 10.3                               |                   |
| GPIOC                      | 2.2                                |                   |
| GIOD                       | 8.8                                |                   |
| GPIOE                      | 3.3                                |                   |
| GPIOF                      | 3.0                                |                   |
| TSC                        | 5.5                                |                   |
| ADC1&2                     | 17.3                               |                   |
| ADC3&4                     | 18.8                               |                   |
| APB2-Bridge <sup>(3)</sup> | 3.6                                |                   |
| SYSCFG                     | 7.3                                |                   |
| TIM1                       | 40.0                               |                   |
| SPI1                       | 8.8                                |                   |
| TIM8                       | 36.4                               |                   |
| USART1                     | 23.3                               |                   |
| TIM15                      | 17.1                               |                   |
| TIM16                      | 10.1                               |                   |
| TIM17                      | 11.0                               |                   |
| APB1-Bridge <sup>(3)</sup> | 6.1                                |                   |
| TIM2                       | 49.1                               |                   |
| TIM3                       | 38.8                               |                   |
| TIM4                       | 38.3                               |                   |

Table 36. Peripheral current consumption (continued)

| Peripheral | Typical consumption <sup>(1)</sup> | Unit   |
|------------|------------------------------------|--------|
|            | I <sub>DD</sub>                    |        |
| TIM6       | 9.7                                | μA/MHz |
| TIM7       | 12.1                               |        |
| WWDG       | 6.4                                |        |
| SPI2       | 40.4                               |        |
| SPI3       | 40.0                               |        |
| USART2     | 41.9                               |        |
| USART3     | 40.2                               |        |
| UART4      | 36.5                               |        |
| UART5      | 30.8                               |        |
| I2C1       | 10.5                               |        |
| I2C2       | 10.4                               |        |
| CAN        | 33.4                               |        |
| PWR        | 5.7                                |        |
| DAC        | 15.4                               |        |

1. The power consumption of the analog part (I<sub>DDA</sub>) of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.
2. BusMatrix is automatically active when at least one master is ON (CPU, DMA1 or DMA2).
3. The APBx bridge is automatically active when at least one peripheral is ON on the same bus.

### 6.3.5 Wakeup time from low-power mode

The wakeup times given in [Table 37](#) are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep mode: the wakeup event is WFE.
- WKUP1 (PA0) pin is used to wakeup from Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 24](#).

**Table 37. Low-power mode wakeup timings**

| Symbol        | Parameter                   | Typ @ $V_{DD} = 1.8\text{ V}$ , $V_{DDA} = 3.3\text{ V}$ | Max | Unit             |
|---------------|-----------------------------|----------------------------------------------------------|-----|------------------|
| $t_{WUSTOP}$  | Wakeup from Stop mode       | 3.8                                                      | 5.3 | $\mu\text{s}$    |
| $t_{WUSLEEP}$ | Wakeup from Sleep mode      | 6                                                        | -   | CPU clock cycles |
| $t_{WUPOR}$   | Wakeup from Power off state | 69.2                                                     | 100 | $\mu\text{s}$    |

### 6.3.6 External clock source characteristics

#### High-speed external user clock generated from an external source

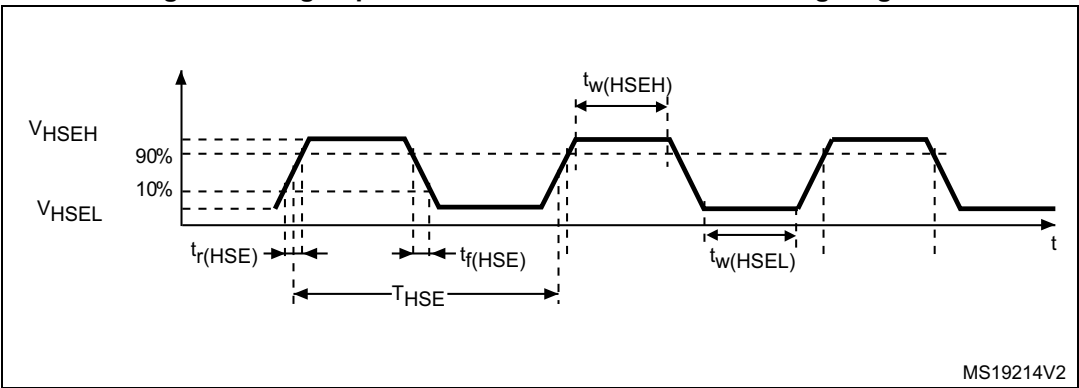
In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO. The external clock signal has to respect the I/O characteristics in [Section 6.3.13](#). However, the recommended clock input waveform is shown in [Figure 13](#).

**Table 38. High-speed external user clock characteristics**

| Symbol                         | Parameter                                           | Conditions | Min         | Typ | Max         | Unit |
|--------------------------------|-----------------------------------------------------|------------|-------------|-----|-------------|------|
| $f_{HSE\_ext}$                 | User external clock source frequency <sup>(1)</sup> | -          | 1           | 8   | 32          | MHz  |
| $V_{HSEH}$                     | OSC_IN input pin high level voltage                 |            | $0.7V_{DD}$ | -   | $V_{DD}$    | V    |
| $V_{HSEL}$                     | OSC_IN input pin low level voltage                  |            | $V_{SS}$    | -   | $0.3V_{DD}$ |      |
| $t_{w(HSEH)}$<br>$t_{w(HSEL)}$ | OSC_IN high or low time <sup>(1)</sup>              |            | 15          | -   | -           | ns   |
| $t_r(HSE)$<br>$t_f(HSE)$       | OSC_IN rise or fall time <sup>(1)</sup>             |            | -           | -   | 20          |      |

1. Guaranteed by design, not tested in production.

**Figure 13. High-speed external clock source AC timing diagram**



### Low-speed external user clock generated from an external source

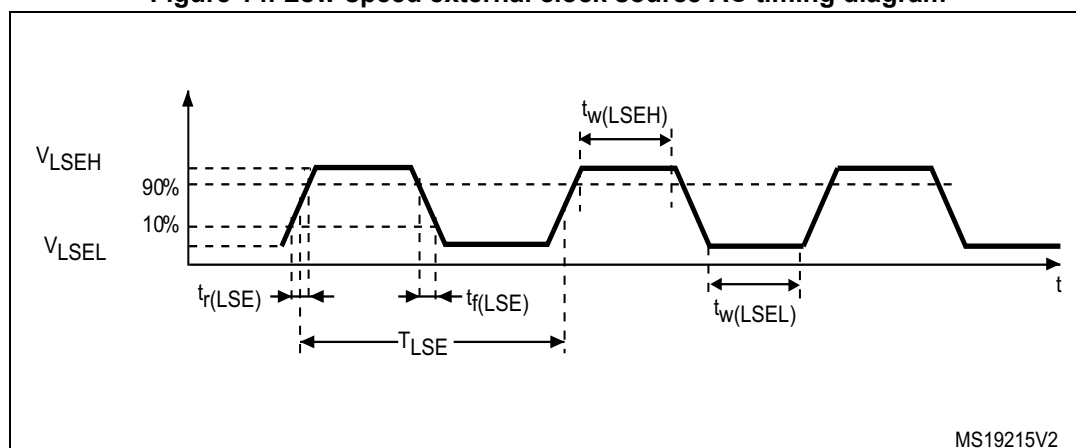
In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO. The external clock signal has to respect the I/O characteristics in [Section 6.3.13](#). However, the recommended clock input waveform is shown in [Figure 14](#)

**Table 39. Low-speed external user clock characteristics**

| Symbol                         | Parameter                                           | Conditions | Min         | Typ    | Max         | Unit |
|--------------------------------|-----------------------------------------------------|------------|-------------|--------|-------------|------|
| $f_{LSE\_ext}$                 | User External clock source frequency <sup>(1)</sup> | -          | -           | 32.768 | 1000        | kHz  |
| $V_{LSEH}$                     | OSC32_IN input pin high level voltage               |            | $0.7V_{DD}$ | -      | $V_{DD}$    | V    |
| $V_{LSEL}$                     | OSC32_IN input pin low level voltage                |            | $V_{SS}$    | -      | $0.3V_{DD}$ |      |
| $t_{w(LSEH)}$<br>$t_{w(LSEL)}$ | OSC32_IN high or low time <sup>(1)</sup>            |            | 450         | -      | -           | ns   |
| $t_{r(LSE)}$<br>$t_{f(LSE)}$   | OSC32_IN rise or fall time <sup>(1)</sup>           |            | -           | -      | 50          |      |

1. Guaranteed by design, not tested in production.

**Figure 14. Low-speed external clock source AC timing diagram**



### High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in [Table 40](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 40. HSE oscillator characteristics**

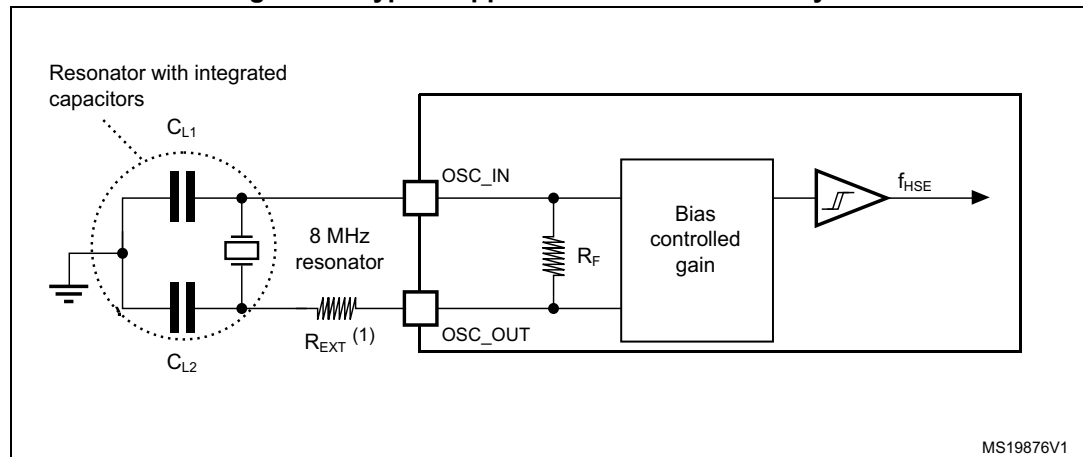
| Symbol              | Parameter                   | Conditions <sup>(1)</sup>                                                   | Min <sup>(2)</sup> | Typ | Max <sup>(2)</sup> | Unit       |
|---------------------|-----------------------------|-----------------------------------------------------------------------------|--------------------|-----|--------------------|------------|
| $f_{OSC\_IN}$       | Oscillator frequency        |                                                                             | 4                  | 8   | 32                 | MHz        |
| $R_F$               | Feedback resistor           |                                                                             | -                  | 200 |                    | k $\Omega$ |
| $I_{DD}$            | HSE current consumption     | During startup <sup>(3)</sup>                                               | -                  | -   | 8.5                | mA         |
|                     |                             | $V_{DD}=3.3\text{ V}$ , $R_m=30\Omega$ ,<br>$CL=10\text{ pF}@8\text{ MHz}$  | -                  | 0.4 | -                  |            |
|                     |                             | $V_{DD}=3.3\text{ V}$ , $R_m=45\Omega$ ,<br>$CL=10\text{ pF}@8\text{ MHz}$  | -                  | 0.5 | -                  |            |
|                     |                             | $V_{DD}=3.3\text{ V}$ , $R_m=30\Omega$ ,<br>$CL=5\text{ pF}@32\text{ MHz}$  | -                  | 0.8 | -                  |            |
|                     |                             | $V_{DD}=3.3\text{ V}$ , $R_m=30\Omega$ ,<br>$CL=10\text{ pF}@32\text{ MHz}$ | -                  | 1   | -                  |            |
|                     |                             | $V_{DD}=3.3\text{ V}$ , $R_m=30\Omega$ ,<br>$CL=20\text{ pF}@32\text{ MHz}$ | -                  | 1.5 | -                  |            |
| $g_m$               | Oscillator transconductance | Startup                                                                     | 10                 | -   | -                  | mA/V       |
| $t_{SU(HSE)}^{(4)}$ | Startup time                | $V_{DD}$ is stabilized                                                      | -                  | 2   | -                  | ms         |

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design, not tested in production.
3. This consumption level occurs during the first 2/3 of the  $t_{SU(HSE)}$  startup time.
4.  $t_{SU(HSE)}$  is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For  $C_{L1}$  and  $C_{L2}$ , it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see [Figure 15](#)).  $C_{L1}$  and  $C_{L2}$  are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of  $C_{L1}$  and  $C_{L2}$ . PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing  $C_{L1}$  and  $C_{L2}$ .

**Note:** For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website [www.st.com](http://www.st.com).

**Figure 15. Typical application with an 8 MHz crystal**



1.  $R_{EXT}$  value depends on the crystal characteristics.

### Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in [Table 41](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

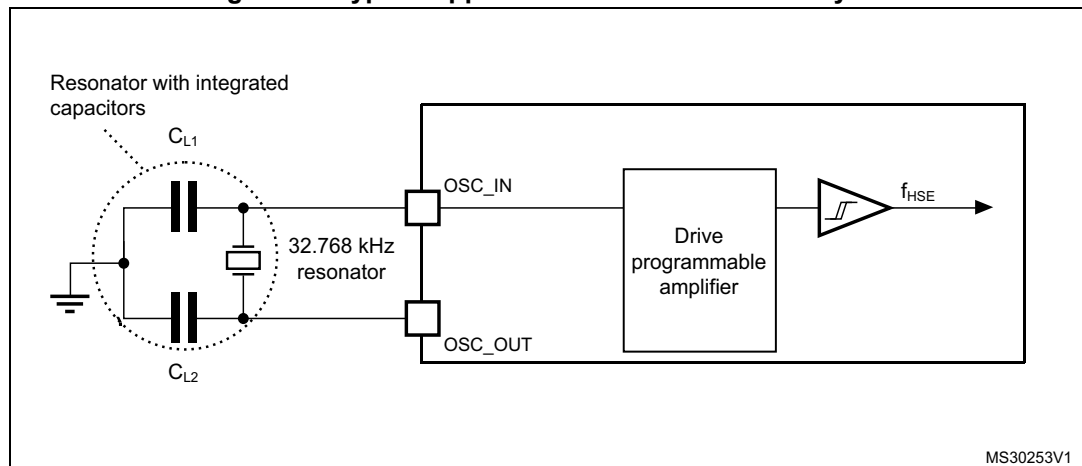
**Table 41. LSE oscillator characteristics ( $f_{LSE} = 32.768$  kHz)**

| Symbol              | Parameter                   | Conditions <sup>(1)</sup>                        | Min <sup>(2)</sup> | Typ | Max <sup>(2)</sup> | Unit      |
|---------------------|-----------------------------|--------------------------------------------------|--------------------|-----|--------------------|-----------|
| $I_{DD}$            | LSE current consumption     | LSEDRV[1:0]=00<br>lower driving capability       | -                  | 0.5 | 0.9                | $\mu A$   |
|                     |                             | LSEDRV[1:0]=01<br>medium low driving capability  | -                  | -   | 1                  |           |
|                     |                             | LSEDRV[1:0]=10<br>medium high driving capability | -                  | -   | 1.3                |           |
|                     |                             | LSEDRV[1:0]=11<br>higher driving capability      | -                  | -   | 1.6                |           |
| $g_m$               | Oscillator transconductance | LSEDRV[1:0]=00<br>lower driving capability       | 5                  | -   | -                  | $\mu A/V$ |
|                     |                             | LSEDRV[1:0]=01<br>medium low driving capability  | 8                  | -   | -                  |           |
|                     |                             | LSEDRV[1:0]=10<br>medium high driving capability | 15                 | -   | -                  |           |
|                     |                             | LSEDRV[1:0]=11<br>higher driving capability      | 25                 | -   | -                  |           |
| $t_{SU(LSE)}^{(3)}$ | Startup time                | $V_{DD}$ is stabilized                           | -                  | 2   | -                  | s         |

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 "Oscillator design guide for ST microcontrollers".
2. Guaranteed by design, not tested in production.
3.  $t_{SU(LSE)}$  is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer.

**Note:** For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website [www.st.com](http://www.st.com).

Figure 16. Typical application with a 32.768 kHz crystal



**Note:** An external resistor is not required between  $OSC32\_IN$  and  $OSC32\_OUT$  and it is forbidden to add one.

### 6.3.7 Internal clock source characteristics

The parameters given in [Table 42](#) are derived from tests performed under ambient temperature and supply voltage conditions summarized in [Table 24](#).

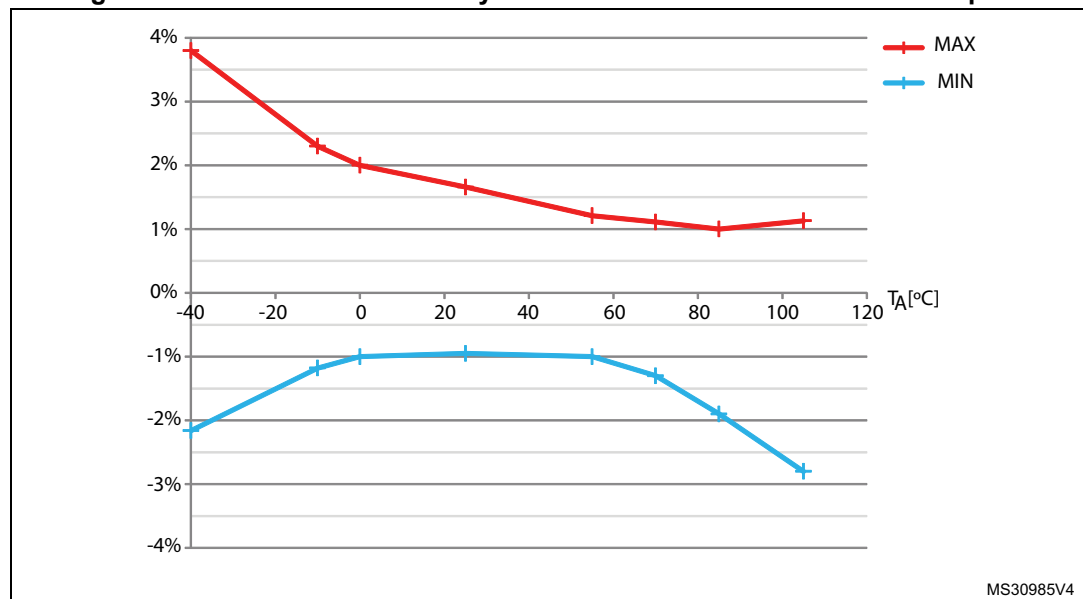
#### High-speed internal (HSI) RC oscillator

Table 42. HSI oscillator characteristics<sup>(1)</sup>

| Symbol                | Parameter                        | Conditions                              | Min                 | Typ | Max                | Unit          |
|-----------------------|----------------------------------|-----------------------------------------|---------------------|-----|--------------------|---------------|
| $f_{\text{HSI}}$      | Frequency                        | -                                       | -                   | 8   | -                  | MHz           |
| TRIM                  | HSI user trimming step           | -                                       | -                   | -   | 1 <sup>(2)</sup>   | %             |
| DuCy <sub>(HSI)</sub> | Duty cycle                       | -                                       | 45 <sup>(2)</sup>   | -   | 55 <sup>(2)</sup>  | %             |
| ACC <sub>HSI</sub>    | Accuracy of the HSI oscillator   | $T_A = -40$ to $105^\circ\text{C}$      | -2.8 <sup>(3)</sup> | -   | 3.8 <sup>(3)</sup> | %             |
|                       |                                  | $T_A = -10$ to $85^\circ\text{C}$       | -1.9 <sup>(3)</sup> | -   | 2.3 <sup>(3)</sup> |               |
|                       |                                  | $T_A = 0$ to $85^\circ\text{C}$         | -1.9 <sup>(3)</sup> | -   | 2 <sup>(3)</sup>   |               |
|                       |                                  | $T_A = 0$ to $70^\circ\text{C}$         | -1.3 <sup>(3)</sup> | -   | 2 <sup>(3)</sup>   |               |
|                       |                                  | $T_A = 0$ to $55^\circ\text{C}$         | -1 <sup>(3)</sup>   | -   | 2 <sup>(3)</sup>   |               |
|                       |                                  | $T_A = 25^\circ\text{C}$ <sup>(4)</sup> | -1                  | -   | 1                  |               |
| $t_{\text{su(HSI)}}$  | HSI oscillator startup time      | -                                       | 1 <sup>(2)</sup>    | -   | 2 <sup>(2)</sup>   | $\mu\text{s}$ |
| $I_{\text{DDA(HSI)}}$ | HSI oscillator power consumption | -                                       | -                   | 80  | 100 <sup>(2)</sup> | $\mu\text{A}$ |

1.  $V_{\text{DDA}} = 3.3\text{ V}$ ,  $T_A = -40$  to  $105^\circ\text{C}$  unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.
4. Factory calibrated, parts not soldered.

Figure 17. HSI oscillator accuracy characterization results for soldered parts



### Low-speed internal (LSI) RC oscillator

**Table 43. LSI oscillator characteristics<sup>(1)</sup>**

| Symbol              | Parameter                        | Min | Typ  | Max | Unit    |
|---------------------|----------------------------------|-----|------|-----|---------|
| $f_{LSI}$           | Frequency                        | 30  | 40   | 50  | kHz     |
| $t_{su(LSI)}^{(2)}$ | LSI oscillator startup time      | -   | -    | 85  | $\mu$ s |
| $I_{DD(LSI)}^{(2)}$ | LSI oscillator power consumption | -   | 0.75 | 1.2 | $\mu$ A |

1.  $V_{DDA} = 3.3$  V,  $T_A = -40$  to  $105$  °C unless otherwise specified.

2. Guaranteed by design, not tested in production.

### 6.3.8 PLL characteristics

The parameters given in [Table 44](#) are derived from tests performed under ambient temperature and supply voltage conditions summarized in [Table 24](#).

**Table 44. PLL characteristics**

| Symbol         | Parameter                      | Value             |     |                    | Unit    |
|----------------|--------------------------------|-------------------|-----|--------------------|---------|
|                |                                | Min               | Typ | Max                |         |
| $f_{PLL\_IN}$  | PLL input clock <sup>(1)</sup> | 1 <sup>(2)</sup>  | -   | 24 <sup>(2)</sup>  | MHz     |
|                | PLL input clock duty cycle     | 40 <sup>(2)</sup> | -   | 60 <sup>(2)</sup>  | %       |
| $f_{PLL\_OUT}$ | PLL multiplier output clock    | 16 <sup>(2)</sup> | -   | 72                 | MHz     |
| $t_{LOCK}$     | PLL lock time                  | -                 | -   | 200 <sup>(2)</sup> | $\mu$ s |
| Jitter         | Cycle-to-cycle jitter          | -                 | -   | 300 <sup>(2)</sup> | ps      |

1. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by  $f_{PLL\_OUT}$ .

2. Guaranteed by design, not tested in production.

### 6.3.9 Memory characteristics

#### Flash memory

The characteristics are given at  $T_A = -40$  to  $+105\text{ }^{\circ}\text{C}$  unless otherwise specified.

**Table 45. Flash memory characteristics**

| Symbol             | Parameter               | Conditions                                    | Min | Typ  | Max <sup>(1)</sup> | Unit          |
|--------------------|-------------------------|-----------------------------------------------|-----|------|--------------------|---------------|
| $t_{\text{prog}}$  | 16-bit programming time | $T_A = -40$ to $+105\text{ }^{\circ}\text{C}$ | 40  | 53.5 | 60                 | $\mu\text{s}$ |
| $t_{\text{ERASE}}$ | Page (2 KB) erase time  | $T_A = -40$ to $+105\text{ }^{\circ}\text{C}$ | 20  | -    | 40                 | ms            |
| $t_{\text{ME}}$    | Mass erase time         | $T_A = -40$ to $+105\text{ }^{\circ}\text{C}$ | 20  | -    | 40                 | ms            |
| $I_{\text{DD}}$    | Supply current          | Write mode                                    | -   | -    | 10                 | mA            |
|                    |                         | Erase mode                                    | -   | -    | 12                 | mA            |

1. Guaranteed by design, not tested in production.

**Table 46. Flash memory endurance and data retention**

| Symbol           | Parameter      | Conditions                                                                                                                            | Value              | Unit    |
|------------------|----------------|---------------------------------------------------------------------------------------------------------------------------------------|--------------------|---------|
|                  |                |                                                                                                                                       | Min <sup>(1)</sup> |         |
| $N_{\text{END}}$ | Endurance      | $T_A = -40$ to $+85\text{ }^{\circ}\text{C}$ (6 suffix versions)<br>$T_A = -40$ to $+105\text{ }^{\circ}\text{C}$ (7 suffix versions) | 10                 | kcycles |
| $t_{\text{RET}}$ | Data retention | 1 kcycle <sup>(2)</sup> at $T_A = 85\text{ }^{\circ}\text{C}$                                                                         | 30                 | Years   |
|                  |                | 1 kcycle <sup>(2)</sup> at $T_A = 105\text{ }^{\circ}\text{C}$                                                                        | 10                 |         |
|                  |                | 10 kcycles <sup>(2)</sup> at $T_A = 55\text{ }^{\circ}\text{C}$                                                                       | 20                 |         |

1. Data based on characterization results, not tested in production.

2. Cycling performed over the whole temperature range.

### 6.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

#### Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to  $V_{DD}$  and  $V_{SS}$  through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in [Table 47](#). They are based on the EMS levels and classes defined in application note AN1709.

**Table 47. EMS characteristics**

| Symbol     | Parameter                                                                                                                         | Conditions                                                                                                                | Level/Class |
|------------|-----------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------|-------------|
| $V_{FESD}$ | Voltage limits to be applied on any I/O pin to induce a functional disturbance                                                    | $V_{DD} = 1.8\text{ V}$ , LQFP100, $T_A = +25^\circ\text{C}$ ,<br>$f_{HCLK} = 72\text{ MHz}$<br>conforms to IEC 61000-4-2 | 2B          |
| $V_{EFTB}$ | Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance | $V_{DD} = 1.8\text{ V}$ , LQFP100, $T_A = +25^\circ\text{C}$ ,<br>$f_{HCLK} = 72\text{ MHz}$<br>conforms to IEC 61000-4-4 | 4A          |

#### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

#### Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

### Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

### Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

**Table 48. EMI characteristics**

| Symbol           | Parameter  | Conditions                                                                                  | Monitored frequency band | Max vs. [f <sub>HSE</sub> /f <sub>HCLK</sub> ] | Unit |
|------------------|------------|---------------------------------------------------------------------------------------------|--------------------------|------------------------------------------------|------|
|                  |            |                                                                                             |                          | 8/72 MHz                                       |      |
| S <sub>EMI</sub> | Peak level | V <sub>DD</sub> = 1.8 V, T <sub>A</sub> = 25 °C, LQFP100 package compliant with IEC 61967-2 | 0.1 to 30 MHz            | 7                                              | dBμV |
|                  |            |                                                                                             | 30 to 130 MHz            | 16                                             |      |
|                  |            |                                                                                             | 130 MHz to 1GHz          | 23                                             |      |
|                  |            |                                                                                             | SAE EMI Level            | 4                                              | -    |

## 6.3.11 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

### Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

**Table 49. ESD absolute maximum ratings**

| Symbol                | Ratings                                               | Conditions                                         | Class | Maximum value <sup>(1)</sup> | Unit |
|-----------------------|-------------------------------------------------------|----------------------------------------------------|-------|------------------------------|------|
| V <sub>ESD(HBM)</sub> | Electrostatic discharge voltage (human body model)    | T <sub>A</sub> = +25 °C, conforming to JESD22-A114 | 2     | 2000                         | V    |
| V <sub>ESD(CDM)</sub> | Electrostatic discharge voltage (charge device model) | T <sub>A</sub> = +25 °C, conforming to JESD22-C101 | II    | 500                          |      |

1. Data based on characterization results, not tested in production.

### Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

**Table 50. Electrical sensitivities**

| Symbol | Parameter             | Conditions                                                 | Class      |
|--------|-----------------------|------------------------------------------------------------|------------|
| LU     | Static latch-up class | $T_A = +105\text{ }^{\circ}\text{C}$ conforming to JESD78A | II level A |

### 6.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below  $V_{SS}$  or above  $V_{DD}$  (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

#### Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of  $-5\text{ }\mu\text{A}/+0\text{ }\mu\text{A}$  range), or other functional failure (for example reset occurrence or oscillator frequency deviation).

The test results are given in [Table 51](#)

Table 51. I/O current injection susceptibility

| Symbol           | Description                                                                                                                                                                                                                                                                                                 | Functional susceptibility |                    | Unit |
|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------|--------------------|------|
|                  |                                                                                                                                                                                                                                                                                                             | Negative injection        | Positive injection |      |
| I <sub>INJ</sub> | Injected current on BOOT0                                                                                                                                                                                                                                                                                   | – 0                       | NA                 | mA   |
|                  | Injected current on PC0, PC1, PC2, PC3, PF2, PA0, PA1, PA2, PA3, PF4, PA4, PA5, PA6, PA7, PC4, PC5 with induced leakage current on other pins from this group less than -50 µA                                                                                                                              | – 5                       | -                  |      |
|                  | Injected current on PB0, PB1, PE7, PE8, PE9, PE10, PE11, PE12, PE13, PE14, PE15, PB12, PB13, PB14, PB15, PD8, PD9, PD10, PD11, PD12, PD13, PD14 with induced leakage current on other pins from this group less than -50 µA                                                                                 | – 5                       | -                  |      |
|                  | Injected current on PC0, PC1, PC2, PC3, PF2, PA0, PA1, PA2, PA3, PF4, PA4, PA5, PA6, PA7, PC4, PC5, PB0, PB1, PE7, PE8, PE9, PE10, PE11, PE12, PE13, PE14, PE15, PB12, PB13, PB14, PB15, PD8, PD9, PD10, PD11, PD12, PD13, PD14 with induced leakage current on other pins from this group less than 400 µA | -                         | +5                 |      |
|                  | Injected current on NPOR pin and on any other FT and FTf pins                                                                                                                                                                                                                                               | – 5                       | NA                 |      |
|                  | Injected current on any other pins                                                                                                                                                                                                                                                                          | – 5                       | +5                 |      |

**Note:** *It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.*

### 6.3.13 I/O port characteristics

#### General input/output characteristics

Unless otherwise specified, the parameters given in [Table 52](#) are derived from tests performed under the conditions summarized in [Table 24](#). All I/Os are CMOS and TTL compliant.

**Table 52. I/O static characteristics**

| Symbol    | Parameter                                         | Conditions                                                                             | Min                          | Typ                | Max                        | Unit       |
|-----------|---------------------------------------------------|----------------------------------------------------------------------------------------|------------------------------|--------------------|----------------------------|------------|
| $V_{IL}$  | Low level input voltage                           | TC and TTa I/O                                                                         | -                            | -                  | $0.3 V_{DD} + 0.07^{(1)}$  | V          |
|           |                                                   | FT and FTf I/O                                                                         | -                            | -                  | $0.475 V_{DD} - 0.2^{(1)}$ |            |
|           |                                                   | BOOT0                                                                                  | -                            | -                  | $0.3 V_{DD} - 0.3^{(1)}$   |            |
|           |                                                   | All I/Os except BOOT0                                                                  | -                            | -                  | $0.3 V_{DD}^{(2)}$         |            |
| $V_{IH}$  | High level input voltage                          | TC and TTa I/O                                                                         | $0.445 V_{DD} + 0.398^{(1)}$ | -                  | -                          | V          |
|           |                                                   | FT and FTf I/O                                                                         | $0.5 V_{DD} + 0.2^{(1)}$     | -                  | -                          |            |
|           |                                                   | BOOT0                                                                                  | $0.2 V_{DD} + 0.95^{(1)}$    | -                  | -                          |            |
|           |                                                   | All I/Os except BOOT0                                                                  | $0.7 V_{DD}^{(2)}$           | -                  | -                          |            |
| $V_{hys}$ | Schmitt trigger hysteresis                        | TC and TTa I/O                                                                         | -                            | 200 <sup>(1)</sup> | -                          | mV         |
|           |                                                   | FT and FTf I/O                                                                         | -                            | 100 <sup>(1)</sup> | -                          |            |
|           |                                                   | BOOT0                                                                                  | -                            | 300 <sup>(1)</sup> | -                          |            |
| $I_{lkg}$ | Input leakage current <sup>(3)</sup>              | TC, FT, FTf and POR I/O<br>TTa I/O in digital mode<br>$V_{SS} \leq V_{IN} \leq V_{DD}$ | -                            | -                  | $\pm 0.1$                  | $\mu A$    |
|           |                                                   | TTa I/O in digital mode<br>$V_{DD} \leq V_{IN} \leq V_{DDA}$                           | -                            | -                  | 1                          |            |
|           |                                                   | TTa I/O in analog mode<br>$V_{SS} \leq V_{IN} \leq V_{DDA}$                            | -                            | -                  | $\pm 0.2$                  |            |
|           |                                                   | FT and FTf I/O <sup>(4)</sup><br>$V_{DD} \leq V_{IN} \leq 5 V$                         | -                            | -                  | 10                         |            |
|           |                                                   | POR<br>$V_{DDA} \leq V_{IN} \leq 5 V$                                                  | -                            | -                  | 10                         |            |
| $R_{PU}$  | Weak pull-up equivalent resistor <sup>(5)</sup>   | $V_{IN} = V_{SS}$                                                                      | 25                           | 40                 | 55                         | k $\Omega$ |
| $R_{PD}$  | Weak pull-down equivalent resistor <sup>(5)</sup> | $V_{IN} = V_{DD}$                                                                      | 25                           | 40                 | 55                         | k $\Omega$ |
| $C_{IO}$  | I/O pin capacitance                               | -                                                                                      | -                            | 5                  | -                          | pF         |

1. Data based on design simulation.

2. Tested in production.

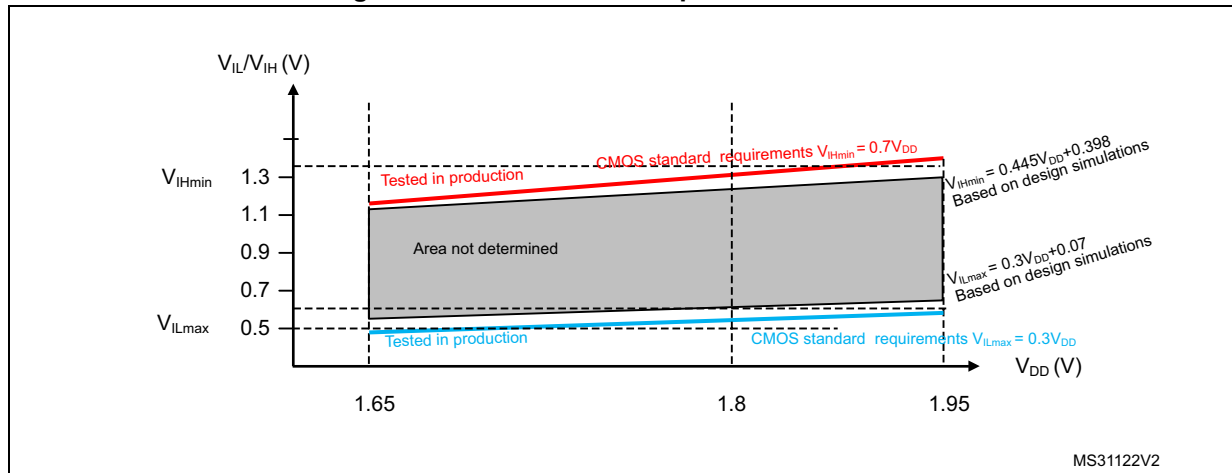
3. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to [Table 51: I/O current injection susceptibility](#).

4. To sustain a voltage higher than  $V_{DD} + 0.3 V$ , the internal pull-up/pull-down resistors must be disabled.

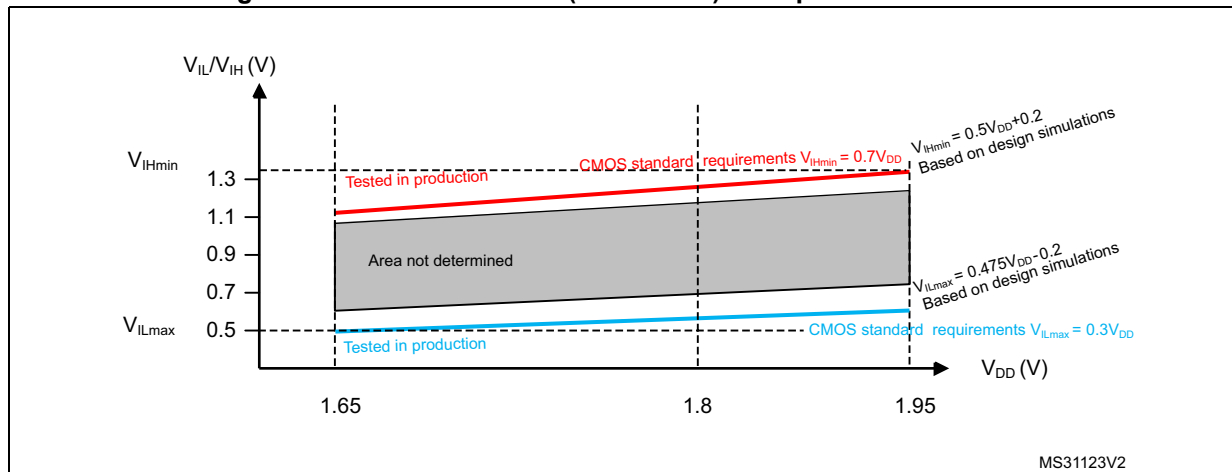
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters.

**Figure 18. TC and TTa I/O input characteristics**



**Figure 19. Five volt tolerant (FT and FTf) I/O input characteristics**



### Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to  $\pm 8$  mA, and sink or source up to  $\pm 20$  mA (with a relaxed  $V_{OL}/V_{OH}$ ).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in [Section 6.2](#):

- The sum of the currents sourced by all the I/Os on  $V_{DD}$ , plus the maximum Run consumption of the MCU sourced on  $V_{DD}$ , cannot exceed the absolute maximum rating  $\Sigma I_{VDD}$  (see [Table 22](#)).
- The sum of the currents sunk by all the I/Os on  $V_{SS}$  plus the maximum Run consumption of the MCU sunk on  $V_{SS}$  cannot exceed the absolute maximum rating  $\Sigma I_{VSS}$  (see [Table 22](#)).

### Output voltage levels

Unless otherwise specified, the parameters given in [Table 53](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 24](#). All I/Os (FT, TTA and TC unless otherwise specified) are CMOS and TTL compliant.

**Table 53. Output voltage characteristics**

| Symbol               | Parameter                                               | Conditions                                         | Min            | Max | Unit |
|----------------------|---------------------------------------------------------|----------------------------------------------------|----------------|-----|------|
| $V_{OL}^{(1)}$       | Output low level voltage for an I/O pin                 | $I_{IO} = +4$ mA<br>$1.65$ V $< V_{DD} < 1.95$ V   | -              | 0.4 | V    |
| $V_{OH}^{(2)}$       | Output high level voltage for an I/O pin                | $I_{IO} = -4$ mA<br>$1.65$ V $< V_{DD} < 1.95$ V   | $V_{DD} - 0.4$ | -   |      |
| $V_{OLFM+}^{(1)(3)}$ | Output low level voltage for an FTf I/O pin in FM+ mode | $I_{IO} = +10$ mA<br>$V_{DD} = 1.65$ V to $1.95$ V | -              | 0.4 |      |

1. The  $I_{IO}$  current sunk by the device must always respect the absolute maximum rating specified in [Table 22](#) and the sum of  $I_{IO}$  (I/O ports and control pins) must not exceed  $\Sigma I_{IO(PIN)}$ .
2. The  $I_{IO}$  current sourced by the device must always respect the absolute maximum rating specified in [Table 22](#) and the sum of  $I_{IO}$  (I/O ports and control pins) must not exceed  $\Sigma I_{IO(PIN)}$ .
3. Guaranteed by Design, not tested in production.

### Input/output AC characteristics

The definition and values of input/output AC characteristics are given in [Figure 20](#) and [Table 54](#), respectively.

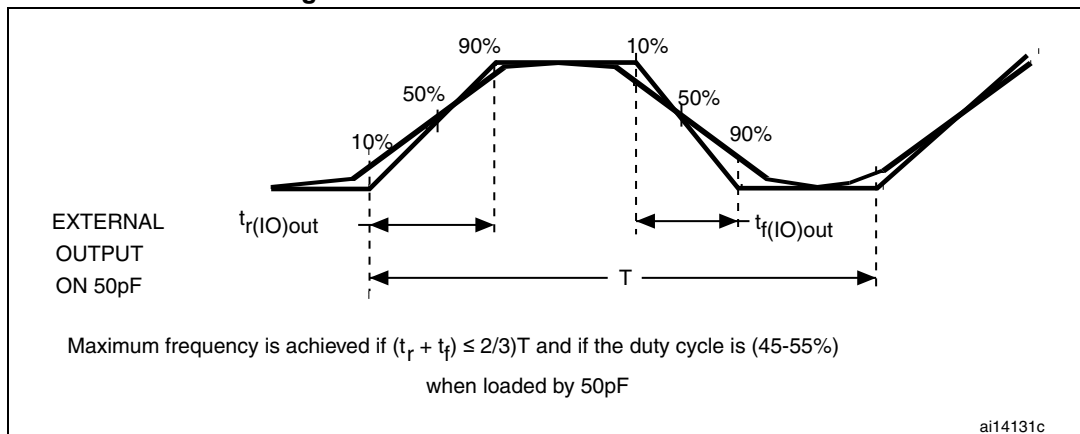
Unless otherwise specified, the parameters given are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 24](#).

**Table 54. I/O AC characteristics<sup>(1)</sup>**

| OSPEEDRx[1:0] value <sup>(1)</sup> | Symbol                          | Parameter                                                       | Conditions                                                           | Min | Max                   | Unit |
|------------------------------------|---------------------------------|-----------------------------------------------------------------|----------------------------------------------------------------------|-----|-----------------------|------|
| x0                                 | $f_{\max(\text{IO})\text{out}}$ | Maximum frequency <sup>(2)</sup>                                | $C_L = 50 \text{ pF}$ , $V_{DD} = 1.65 \text{ V to } 1.95 \text{ V}$ | -   | 1                     | MHz  |
|                                    | $t_{f(\text{IO})\text{out}}$    | Output high to low level fall time                              | $C_L = 50 \text{ pF}$ , $V_{DD} = 1.65 \text{ V to } 1.95 \text{ V}$ | -   | 125 <sup>(3)</sup>    | ns   |
|                                    | $t_{r(\text{IO})\text{out}}$    | Output low to high level rise time                              |                                                                      | -   | 125 <sup>(3)</sup>    |      |
| 01                                 | $f_{\max(\text{IO})\text{out}}$ | Maximum frequency <sup>(2)</sup>                                | $C_L = 50 \text{ pF}$ , $V_{DD} = 1.65 \text{ V to } 1.95 \text{ V}$ | -   | 4 <sup>(3)</sup>      | MHz  |
|                                    | $t_{f(\text{IO})\text{out}}$    | Output high to low level fall time                              | $C_L = 50 \text{ pF}$ , $V_{DD} = 1.65 \text{ V to } 1.95 \text{ V}$ | -   | 62.5 <sup>(3)</sup>   | ns   |
|                                    | $t_{r(\text{IO})\text{out}}$    | Output low to high level rise time                              |                                                                      | -   | 62.5 <sup>(3)</sup>   |      |
| 11                                 | $f_{\max(\text{IO})\text{out}}$ | Maximum frequency <sup>(2)</sup>                                | $C_L = 50 \text{ pF}$ , $V_{DD} = 1.65 \text{ V to } 1.95 \text{ V}$ | -   | 10 <sup>(3)</sup>     | MHz  |
|                                    | $t_{f(\text{IO})\text{out}}$    | Output high to low level fall time                              | $C_L = 50 \text{ pF}$ , $V_{DD} = 1.65 \text{ V to } 1.95 \text{ V}$ | -   | 25 <sup>(3)</sup>     | ns   |
|                                    | $t_{r(\text{IO})\text{out}}$    | Output low to high level rise time                              | $C_L = 50 \text{ pF}$ , $V_{DD} = 1.65 \text{ V to } 1.95 \text{ V}$ | -   | 25 <sup>(3)</sup>     |      |
| FM+ configuration <sup>(4)</sup>   | $f_{\max(\text{IO})\text{out}}$ | Maximum frequency <sup>(2)</sup>                                | $C_L = 50 \text{ pF}$ , $V_{DD} = 1.65 \text{ V to } 1.95 \text{ V}$ | -   | 0.5 <sup>(4)(3)</sup> | MHz  |
|                                    | $t_{f(\text{IO})\text{out}}$    | Output high to low level fall time                              |                                                                      | -   | 16 <sup>(4)(3)</sup>  | ns   |
|                                    | $t_{r(\text{IO})\text{out}}$    | Output low to high level rise time                              |                                                                      | -   | 44 <sup>(4)(3)</sup>  |      |
| -                                  | $t_{\text{EXTI}pw}$             | Pulse width of external signals detected by the EXTI controller | -                                                                    | 10  | -                     | ns   |

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the RM0316 reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in [Figure 20](#).
3. Guaranteed by design, not tested in production.
4. The I/O speed configuration is bypassed in FM+ I/O mode. Refer to the RM0316 STM32F303xx, STM32F358xC and STM32F328x4/6/8 reference manual (RM0316) for a description of FM+ I/O mode configuration.

Figure 20. I/O AC characteristics definition



### 6.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor,  $R_{PU}$  (see [Table 52](#)).

Unless otherwise specified, the parameters given in [Table 55](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 24](#).

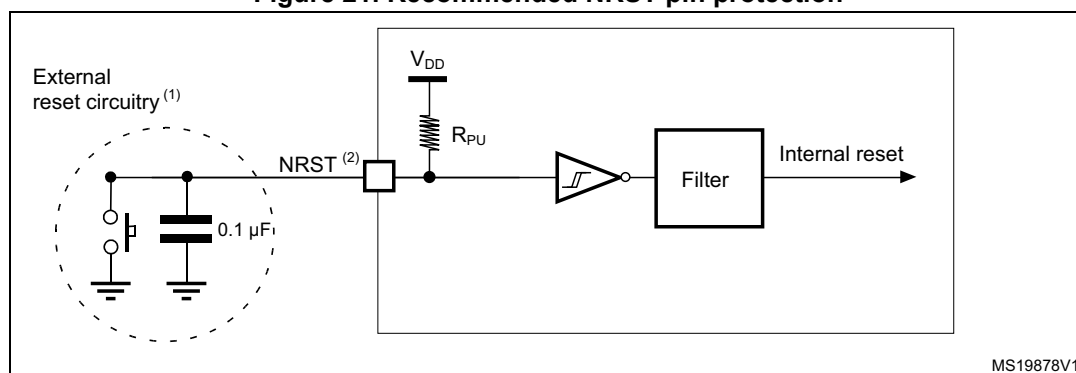
Table 55. NRST pin characteristics

| Symbol               | Parameter                                       | Conditions        | Min                         | Typ | Max                      | Unit       |
|----------------------|-------------------------------------------------|-------------------|-----------------------------|-----|--------------------------|------------|
| $V_{IL(NRST)}^{(1)}$ | NRST Input low level voltage                    | -                 | -                           | -   | $0.3V_{DD} + 0.07^{(1)}$ | V          |
| $V_{IH(NRST)}^{(1)}$ | NRST Input high level voltage                   | -                 | $0.445V_{DD} + 0.398^{(1)}$ | -   | -                        |            |
| $V_{hys(NRST)}$      | NRST Schmitt trigger voltage hysteresis         | -                 | -                           | 200 | -                        | mV         |
| $R_{PU}$             | Weak pull-up equivalent resistor <sup>(2)</sup> | $V_{IN} = V_{SS}$ | 25                          | 40  | 55                       | k $\Omega$ |
| $V_{F(NRST)}^{(1)}$  | NRST Input filtered pulse                       | -                 | -                           | -   | $100^{(1)}$              | ns         |
| $V_{NF(NRST)}^{(1)}$ | NRST Input not filtered pulse                   | -                 | $700^{(1)}$                 | -   | -                        | ns         |

1. Guaranteed by design, not tested in production.

2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Figure 21. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the  $V_{IL(NRST)}$  max level specified in [Table 55](#). Otherwise the reset will not be taken into account by the device.

### 6.3.15 NPOR pin characteristics

The NPOR pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor,  $R_{PU}$  (see [Table 56](#)) connected to  $V_{DDA}$  supply.

Unless otherwise specified, the parameters given in [Table 56](#) are derived from tests performed under ambient temperature and  $V_{DDA}$  supply voltage conditions summarized in [Table 24](#).

Table 56. NPOR pin characteristics

| Symbol <sup>(1)</sup> | Parameter                                       | Conditions        | Min                | Typ | Max                  | Unit       |
|-----------------------|-------------------------------------------------|-------------------|--------------------|-----|----------------------|------------|
| $V_{IL(NPOR)}$        | NPOR Input low level voltage                    | -                 | -                  | -   | $0.475V_{DDA} - 0.2$ | V          |
| $V_{IH(NPOR)}$        | NPOR Input high level voltage                   | -                 | $0.5V_{DDA} + 0.2$ | -   | -                    |            |
| $V_{hys(NPOR)}$       | NPOR Schmitt trigger voltage hysteresis         | -                 | -                  | 100 | -                    | mV         |
| $R_{PU}$              | Weak pull-up equivalent resistor <sup>(2)</sup> | $V_{IN} = V_{SS}$ | 25                 | 40  | 55                   | k $\Omega$ |

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

### 6.3.16 Timer characteristics

The parameters given in [Table 57](#) are guaranteed by design.

Refer to [Section 6.3.13: I/O port characteristics](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 57. TIMx<sup>(1)(2)</sup> characteristics

| Symbol                    | Parameter                                    | Conditions                                            | Min    | Max                    | Unit                 |
|---------------------------|----------------------------------------------|-------------------------------------------------------|--------|------------------------|----------------------|
| $t_{\text{res(TIM)}}$     | Timer resolution time                        | -                                                     | 1      | -                      | $t_{\text{TIMxCLK}}$ |
|                           |                                              | $f_{\text{TIMxCLK}} = 72 \text{ MHz}$                 | 13.9   | -                      | ns                   |
|                           |                                              | $f_{\text{TIMxCLK}} = 144 \text{ MHz}$ ,<br>$x = 1.8$ | 6.95   | -                      | ns                   |
| $f_{\text{EXT}}$          | Timer external clock frequency on CH1 to CH4 | -                                                     | 0      | $f_{\text{TIMxCLK}}/2$ | MHz                  |
|                           |                                              | $f_{\text{TIMxCLK}} = 72 \text{ MHz}$                 | 0      | 36                     | MHz                  |
| $\text{Res}_{\text{TIM}}$ | Timer resolution                             | TIMx (except TIM2)                                    | -      | 16                     | bit                  |
|                           |                                              | TIM2                                                  | -      | 32                     |                      |
| $t_{\text{COUNTER}}$      | 16-bit counter clock period                  | -                                                     | 1      | 65536                  | $t_{\text{TIMxCLK}}$ |
|                           |                                              | $f_{\text{TIMxCLK}} = 72 \text{ MHz}$                 | 0.0139 | 910                    | $\mu\text{s}$        |
|                           |                                              | $f_{\text{TIMxCLK}} = 144 \text{ MHz}$ ,<br>$x = 1.8$ | 0.0069 | 455                    | $\mu\text{s}$        |
| $t_{\text{MAX\_COUNT}}$   | Maximum possible count with 32-bit counter   | -                                                     | -      | $65536 \times 65536$   | $t_{\text{TIMxCLK}}$ |
|                           |                                              | $f_{\text{TIMxCLK}} = 72 \text{ MHz}$                 | -      | 59.65                  | s                    |
|                           |                                              | $f_{\text{TIMxCLK}} = 144 \text{ MHz}$ ,<br>$x = 1.8$ | -      | 29.825                 | s                    |

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3, TIM4, TIM6, TIM15, TIM16 and TIM17 timers.

2. Guaranteed by design, not tested in production.

**Table 58. IWDG min/max timeout period at 40 kHz (LSI) <sup>(1)</sup>**

| Prescaler divider | PR[2:0] bits | Min timeout (ms) RL[11:0]=<br>0x000 | Max timeout (ms) RL[11:0]=<br>0xFFFF |
|-------------------|--------------|-------------------------------------|--------------------------------------|
| /4                | 0            | 0.1                                 | 409.6                                |
| /8                | 1            | 0.2                                 | 819.2                                |
| /16               | 2            | 0.4                                 | 1638.4                               |
| /32               | 3            | 0.8                                 | 3276.8                               |
| /64               | 4            | 1.6                                 | 6553.6                               |
| /128              | 5            | 3.2                                 | 13107.2                              |
| /256              | 7            | 6.4                                 | 26214.4                              |

1. These timings are given for a 40 kHz clock but the microcontroller's internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

**Table 59. WWDG min-max timeout value @72 MHz (PCLK)<sup>(1)</sup>**

| Prescaler | WDGTB | Min timeout value | Max timeout value |
|-----------|-------|-------------------|-------------------|
| 1         | 0     | 0.05687           | 3.6409            |
| 2         | 1     | 0.1137            | 7.2817            |
| 4         | 2     | 0.2275            | 14.564            |
| 8         | 3     | 0.4551            | 29.127            |

1. Guaranteed by design, not tested in production.

### 6.3.17 Communications interfaces

#### I<sup>2</sup>C interface characteristics

The I<sup>2</sup>C interface meets the requirements of the standard I<sup>2</sup>C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V<sub>DD</sub> is disabled, but is still present.

The I<sup>2</sup>C characteristics are described in [Table 60](#). Refer also to [Section 6.3.13: I/O port characteristics](#) for more details on the input/output alternate function characteristics (SDA and SCL).

**Table 60. I2C timings specification (see I2C specification, rev.03, June 2007)<sup>(1)</sup>**

| Symbol              | Parameter                                        | Standard mode |                     | Fast mode |                    | Fast Mode Plus |                     | Unit |
|---------------------|--------------------------------------------------|---------------|---------------------|-----------|--------------------|----------------|---------------------|------|
|                     |                                                  | Min           | Max                 | Min       | Max                | Min            | Max                 |      |
| f <sub>SCL</sub>    | SCL clock frequency                              | 0             | 100                 | 0         | 400                | 0              | 1000                | KHz  |
| t <sub>LOW</sub>    | Low period of the SCL clock                      | 4.7           | -                   | 1.3       | -                  | 0.5            | -                   | μs   |
| t <sub>HIGH</sub>   | High Period of the SCL clock                     | 4             | -                   | 0.6       | -                  | 0.26           | -                   | μs   |
| t <sub>r</sub>      | Rise time of both SDA and SCL signals            | -             | 1000                | -         | 300                | -              | 120                 | ns   |
| t <sub>f</sub>      | Fall time of both SDA and SCL signals            | -             | 300                 | -         | 300                | -              | 120                 | ns   |
| t <sub>HD;DAT</sub> | Data hold time                                   | 0             | -                   | 0         | -                  | 0              | -                   | μs   |
| t <sub>VD;DAT</sub> | Data valid time                                  | -             | 3.45 <sup>(2)</sup> | -         | 0.9 <sup>(2)</sup> | -              | 0.45 <sup>(2)</sup> | μs   |
| t <sub>VD;ACK</sub> | Data valid acknowledge time                      | -             | 3.45 <sup>(2)</sup> | -         | 0.9 <sup>(2)</sup> | -              | 0.45 <sup>(2)</sup> | μs   |
| t <sub>SU;DAT</sub> | Data setup time                                  | 250           | -                   | 100       | -                  | 50             | -                   | ns   |
| t <sub>HD;STA</sub> | Hold time (repeated) START condition             | 4.0           | -                   | 0.6       | -                  | 0.26           | -                   | μs   |
| t <sub>SU;STA</sub> | Set-up time for a repeated START condition       | 4.7           | -                   | 0.6       | -                  | 0.26           | -                   | μs   |
| t <sub>SU;STO</sub> | Set-up time for STOP condition                   | 4.0           | -                   | 0.6       | -                  | 0.26           | -                   | μs   |
| t <sub>BUF</sub>    | Bus free time between a STOP and START condition | 4.7           | -                   | 1.3       | -                  | 0.5            | -                   | μs   |
| C <sub>b</sub>      | Capacitive load for each bus line                | -             | 400                 | -         | 400                | -              | 550                 | pF   |

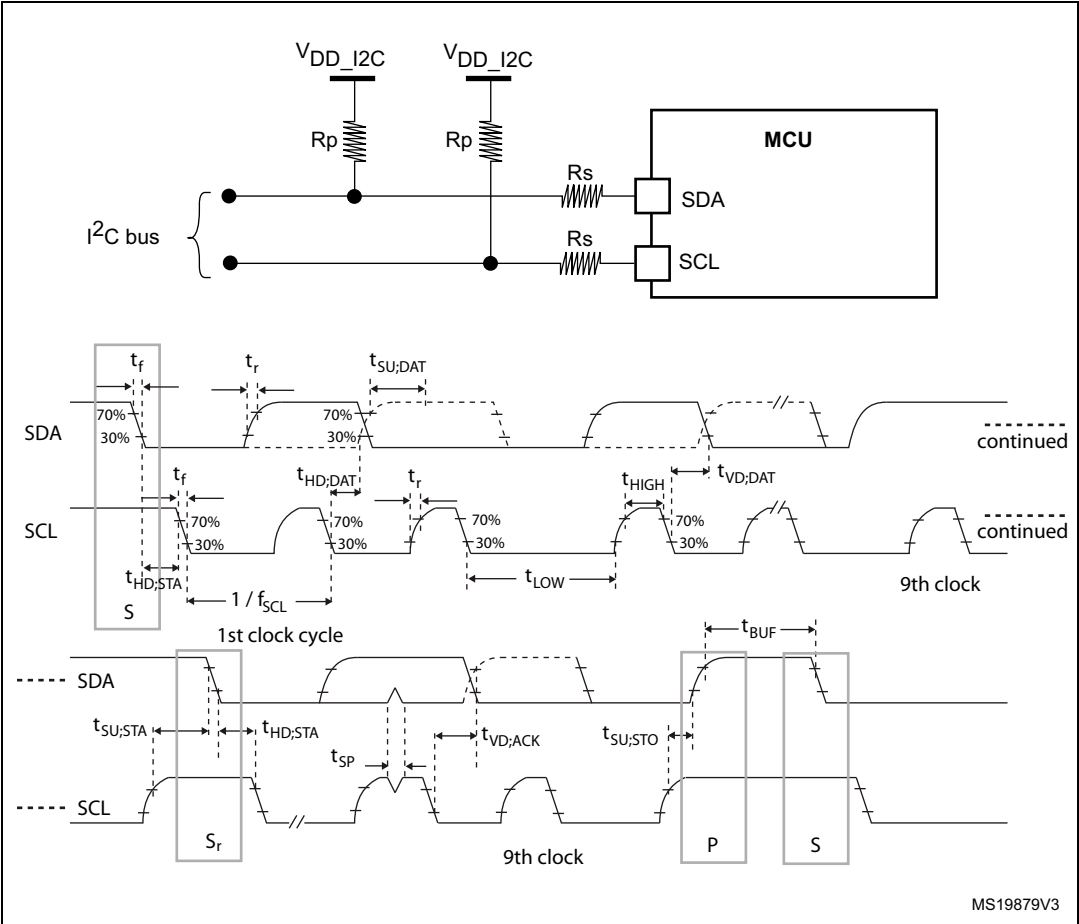
1. The I2C characteristics are the requirements from I2C bus specification rev03. They are guaranteed by design when I2Cx\_TIMING register is correctly programmed (Refer to the reference manual). These characteristics are not tested in production.
2. The maximum t<sub>HD;DAT</sub> could be 3.45 μs, 0.9 μs and 0.45 μs for standard mode, fast mode and fast mode plus, but must be less than the maximum of t<sub>VD;DAT</sub> or t<sub>VD;ACK</sub> by a transition time.

Table 61. I2C analog filter characteristics<sup>(1)</sup>

| Symbol   | Parameter                                                      | Min | Max | Unit |
|----------|----------------------------------------------------------------|-----|-----|------|
| $t_{SP}$ | Pulse width of spikes that are suppressed by the analog filter | 50  | 260 | ns   |

1. Guaranteed by design, not tested in production.

Figure 22. I2C bus AC waveforms and measurement circuit



1. Rs: Series protection resistors, Rp: Pull-up resistors, VDD\_I2C: I2C bus supply.

**SPI/I<sup>2</sup>S characteristics**

Unless otherwise specified, the parameters given in [Table 62](#) for SPI or in [Table 63](#) for I<sup>2</sup>S are derived from tests performed under ambient temperature,  $f_{PCLKx}$  frequency and  $V_{DD}$  supply voltage conditions summarized in [Table 24](#).

Refer to [Section 6.3.13: I/O port characteristics](#) for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I<sup>2</sup>S).

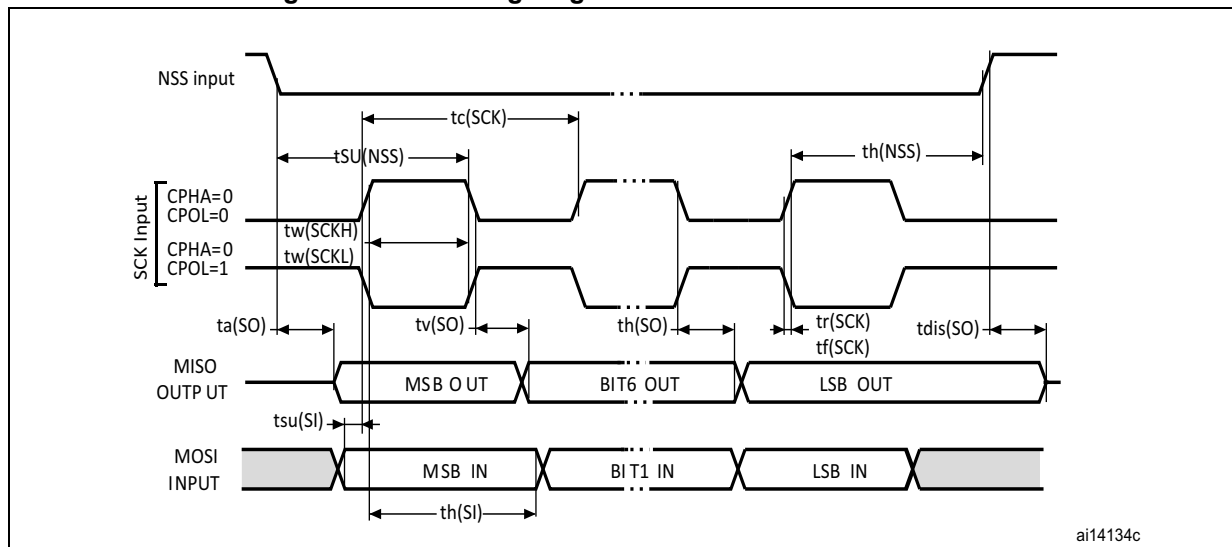
**Table 62. SPI characteristics<sup>(1)</sup>**

| Symbol                       | Parameter                        | Conditions                                     | Min           | Typ        | Max                 | Unit |
|------------------------------|----------------------------------|------------------------------------------------|---------------|------------|---------------------|------|
| $f_{SCK}$<br>$1/t_{c(SCK)}$  | SPI clock frequency              | Master mode, SPI1/2/3                          | -             | -          | 18                  | MHz  |
|                              |                                  | Slave mode, SPI1/2/3                           |               |            | 18                  |      |
|                              |                                  | Slave mode transmitter/full duplex SPI1/2/3    |               |            | 12.5 <sup>(2)</sup> |      |
| Duty(SCK)                    | SPI slave input clock duty cycle | Slave mode                                     | 30            | 50         | 70                  | %    |
| $t_{su}(NSS)$                | NSS setup time                   | Slave mode, SPI presc = 2                      | 4* $T_{pclk}$ | -          | -                   | ns   |
| $t_h(NSS)$                   | NSS hold time                    | Slave mode SPI presc = 2                       | 2* $T_{pclk}$ | -          | -                   |      |
| $t_w(SCKH)$<br>$t_w(SCKL)$   | SCK high and low time            | Master mode, $f_{PCLK} = 36$ MHz,<br>presc = 4 | $T_{pclk}-2$  | $T_{pclk}$ | $T_{pclk}+2$        |      |
| $t_{su}(MI)$<br>$t_{su}(SI)$ | Data input setup time            | Master mode                                    | 5.5           | -          | -                   |      |
|                              |                                  | Slave mode                                     | 6.5           | -          | -                   |      |
| $t_h(MI)$<br>$t_h(SI)$       | Data input hold time             | Master mode                                    | 5             | -          | -                   |      |
|                              |                                  | Slave mode                                     | 5             | -          | -                   |      |
| $t_a(SO)$                    | Data output access time          | Slave mode, $f_{PCLK} = 24$ MHz                | 0             | -          | 4* $T_{pclk}$       |      |
| $t_{dis}(SO)$                | Data output disable time         | Slave mode                                     | 0             | -          | 24                  |      |
| $t_v(SO)$                    | Data output valid time           | Slave mode (after enable edge)                 | -             | 25         | 39                  |      |
| $t_v(MO)$                    | Data output valid time           | Master mode (after enable edge)                | -             | 1.5        | 3                   |      |
| $t_h(SO)$                    | Data output hold time            | Slave mode (after enable edge)                 | 11            | -          | -                   |      |
| $t_h(MO)$                    |                                  | Master mode (after enable edge)                | 0             | -          | -                   |      |

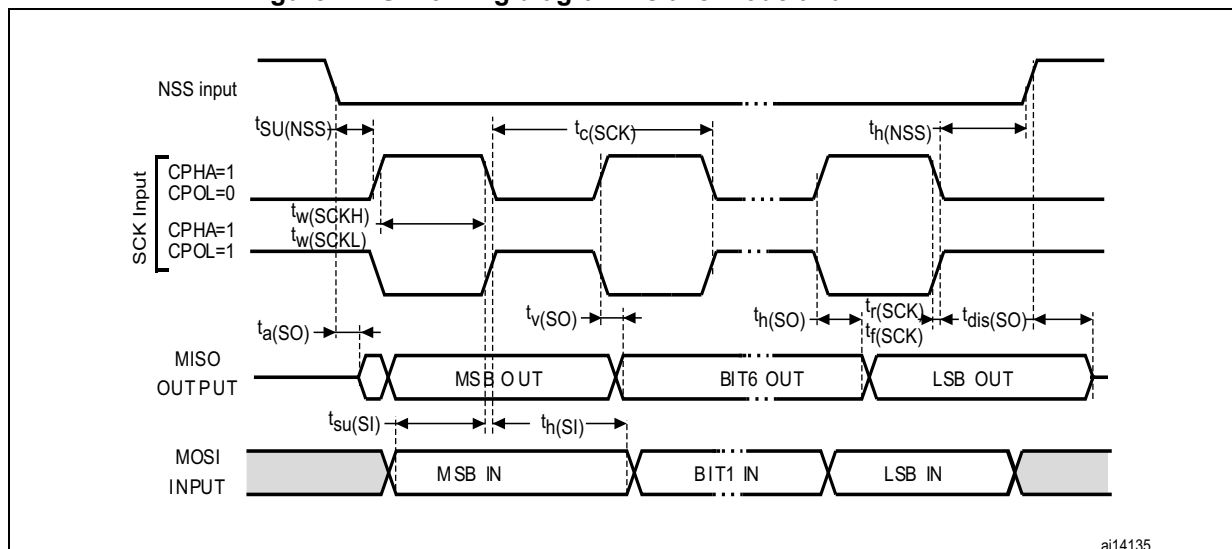
1. Data based on characterization results, not tested in production.

2. Maximum frequency in Slave transmitter mode is determined by the sum of  $t_v(SO)$  and  $t_{su}(MI)$  which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having  $t_{su}(MI) = 0$  while Duty(SCK) = 50%.

Figure 23. SPI timing diagram - slave mode and CPHA = 0

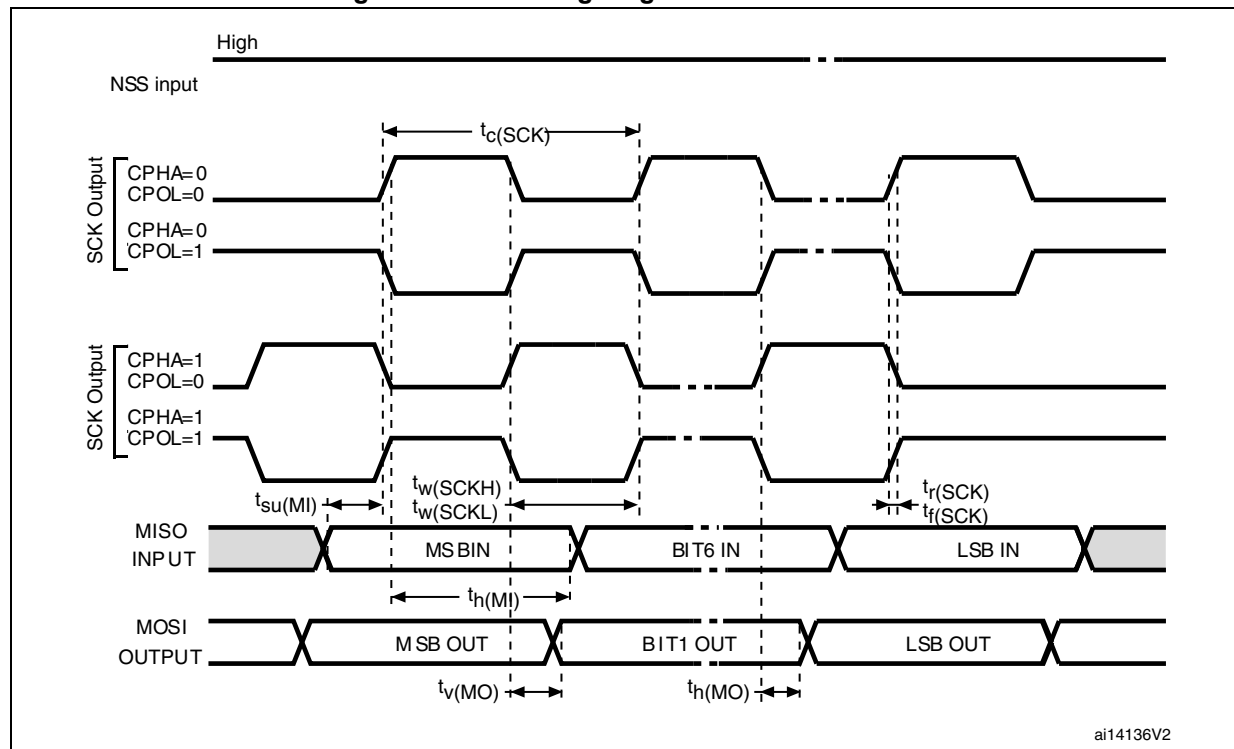


ai14134c

Figure 24. SPI timing diagram - slave mode and CPHA = 1<sup>(1)</sup>

ai14135

1. Measurement points are done at  $0.5V_{DD}$  and with external  $C_L = 30$  pF.

Figure 25. SPI timing diagram - master mode<sup>(1)</sup>

ai14136V2

1. Measurement points are done at 0.5V<sub>DD</sub> and with external C<sub>L</sub> = 30 pF.

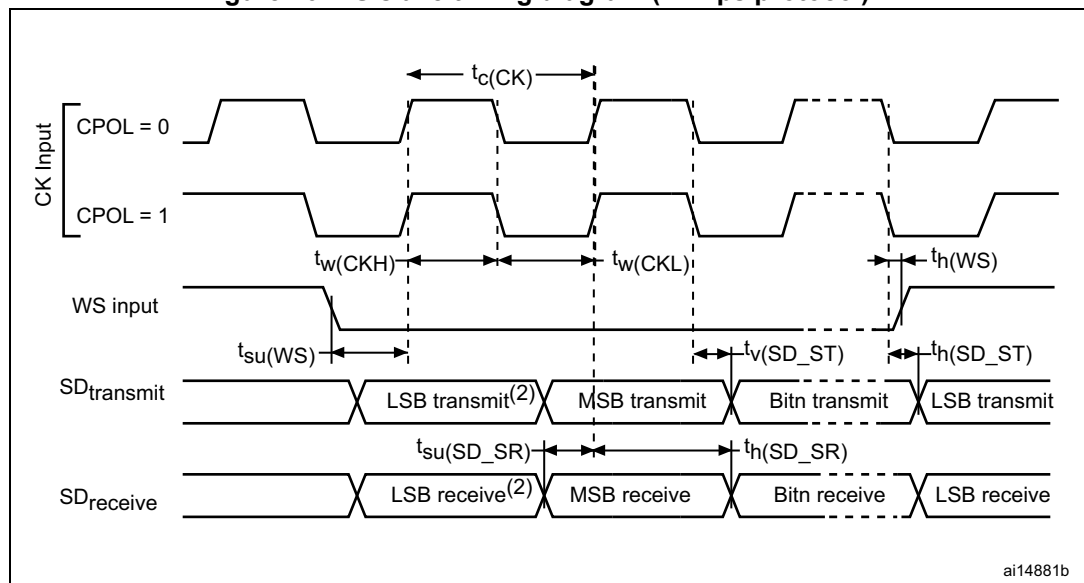
Table 63. I<sup>2</sup>S characteristics<sup>(1)</sup>

| Symbol                     | Parameter                                     | Conditions                                                 | Min   | Max    | Unit |
|----------------------------|-----------------------------------------------|------------------------------------------------------------|-------|--------|------|
| $f_{CK}$<br>$1/t_{c(CK)}$  | I <sup>2</sup> S clock frequency              | Master data: 16 bits,<br>audio freq=48 kHz                 | 1.496 | 1.503  | MHz  |
|                            |                                               | Slave                                                      | 0     | 12.288 |      |
| $t_{r(CK)}$<br>$t_{f(CK)}$ | I <sup>2</sup> S clock rise and fall time     | Capacitive load<br>C <sub>L</sub> = 30 pF                  | -     | 8      | ns   |
| $t_{w(CKH)}$               | I <sup>2</sup> S clock high time              | Master $f_{PCLK}$ = 36 MHz,<br>audio frequency =<br>48 kHz | 331   | -      |      |
| $t_{w(CKL)}$               | I <sup>2</sup> S clock low time               |                                                            | 332   | -      |      |
| $t_{v(WS)}$                | WS valid time                                 | Master mode                                                | 4     | -      |      |
| $t_{h(WS)}$                | WS hold time                                  | Master mode                                                | 4     | -      |      |
| $t_{su(WS)}$               | WS setup time                                 | Slave mode                                                 | 4     | -      |      |
| $t_{h(WS)}$                | WS hold time                                  | Slave mode                                                 | 0     | -      |      |
| Duty Cycle                 | I <sup>2</sup> S slave input clock duty cycle | Slave mode                                                 | 30    | 70     | %    |

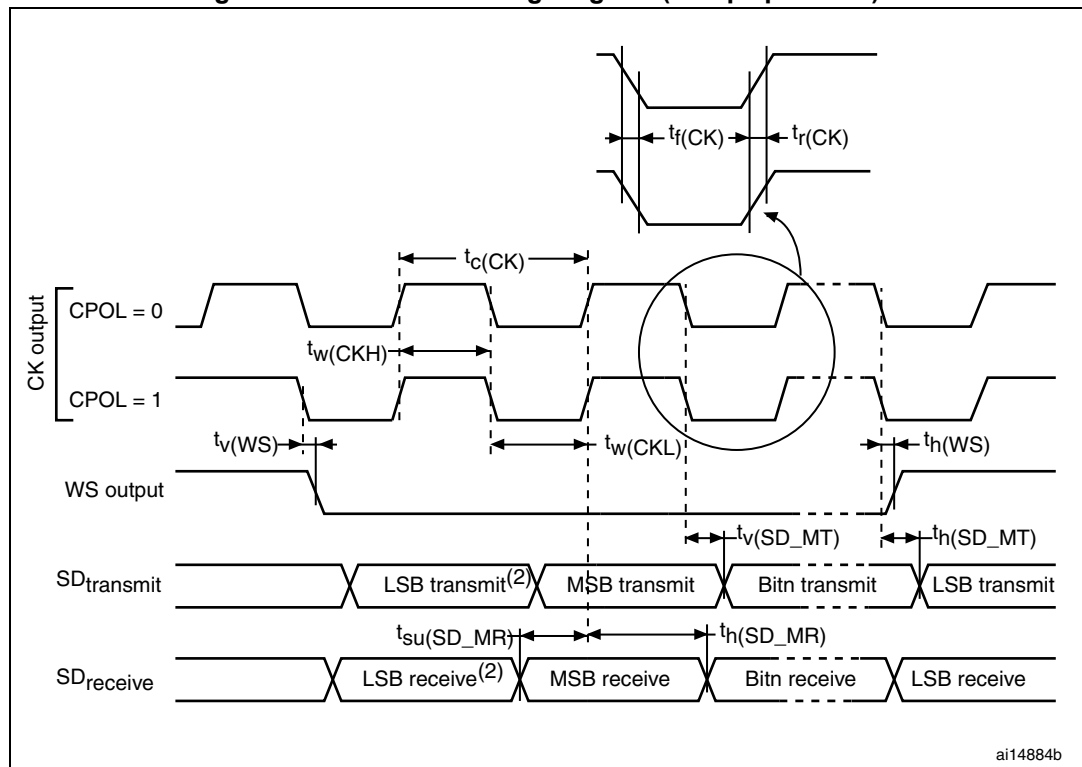
Table 63. I<sup>2</sup>S characteristics<sup>(1)</sup> (continued)

| Symbol           | Parameter              | Conditions                             | Min | Max | Unit |
|------------------|------------------------|----------------------------------------|-----|-----|------|
| $t_{su(SD\_MR)}$ | Data input setup time  | Master receiver                        | 9   | -   | ns   |
| $t_{su(SD\_SR)}$ | Data input setup time  | Slave receiver                         | 2   | -   |      |
| $t_{h(SD\_MR)}$  | Data input hold time   | Master receiver                        | 0   | -   |      |
| $t_{h(SD\_SR)}$  |                        | Slave receiver                         | 0   | -   |      |
| $t_{v(SD\_ST)}$  | Data output valid time | Slave transmitter (after enable edge)  | -   | 29  |      |
| $t_{h(SD\_ST)}$  | Data output hold time  | Slave transmitter (after enable edge)  | 12  | -   |      |
| $t_{v(SD\_MT)}$  | Data output valid time | Master transmitter (after enable edge) | -   | 3   |      |
| $t_{h(SD\_MT)}$  | Data output hold time  | Master transmitter (after enable edge) | 2   | -   |      |

1. Data based on characterization results, not tested in production.

Figure 26. I<sup>2</sup>S slave timing diagram (Philips protocol)<sup>(1)</sup>

1. Measurement points are done at 0.5V<sub>DD</sub> and with external C<sub>L</sub>=30 pF.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 27. I<sup>2</sup>S master timing diagram (Philips protocol)<sup>(1)</sup>

ai14884b

1. Measurement points are done at 0.5V<sub>DD</sub> and with external C<sub>L</sub>=30 pF.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

### CAN (controller area network) interface

Refer to [Section 6.3.13: I/O port characteristics](#) for more details on the input/output alternate function characteristics (CAN\_TX and CAN\_RX).

### 6.3.18 ADC characteristics

Unless otherwise specified, the parameters given in [Table 64](#) to [Table 67](#) are guaranteed by design, with conditions summarized in [Table 24](#).

**Table 64. ADC characteristics**

| Symbol      | Parameter                                                             | Conditions                         | Min    | Typ   | Max       | Unit    |
|-------------|-----------------------------------------------------------------------|------------------------------------|--------|-------|-----------|---------|
| $V_{DDA}$   | Analog supply voltage for ADC                                         | -                                  | 1.8    | -     | 3.6       | V       |
| $I_{DDA}$   | ADC current consumption on VDDA pin (see <a href="#">Figure 28</a> )  | Single-ended mode, 5 MSPS          | -      | 907   | 1033.0    | $\mu A$ |
|             |                                                                       | Single-ended mode, 1 MSPS          | -      | 194   | 285.5     |         |
|             |                                                                       | Single-ended mode, 200 KSPS        | -      | 51.5  | 70        |         |
|             |                                                                       | Differential mode, 5 MSPS          | -      | 887.5 | 1009      |         |
|             |                                                                       | Differential mode, 1 MSPS          | -      | 212   | 285       |         |
|             |                                                                       | Differential mode, 200 KSPS        | -      | 51    | 69.5      |         |
| $V_{REF+}$  | Positive reference voltage                                            | -                                  | 2      | -     | $V_{DDA}$ | V       |
| $I_{REF}$   | ADC current consumption on VREF+ pin (see <a href="#">Figure 29</a> ) | Single-ended mode, 5 MSPS          | -      | 104   | 139       | $\mu A$ |
|             |                                                                       | Single-ended mode, 1 MSPS          | -      | 20.4  | 37        |         |
|             |                                                                       | Single-ended mode, 200 KSPS        | -      | 3.3   | 11.3      |         |
|             |                                                                       | Differential mode, 5 MSPS          | -      | 174   | 235       |         |
|             |                                                                       | Differential mode, 1 MSPS          | -      | 34.6  | 52.6      |         |
|             |                                                                       | Differential mode, 200 KSPS        | -      | 6     | 13.6      |         |
| $f_{ADC}$   | ADC clock frequency                                                   |                                    | 0.14   | -     | 72        | MHz     |
| $f_S^{(1)}$ | Sampling rate                                                         | Resolution = 12 bits, Fast Channel | 0.01   | -     | 5.14      | MSPS    |
|             |                                                                       | Resolution = 10 bits, Fast Channel | 0.012  | -     | 6         |         |
|             |                                                                       | Resolution = 8 bits, Fast Channel  | 0.014  | -     | 7.2       |         |
|             |                                                                       | Resolution = 6 bits, Fast Channel  | 0.0175 | -     | 9         |         |

Table 64. ADC characteristics (continued)

| Symbol                            | Parameter                                                                            | Conditions                                                | Min                                                                          | Typ | Max               | Unit               |
|-----------------------------------|--------------------------------------------------------------------------------------|-----------------------------------------------------------|------------------------------------------------------------------------------|-----|-------------------|--------------------|
| $f_{\text{TRIG}}^{(1)}$           | External trigger frequency                                                           | $f_{\text{ADC}} = 72 \text{ MHz}$<br>Resolution = 12 bits | -                                                                            | -   | 5.14              | MHz                |
|                                   |                                                                                      | Resolution = 12 bits                                      | -                                                                            | -   | 14                | $1/f_{\text{ADC}}$ |
| $V_{\text{AIN}}$                  | Conversion voltage range <sup>(2)</sup>                                              | -                                                         | 0                                                                            | -   | $V_{\text{REF+}}$ | V                  |
| $R_{\text{AIN}}^{(1)}$            | External input impedance                                                             | -                                                         | -                                                                            | -   | 100               | k $\Omega$         |
| $C_{\text{ADC}}^{(1)}$            | Internal sample and hold capacitor                                                   | -                                                         | -                                                                            | 5   | -                 | pF                 |
| $t_{\text{CAL}}^{(1)}$            | Calibration time                                                                     | $f_{\text{ADC}} = 72 \text{ MHz}$                         | 1.56                                                                         |     |                   | $\mu\text{s}$      |
|                                   |                                                                                      | -                                                         | 112                                                                          |     |                   | $1/f_{\text{ADC}}$ |
| $t_{\text{latr}}^{(1)}$           | Trigger conversion latency<br>Regular and injected channels without conversion abort | CKMODE = 00                                               | 1.5                                                                          | 2   | 2.5               | $1/f_{\text{ADC}}$ |
|                                   |                                                                                      | CKMODE = 01                                               | -                                                                            | -   | 2                 | $1/f_{\text{ADC}}$ |
|                                   |                                                                                      | CKMODE = 10                                               | -                                                                            | -   | 2.25              | $1/f_{\text{ADC}}$ |
|                                   |                                                                                      | CKMODE = 11                                               | -                                                                            | -   | 2.125             | $1/f_{\text{ADC}}$ |
| $t_{\text{latrinj}}^{(1)}$        | Trigger conversion latency<br>Injected channels aborting a regular conversion        | CKMODE = 00                                               | 2.5                                                                          | 3   | 3.5               | $1/f_{\text{ADC}}$ |
|                                   |                                                                                      | CKMODE = 01                                               | -                                                                            | -   | 3                 | $1/f_{\text{ADC}}$ |
|                                   |                                                                                      | CKMODE = 10                                               | -                                                                            | -   | 3.25              | $1/f_{\text{ADC}}$ |
|                                   |                                                                                      | CKMODE = 11                                               | -                                                                            | -   | 3.125             | $1/f_{\text{ADC}}$ |
| $t_{\text{s}}^{(1)}$              | Sampling time                                                                        | $f_{\text{ADC}} = 72 \text{ MHz}$                         | 0.021                                                                        | -   | 8.35              | $\mu\text{s}$      |
|                                   |                                                                                      | -                                                         | 1.5                                                                          | -   | 601.5             | $1/f_{\text{ADC}}$ |
| $T_{\text{ADCVRREG\_STUP}}^{(1)}$ | ADC Voltage Regulator Start-up time                                                  | -                                                         | -                                                                            | -   | 10                | $\mu\text{s}$      |
| $t_{\text{CONV}}^{(1)}$           | Total conversion time (including sampling time)                                      | $f_{\text{ADC}} = 72 \text{ MHz}$<br>Resolution = 12 bits | 0.19                                                                         | -   | 8.52              | $\mu\text{s}$      |
|                                   |                                                                                      | Resolution = 12 bits                                      | 14 to 614 ( $t_{\text{s}}$ for sampling + 12.5 for successive approximation) |     |                   | $1/f_{\text{ADC}}$ |

1. Data guaranteed by design, not tested in production.

2.  $V_{\text{REF+}}$  can be internally connected to  $V_{\text{DDA}}$  and  $V_{\text{REF-}}$  can be internally connected to  $V_{\text{SSA}}$ , depending on the package. Refer to [Section 4: Pinouts and pin description](#) for further details.

Figure 28. ADC typical current consumption on VDDA pin

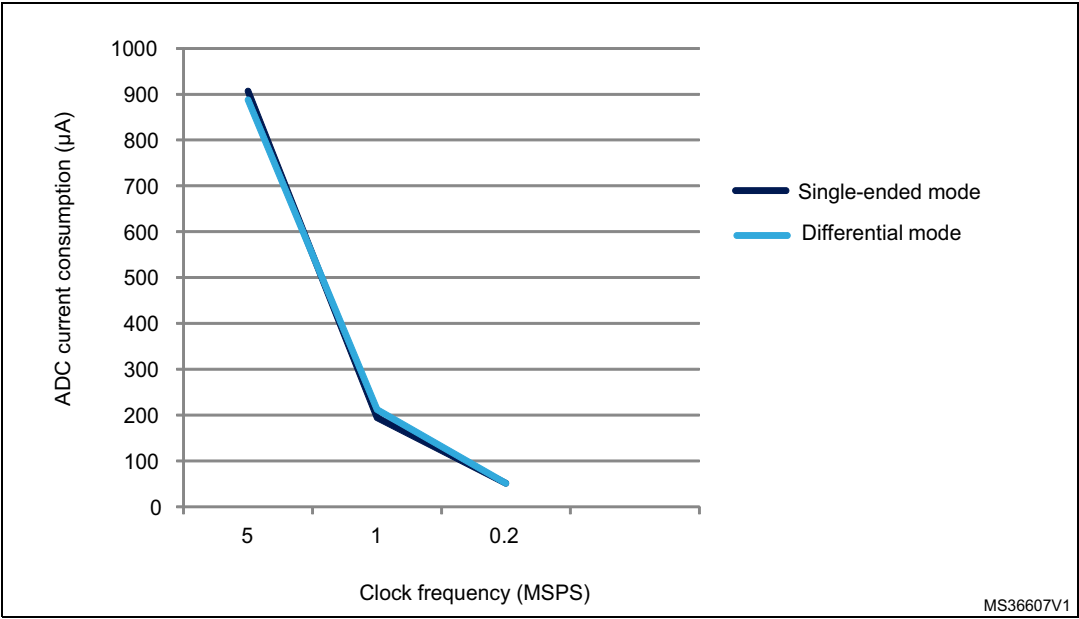


Figure 29. ADC typical current consumption on VREF+ pin

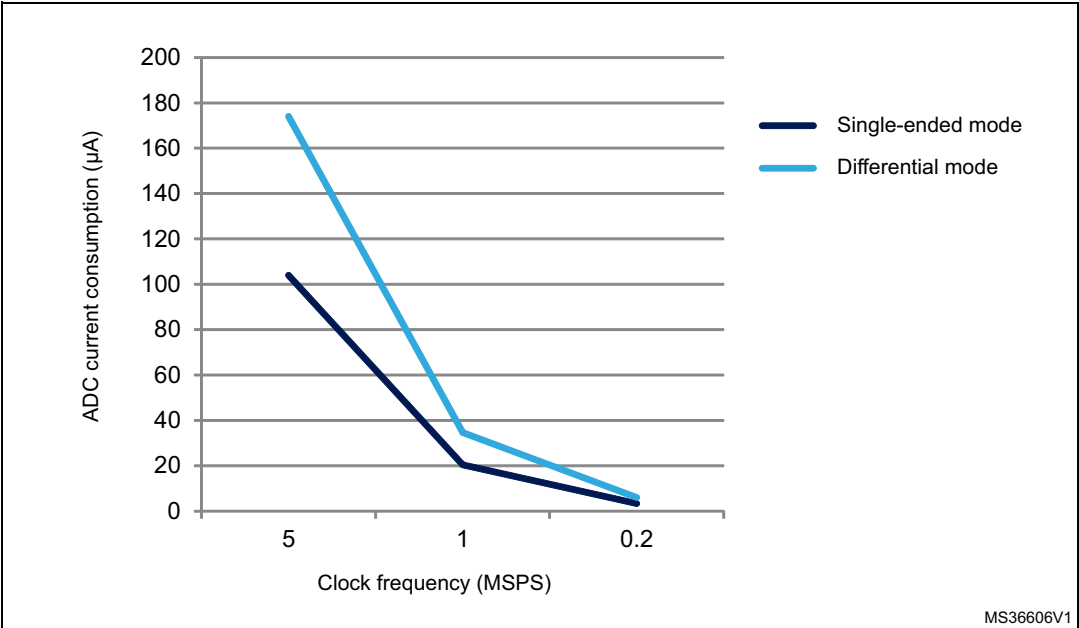


Table 65. Maximum ADC  $R_{AIN}$  <sup>(1)</sup>

| Resolution | Sampling cycle @ 72 MHz | Sampling time [ns] @ 72 MHz | $R_{AIN}$ max (k $\Omega$ )  |               |                               |
|------------|-------------------------|-----------------------------|------------------------------|---------------|-------------------------------|
|            |                         |                             | Fast channels <sup>(2)</sup> | Slow channels | Other channels <sup>(3)</sup> |
| 12 bits    | 1.5                     | 20.83                       | 0.018                        | NA            | NA                            |
|            | 2.5                     | 34.72                       | 0.150                        | NA            | 0.022                         |
|            | 4.5                     | 62.50                       | 0.470                        | 0.220         | 0.180                         |
|            | 7.5                     | 104.17                      | 0.820                        | 0.560         | 0.470                         |
|            | 19.5                    | 270.83                      | 2.70                         | 1.80          | 1.50                          |
|            | 61.5                    | 854.17                      | 8.20                         | 6.80          | 4.70                          |
|            | 181.5                   | 2520.83                     | 22.0                         | 18.0          | 15.0                          |
|            | 601.5                   | 8354.17                     | 82.0                         | 68.0          | 47.0                          |
| 10 bits    | 1.5                     | 20.83                       | 0.082                        | NA            | NA                            |
|            | 2.5                     | 34.72                       | 0.270                        | 0.082         | 0.100                         |
|            | 4.5                     | 62.50                       | 0.560                        | 0.390         | 0.330                         |
|            | 7.5                     | 104.17                      | 1.20                         | 0.82          | 0.68                          |
|            | 19.5                    | 270.83                      | 3.30                         | 2.70          | 2.20                          |
|            | 61.5                    | 854.17                      | 10.0                         | 8.2           | 6.8                           |
|            | 181.5                   | 2520.83                     | 33.0                         | 27.0          | 22.0                          |
|            | 601.5                   | 8354.17                     | 100.0                        | 82.0          | 68.0                          |
| 8 bits     | 1.5                     | 20.83                       | 0.150                        | NA            | 0.039                         |
|            | 2.5                     | 34.72                       | 0.390                        | 0.180         | 0.180                         |
|            | 4.5                     | 62.50                       | 0.820                        | 0.560         | 0.470                         |
|            | 7.5                     | 104.17                      | 1.50                         | 1.20          | 1.00                          |
|            | 19.5                    | 270.83                      | 3.90                         | 3.30          | 2.70                          |
|            | 61.5                    | 854.17                      | 12.00                        | 12.00         | 8.20                          |
|            | 181.5                   | 2520.83                     | 39.00                        | 33.00         | 27.00                         |
|            | 601.5                   | 8354.17                     | 100.00                       | 100.00        | 82.00                         |
| 6 bits     | 1.5                     | 20.83                       | 0.270                        | 0.100         | 0.150                         |
|            | 2.5                     | 34.72                       | 0.560                        | 0.390         | 0.330                         |
|            | 4.5                     | 62.50                       | 1.200                        | 0.820         | 0.820                         |
|            | 7.5                     | 104.17                      | 2.20                         | 1.80          | 1.50                          |
|            | 19.5                    | 270.83                      | 5.60                         | 4.70          | 3.90                          |
|            | 61.5                    | 854.17                      | 18.0                         | 15.0          | 12.0                          |
|            | 181.5                   | 2520.83                     | 56.0                         | 47.0          | 39.0                          |
|            | 601.5                   | 8354.17                     | 100.00                       | 100.0         | 100.0                         |

1. Data based on characterization results, not tested in production.

2. All fast channels, expect channels on PA2, PA6, PB1, PB12.

3. Channels available on PA2, PA6, PB1 and PB12.

**Table 66. ADC accuracy - limited test conditions 100-pin packages<sup>(1)(2)</sup>**

| Symbol | Parameter                            | Conditions   |                     | Min<br>(3) | Typ  | Max<br>(3) | Unit |
|--------|--------------------------------------|--------------|---------------------|------------|------|------------|------|
| ET     | Total unadjusted error               | Single ended | Fast channel 5.1 Ms | -          | ±3.5 | ±4.5       | LSB  |
|        |                                      |              | Slow channel 4.8 Ms | -          | ±4   | ±4.5       |      |
|        |                                      | Differential | Fast channel 5.1 Ms | -          | ±3   | ±3         |      |
|        |                                      |              | Slow channel 4.8 Ms | -          | ±3   | ±3         |      |
| EO     | Offset error                         | Single ended | Fast channel 5.1 Ms | -          | ±1   | ±1.5       |      |
|        |                                      |              | Slow channel 4.8 Ms | -          | ±1   | ±2.5       |      |
|        |                                      | Differential | Fast channel 5.1 Ms | -          | ±1   | ±1.5       |      |
|        |                                      |              | Slow channel 4.8 Ms | -          | ±1   | ±1.5       |      |
| EG     | Gain error                           | Single ended | Fast channel 5.1 Ms | -          | ±3   | ±4         |      |
|        |                                      |              | Slow channel 4.8 Ms | -          | ±3.5 | ±4         |      |
|        |                                      | Differential | Fast channel 5.1 Ms | -          | ±1.5 | ±2.5       |      |
|        |                                      |              | Slow channel 4.8 Ms | -          | ±2   | ±2.5       |      |
| ED     | Differential linearity error         | Single ended | Fast channel 5.1 Ms | -          | ±1   | ±1.5       |      |
|        |                                      |              | Slow channel 4.8 Ms | -          | ±1   | ±1.5       |      |
|        |                                      | Differential | Fast channel 5.1 Ms | -          | ±1   | ±1         |      |
|        |                                      |              | Slow channel 4.8 Ms | -          | ±1   | ±1         |      |
| EL     | Integral linearity error             | Single ended | Fast channel 5.1 Ms | -          | ±1.5 | ±2         |      |
|        |                                      |              | Slow channel 4.8 Ms | -          | ±1.5 | ±3         |      |
|        |                                      | Differential | Fast channel 5.1 Ms | -          | ±1   | ±1.5       |      |
|        |                                      |              | Slow channel 4.8 Ms | -          | ±1   | ±1.5       |      |
| ENOB   | Effective number of bits             | Single ended | Fast channel 5.1 Ms | 10.7       | 10.8 | -          | bits |
|        |                                      |              | Slow channel 4.8 Ms | 10.7       | 10.8 | -          |      |
|        |                                      | Differential | Fast channel 5.1 Ms | 11.2       | 11.3 | -          |      |
|        |                                      |              | Slow channel 4.8 Ms | 11.1       | 11.3 | -          |      |
| SINAD  | Signal-to-noise and distortion ratio | Single ended | Fast channel 5.1 Ms | 66         | 67   | -          | dB   |
|        |                                      |              | Slow channel 4.8 Ms | 66         | 67   | -          |      |
|        |                                      | Differential | Fast channel 5.1 Ms | 69         | 70   | -          |      |
|        |                                      |              | Slow channel 4.8 Ms | 69         | 70   | -          |      |

Table 66. ADC accuracy - limited test conditions 100-pin packages<sup>(1)(2)</sup> (continued)

| Symbol | Parameter                 | Conditions                                                                                                              |              |                     | Min<br>(3) | Typ | Max<br>(3) | Unit |
|--------|---------------------------|-------------------------------------------------------------------------------------------------------------------------|--------------|---------------------|------------|-----|------------|------|
| SNR    | Signal-to-noise ratio     | ADC clock freq. $\leq$ 72 MHz<br>Sampling freq $\leq$ 5 Msps<br>$V_{DDA} = V_{REF+} = 3.3$ V<br>25°C<br>100-pin package | Single ended | Fast channel 5.1 Ms | 66         | 67  | -          | dB   |
|        |                           |                                                                                                                         |              | Slow channel 4.8 Ms | 66         | 67  | -          |      |
|        |                           |                                                                                                                         | Differential | Fast channel 5.1 Ms | 69         | 70  | -          |      |
|        |                           |                                                                                                                         |              | Slow channel 4.8 Ms | 69         | 70  | -          |      |
| THD    | Total harmonic distortion |                                                                                                                         | Single ended | Fast channel 5.1 Ms | -          | -76 | -76        |      |
|        |                           |                                                                                                                         |              | Slow channel 4.8 Ms | -          | -76 | -76        |      |
|        |                           |                                                                                                                         | Differential | Fast channel 5.1 Ms | -          | -80 | -80        |      |
|        |                           |                                                                                                                         |              | Slow channel 4.8 Ms | -          | -80 | -80        |      |

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.  
Any positive injection current within the limits specified for  $I_{INJ(PIN)}$  and  $\Sigma I_{INJ(PIN)}$  in [Section 6.3.13](#) does not affect the ADC accuracy.
3. Data based on characterization results, not tested in production.

Table 67. ADC accuracy, 100-pin packages<sup>(1)(2)(3)</sup>

| Symbol | Parameter                    | Conditions                                                                                                                     |                     |                     | Min <sup>(4)</sup> | Max <sup>(4)</sup> | Unit |
|--------|------------------------------|--------------------------------------------------------------------------------------------------------------------------------|---------------------|---------------------|--------------------|--------------------|------|
| ET     | Total unadjusted error       | ADC clock freq. ≤ 72 MHz,<br>Sampling freq. ≤ 5 Msps<br>1.8V ≤ V <sub>DDA</sub> , V <sub>REF+</sub> ≤ 3.6 V<br>100-pin package | Single Ended        | Fast channel 5.1 Ms | -                  | ±6.5               | LSB  |
|        |                              |                                                                                                                                |                     | Slow channel 4.8 Ms | -                  | ±6.5               |      |
|        |                              |                                                                                                                                | Differential        | Fast channel 5.1 Ms | -                  | ±4                 |      |
|        |                              |                                                                                                                                |                     | Slow channel 4.8 Ms | -                  | ±4                 |      |
| EO     | Offset error                 |                                                                                                                                | Single Ended        | Fast channel 5.1 Ms | -                  | ±3                 |      |
|        |                              |                                                                                                                                |                     | Slow channel 4.8 Ms | -                  | ±3                 |      |
|        |                              |                                                                                                                                | Differential        | Fast channel 5.1 Ms | -                  | ±2                 |      |
|        |                              |                                                                                                                                |                     | Slow channel 4.8 Ms | -                  | ±2                 |      |
| EG     | Gain error                   |                                                                                                                                | Single Ended        | Fast channel 5.1 Ms | -                  | ±6                 |      |
|        |                              |                                                                                                                                |                     | Slow channel 4.8 Ms | -                  | ±6                 |      |
|        |                              |                                                                                                                                | Differential        | Fast channel 5.1 Ms | -                  | ±3                 |      |
|        |                              |                                                                                                                                |                     | Slow channel 4.8 Ms | -                  | ±3                 |      |
| ED     | Differential linearity error | Single Ended                                                                                                                   | Fast channel 5.1 Ms | -                   | ±1.5               |                    |      |
|        |                              |                                                                                                                                | Slow channel 4.8 Ms | -                   | ±1.5               |                    |      |
|        |                              | Differential                                                                                                                   | Fast channel 5.1 Ms | -                   | ±1.5               |                    |      |
|        |                              |                                                                                                                                | Slow channel 4.8 Ms | -                   | ±1.5               |                    |      |
| EL     | Integral linearity error     | Single Ended                                                                                                                   | Fast channel 5.1 Ms | -                   | ±2                 |                    |      |
|        |                              |                                                                                                                                | Slow channel 4.8 Ms | -                   | ±3                 |                    |      |
|        |                              | Differential                                                                                                                   | Fast channel 5.1 Ms | -                   | ±2                 |                    |      |
|        |                              |                                                                                                                                | Slow channel 4.8 Ms | -                   | ±2                 |                    |      |
| ENOB   | Effective number of bits     | Single Ended                                                                                                                   | Fast channel 5.1 Ms | 10.4                | -                  | bits               |      |
|        |                              |                                                                                                                                | Slow channel 4.8 Ms | 10.2                | -                  |                    |      |
|        |                              | Differential                                                                                                                   | Fast channel 5.1 Ms | 10.8                | -                  |                    |      |
|        |                              |                                                                                                                                | Slow channel 4.8 Ms | 10.8                | -                  |                    |      |

Table 67. ADC accuracy, 100-pin packages<sup>(1)(2)(3)</sup> (continued)

| Symbol | Parameter                            | Conditions                                                                                                                      |                     |                     | Min <sup>(4)</sup> | Max <sup>(4)</sup> | Unit |
|--------|--------------------------------------|---------------------------------------------------------------------------------------------------------------------------------|---------------------|---------------------|--------------------|--------------------|------|
| SINAD  | Signal-to-noise and distortion ratio | ADC clock freq. ≤ 72 MHz,<br>Sampling freq. ≤ 5 Msps,<br>1.8V ≤ V <sub>DDA</sub> , V <sub>REF+</sub> ≤ 3.6 V<br>100-pin package | Single Ended        | Fast channel 5.1 Ms | -                  | 64                 | dB   |
|        |                                      |                                                                                                                                 |                     | Slow channel 4.8 Ms | -                  | 63                 |      |
|        |                                      |                                                                                                                                 | Differential        | Fast channel 5.1 Ms | -                  | 67                 |      |
|        |                                      |                                                                                                                                 |                     | Slow channel 4.8 Ms | -                  | 67                 |      |
| SNR    | Signal-to-noise ratio                |                                                                                                                                 | Single Ended        | Fast channel 5.1 Ms | 64                 | -                  |      |
|        |                                      |                                                                                                                                 |                     | Slow channel 4.8 Ms | 64                 | -                  |      |
|        |                                      |                                                                                                                                 | Differential        | Fast channel 5.1 Ms | 67                 | -                  |      |
|        |                                      |                                                                                                                                 |                     | Slow channel 4.8 Ms | 67                 | -                  |      |
| THD    | Total harmonic distortion            | Single Ended                                                                                                                    | Fast channel 5.1 Ms | -                   | -74                |                    |      |
|        |                                      |                                                                                                                                 | Slow channel 4.8 Ms | -                   | -74                |                    |      |
|        |                                      | Differential                                                                                                                    | Fast channel 5.1 Ms | -                   | -78                |                    |      |
|        |                                      |                                                                                                                                 | Slow channel 4.8 Ms | -                   | -76                |                    |      |

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current. Any positive injection current within the limits specified for  $I_{\text{INJ(PIN)}}$  and  $\Sigma I_{\text{INJ(PIN)}}$  in [Section 6.3.13](#) does not affect the ADC accuracy.
3. Better performance may be achieved in restricted  $V_{\text{DDA}}$ , frequency and temperature ranges.
4. Data based on characterization results, not tested in production.

Table 68. ADC accuracy - limited test conditions 64-pin packages<sup>(1)(2)</sup>

| Symbol               | Parameter                            | Conditions                                                                                                                  |                     |                     | Min<br>(3) | Typ  | Max<br>(3) | Unit |
|----------------------|--------------------------------------|-----------------------------------------------------------------------------------------------------------------------------|---------------------|---------------------|------------|------|------------|------|
| ET                   | Total unadjusted error               | ADC clock freq. ≤72 MHz<br>Sampling freq. ≤5 Msps<br>V <sub>DDA</sub> = V <sub>REF+</sub> = 3.3 V<br>25°C<br>64-pin package | Single ended        | Fast channel 5.1 Ms | -          | ±4.0 | ±4.5       | LSB  |
|                      |                                      |                                                                                                                             |                     | Slow channel 4.8 Ms | -          | ±5.5 | ±6.0       |      |
| Differential         |                                      |                                                                                                                             | Fast channel 5.1 Ms | -                   | ±3.5       | ±4.0 |            |      |
|                      |                                      |                                                                                                                             | Slow channel 4.8 Ms | -                   | ±3.5       | ±4.0 |            |      |
| EO                   | Offset error                         |                                                                                                                             | Single ended        | Fast channel 5.1 Ms | -          | ±2.0 | ±2.0       |      |
|                      |                                      |                                                                                                                             |                     | Slow channel 4.8 Ms | -          | ±1.5 | ±2.0       |      |
|                      |                                      |                                                                                                                             | Differential        | Fast channel 5.1 Ms | -          | ±1.5 | ±2.0       |      |
|                      |                                      |                                                                                                                             |                     | Slow channel 4.8 Ms | -          | ±1.5 | ±2.0       |      |
| EG                   | Gain error                           |                                                                                                                             | Single ended        | Fast channel 5.1 Ms | -          | ±3.0 | ±4.0       |      |
|                      |                                      |                                                                                                                             |                     | Slow channel 4.8 Ms | -          | ±5.0 | ±5.5       |      |
|                      |                                      |                                                                                                                             | Differential        | Fast channel 5.1 Ms | -          | ±3.0 | ±3.0       |      |
|                      |                                      |                                                                                                                             |                     | Slow channel 4.8 Ms | -          | ±3.0 | ±3.0       |      |
| ED                   | Differential linearity error         | Single ended                                                                                                                | Fast channel 5.1 Ms | -                   | ±1.0       | ±1.0 |            |      |
|                      |                                      |                                                                                                                             | Slow channel 4.8 Ms | -                   | ±1.0       | ±1.0 |            |      |
|                      |                                      | Differential                                                                                                                | Fast channel 5.1 Ms | -                   | ±1.0       | ±1.0 |            |      |
|                      |                                      |                                                                                                                             | Slow channel 4.8 Ms | -                   | ±1.0       | ±1.0 |            |      |
| EL                   | Integral linearity error             | Single ended                                                                                                                | Fast channel 5.1 Ms | -                   | ±1.5       | ±2.0 |            |      |
|                      |                                      |                                                                                                                             | Slow channel 4.8 Ms | -                   | ±2.0       | ±3.0 |            |      |
|                      |                                      | Differential                                                                                                                | Fast channel 5.1 Ms | -                   | ±1.5       | ±1.5 |            |      |
|                      |                                      |                                                                                                                             | Slow channel 4.8 Ms | -                   | ±1.5       | ±2.0 |            |      |
| ENOB <sup>(4)</sup>  | Effective number of bits             | Single ended                                                                                                                | Fast channel 5.1 Ms | 10.8                | 10.8       | -    | bits       |      |
|                      |                                      |                                                                                                                             | Slow channel 4.8 Ms | 10.8                | 10.8       | -    |            |      |
|                      |                                      | Differential                                                                                                                | Fast channel 5.1 Ms | 11.2                | 11.3       | -    |            |      |
|                      |                                      |                                                                                                                             | Slow channel 4.8 Ms | 11.2                | 11.3       | -    |            |      |
| SINAD <sup>(4)</sup> | Signal-to-noise and distortion ratio | Single ended                                                                                                                | Fast channel 5.1 Ms | 66                  | 67         | -    | dB         |      |
|                      |                                      |                                                                                                                             | Slow channel 4.8 Ms | 66                  | 67         | -    |            |      |
|                      |                                      | Differential                                                                                                                | Fast channel 5.1 Ms | 69                  | 70         | -    |            |      |
|                      |                                      |                                                                                                                             | Slow channel 4.8 Ms | 69                  | 70         | -    |            |      |

Table 68. ADC accuracy - limited test conditions 64-pin packages<sup>(1)(2)</sup> (continued)

| Symbol             | Parameter                 | Conditions                                                                                                                    |              |                     | Min<br>(3) | Typ | Max<br>(3) | Unit |
|--------------------|---------------------------|-------------------------------------------------------------------------------------------------------------------------------|--------------|---------------------|------------|-----|------------|------|
| SNR <sup>(4)</sup> | Signal-to-noise ratio     | ADC clock freq. ≤ 72 MHz<br>Sampling freq ≤ 5 Msps<br>V <sub>DDA</sub> = V <sub>REF+</sub> = 3.3 V<br>25°C<br>100-pin package | Single ended | Fast channel 5.1 Ms | 66         | 67  | -          | dB   |
|                    |                           |                                                                                                                               |              | Slow channel 4.8 Ms | 66         | 67  | -          |      |
|                    |                           |                                                                                                                               | Differential | Fast channel 5.1 Ms | 69         | 70  | -          |      |
|                    |                           |                                                                                                                               |              | Slow channel 4.8 Ms | 69         | 70  | -          |      |
| THD <sup>(4)</sup> | Total harmonic distortion |                                                                                                                               | Single ended | Fast channel 5.1 Ms | -          | -80 | -80        |      |
|                    |                           |                                                                                                                               |              | Slow channel 4.8 Ms | -          | -78 | -77        |      |
|                    |                           |                                                                                                                               | Differential | Fast channel 5.1 Ms | -          | -83 | -82        |      |
|                    |                           |                                                                                                                               |              | Slow channel 4.8 Ms | -          | -81 | -80        |      |

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current. Any positive injection current within the limits specified for  $I_{INJ(PIN)}$  and  $\Sigma I_{INJ(PIN)}$  in [Section 6.3.13](#) does not affect the ADC accuracy.
3. Data based on characterization results, not tested in production.
4. Value measured with a -0.5dB Full Scale 50kHz sine wave input signal.

Table 69. ADC accuracy, 64-pin packages<sup>(1)(2)(3)</sup>

| Symbol | Parameter                    | Conditions                                                                                                                    |                     |                     | Min <sup>(4)</sup> | Max <sup>(4)</sup> | Unit |
|--------|------------------------------|-------------------------------------------------------------------------------------------------------------------------------|---------------------|---------------------|--------------------|--------------------|------|
| ET     | Total unadjusted error       | ADC clock freq. ≤ 72 MHz,<br>Sampling freq. ≤ 5 Msps<br>1.8V ≤ V <sub>DDA</sub> , V <sub>REF+</sub> ≤ 3.6 V<br>64-pin package | Single Ended        | Fast channel 5.1 Ms | -                  | ±6.5               | LSB  |
|        |                              |                                                                                                                               |                     | Slow channel 4.8 Ms | -                  | ±6.5               |      |
|        |                              |                                                                                                                               | Differential        | Fast channel 5.1 Ms | -                  | ±4                 |      |
|        |                              |                                                                                                                               |                     | Slow channel 4.8 Ms | -                  | ±4.5               |      |
| EO     | Offset error                 |                                                                                                                               | Single Ended        | Fast channel 5.1 Ms | -                  | ±3                 |      |
|        |                              |                                                                                                                               |                     | Slow channel 4.8 Ms | -                  | ±3                 |      |
|        |                              |                                                                                                                               | Differential        | Fast channel 5.1 Ms | -                  | ±2.5               |      |
|        |                              |                                                                                                                               |                     | Slow channel 4.8 Ms | -                  | ±2.5               |      |
| EG     | Gain error                   |                                                                                                                               | Single Ended        | Fast channel 5.1 Ms | -                  | ±6                 |      |
|        |                              |                                                                                                                               |                     | Slow channel 4.8 Ms | -                  | ±6                 |      |
|        |                              |                                                                                                                               | Differential        | Fast channel 5.1 Ms | -                  | ±3.5               |      |
|        |                              |                                                                                                                               |                     | Slow channel 4.8 Ms | -                  | ±4                 |      |
| ED     | Differential linearity error | Single Ended                                                                                                                  | Fast channel 5.1 Ms | -                   | ±1.5               |                    |      |
|        |                              |                                                                                                                               | Slow channel 4.8 Ms | -                   | ±1.5               |                    |      |
|        |                              | Differential                                                                                                                  | Fast channel 5.1 Ms | -                   | ±1.5               |                    |      |
|        |                              |                                                                                                                               | Slow channel 4.8 Ms | -                   | ±1.5               |                    |      |
| EL     | Integral linearity error     | Single Ended                                                                                                                  | Fast channel 5.1 Ms | -                   | ±3                 |                    |      |
|        |                              |                                                                                                                               | Slow channel 4.8 Ms | -                   | ±3.5               |                    |      |
|        |                              | Differential                                                                                                                  | Fast channel 5.1 Ms | -                   | ±2                 |                    |      |
|        |                              |                                                                                                                               | Slow channel 4.8 Ms | -                   | ±2.5               |                    |      |
| ENOB   | Effective number of bits     | Single Ended                                                                                                                  | Fast channel 5.1 Ms | 10.4                | -                  | bits               |      |
|        |                              |                                                                                                                               | Slow channel 4.8 Ms | 10.4                | -                  |                    |      |
|        |                              | Differential                                                                                                                  | Fast channel 5.1 Ms | 10.8                | -                  |                    |      |
|        |                              |                                                                                                                               | Slow channel 4.8 Ms | 10.8                | -                  |                    |      |

Table 69. ADC accuracy, 64-pin packages<sup>(1)(2)(3)</sup> (continued)

| Symbol | Parameter                            | Conditions                                                                                                                     |                     |                     | Min <sup>(4)</sup> | Max <sup>(4)</sup> | Unit |
|--------|--------------------------------------|--------------------------------------------------------------------------------------------------------------------------------|---------------------|---------------------|--------------------|--------------------|------|
| SINAD  | Signal-to-noise and distortion ratio | ADC clock freq. ≤ 72 MHz,<br>Sampling freq. ≤ 5 Msps,<br>1.8V ≤ V <sub>DDA</sub> , V <sub>REF+</sub> ≤ 3.6 V<br>64-pin package | Single Ended        | Fast channel 5.1 Ms | 64                 | -                  | dB   |
|        |                                      |                                                                                                                                |                     | Slow channel 4.8 Ms | 63                 | -                  |      |
|        |                                      |                                                                                                                                | Differential        | Fast channel 5.1 Ms | 67                 | -                  |      |
|        |                                      |                                                                                                                                |                     | Slow channel 4.8 Ms | 67                 | -                  |      |
| SNR    | Signal-to-noise ratio                |                                                                                                                                | Single Ended        | Fast channel 5.1 Ms | 64                 | -                  |      |
|        |                                      |                                                                                                                                |                     | Slow channel 4.8 Ms | 64                 | -                  |      |
|        |                                      |                                                                                                                                | Differential        | Fast channel 5.1 Ms | 67                 | -                  |      |
|        |                                      |                                                                                                                                |                     | Slow channel 4.8 Ms | 67                 | -                  |      |
| THD    | Total harmonic distortion            | Single Ended                                                                                                                   | Fast channel 5.1 Ms | -                   | -75                |                    |      |
|        |                                      |                                                                                                                                | Slow channel 4.8 Ms | -                   | -75                |                    |      |
|        |                                      | Differential                                                                                                                   | Fast channel 5.1 Ms | -                   | -79                |                    |      |
|        |                                      |                                                                                                                                | Slow channel 4.8 Ms | -                   | -78                |                    |      |

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current. Any positive injection current within the limits specified for  $I_{INJ(PIN)}$  and  $\Sigma I_{INJ(PIN)}$  in [Section 6.3.13](#) does not affect the ADC accuracy.
3. Better performance may be achieved in restricted  $V_{DDA}$ , frequency and temperature ranges.
4. Data based on characterization results, not tested in production.

Table 70. ADC accuracy at 1MSPS<sup>(1)(2)</sup>

| Symbol | Parameter                    | Conditions                                                                                                                       |              | Typ  | Max <sup>(3)</sup> | Unit |
|--------|------------------------------|----------------------------------------------------------------------------------------------------------------------------------|--------------|------|--------------------|------|
| ET     | Total unadjusted error       | ADC clock freq. ≤ 72 MHz,<br>Sampling freq. ≤ 1 Msps<br>2.4V ≤ V <sub>DDA</sub> , V <sub>REF+</sub> ≤ 3.6 V<br>single-ended mode | Fast channel | ±2.5 | ±5                 | LSB  |
|        |                              |                                                                                                                                  | Slow channel | ±3.5 | ±5                 |      |
| EO     | Offset error                 |                                                                                                                                  | Fast channel | ±1   | ±2.5               |      |
|        |                              |                                                                                                                                  | Slow channel | ±1.5 | ±2.5               |      |
| EG     | Gain error                   |                                                                                                                                  | Fast channel | ±2   | ±3                 |      |
|        |                              |                                                                                                                                  | Slow channel | ±3   | ±4                 |      |
| ED     | Differential linearity error |                                                                                                                                  | Fast channel | ±0.7 | ±2                 |      |
|        |                              |                                                                                                                                  | Slow channel | ±0.7 | ±2                 |      |
| EL     | Integral linearity error     |                                                                                                                                  | Fast channel | ±1   | ±3                 |      |
|        |                              |                                                                                                                                  | Slow channel | ±1.2 | ±3                 |      |

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current. Any positive injection current within the limits specified for  $I_{INJ(PIN)}$  and  $\Sigma I_{INJ(PIN)}$  in [Section 6.3.13](#) does not affect the ADC accuracy.
3. Data based on characterization results, not tested in production.

Figure 30. ADC accuracy characteristics

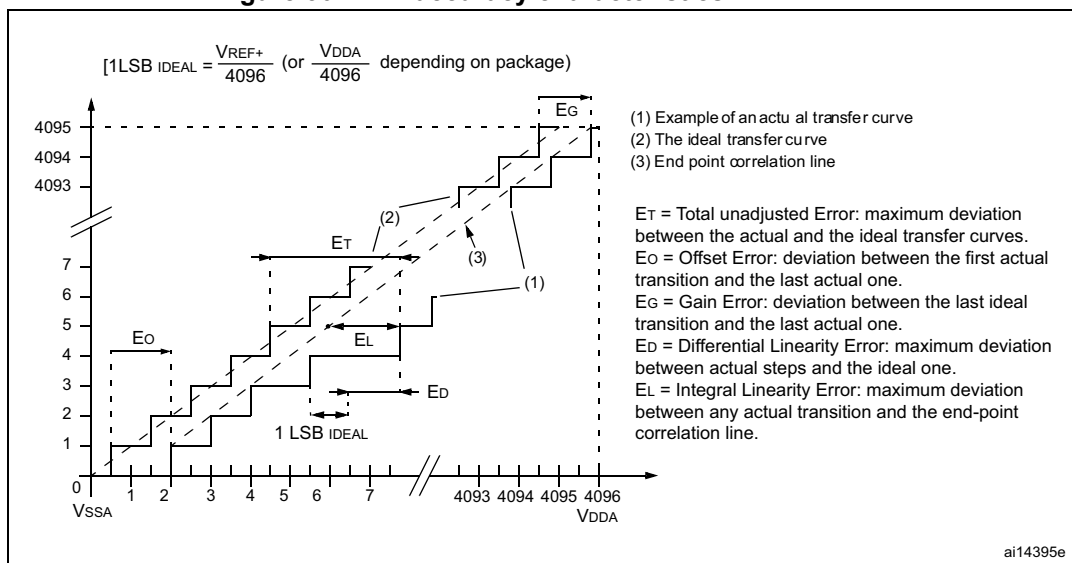
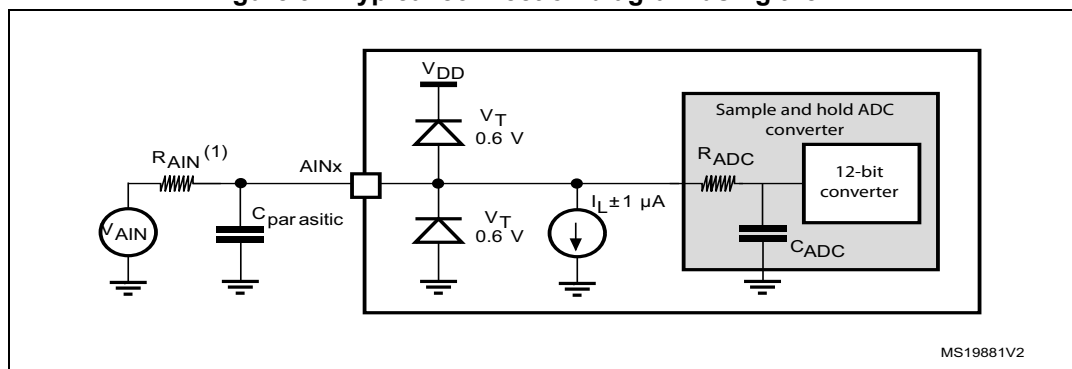


Figure 31. Typical connection diagram using the ADC



1. Refer to [Table 64](#) for the values of  $R_{\text{AIN}}$ .
2.  $C_{\text{parasitic}}$  represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high  $C_{\text{parasitic}}$  value will downgrade conversion accuracy. To remedy this,  $f_{\text{ADC}}$  should be reduced.

### General PCB design guidelines

Power supply decoupling should be performed as shown in [Figure 10](#). The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

## 6.3.19 DAC electrical specifications

Table 71. DAC characteristics

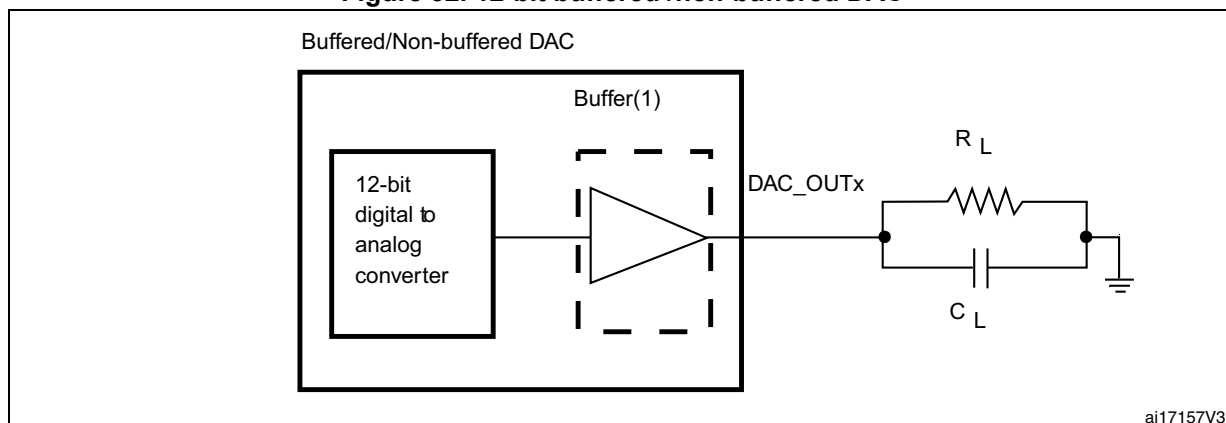
| Symbol                                | Parameter                                                                                                                                         | Min | Typ | Max                     | Unit       | Comments                                                                                                                                                                      |
|---------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-------------------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $V_{DDA}$                             | Analog supply voltage for DAC ON                                                                                                                  | 2.4 | -   | 3.6                     | V          | -                                                                                                                                                                             |
| $R_{LOAD}^{(1)}$                      | Resistive load with buffer ON                                                                                                                     | 5   | -   | -                       | k $\Omega$ | -                                                                                                                                                                             |
| $R_O^{(1)}$                           | Impedance output with buffer OFF                                                                                                                  | -   | -   | 15                      | k $\Omega$ | When the buffer is OFF, the Minimum resistive load between DAC_OUT and $V_{SS}$ to have a 1% accuracy is 1.5 M $\Omega$                                                       |
| $C_{LOAD}^{(1)}$                      | Capacitive load                                                                                                                                   | -   | -   | 50                      | pF         | Maximum capacitive load at DAC_OUT pin (when the buffer is ON).                                                                                                               |
| DAC_OUT <sub>min</sub> <sup>(1)</sup> | Lower DAC_OUT voltage with buffer ON                                                                                                              | 0.2 | -   | -                       | V          | It gives the maximum output excursion of the DAC.<br>It corresponds to 12-bit input code (0x0E0) to (0xF1C) at $V_{DDA} = 3.6$ V and (0x155) and (0xEAB) at $V_{DDA} = 2.4$ V |
| DAC_OUT <sub>max</sub> <sup>(1)</sup> | Higher DAC_OUT voltage with buffer ON                                                                                                             | -   | -   | $V_{DDA} - 0.2$         | V          |                                                                                                                                                                               |
| DAC_OUT <sub>min</sub> <sup>(1)</sup> | Lower DAC_OUT voltage with buffer OFF                                                                                                             | -   | 0.5 | -                       | mV         | It gives the maximum output excursion of the DAC.                                                                                                                             |
| DAC_OUT <sub>max</sub> <sup>(1)</sup> | Higher DAC_OUT voltage with buffer OFF                                                                                                            | -   | -   | $V_{DDA} - 1\text{LSB}$ | V          |                                                                                                                                                                               |
| $I_{DDA}^{(3)}$                       | DAC DC current consumption in quiescent mode <sup>(2)</sup>                                                                                       | -   | -   | 380                     | $\mu$ A    | With no load, middle code (0x800) on the input                                                                                                                                |
|                                       |                                                                                                                                                   | -   | -   | 480                     | $\mu$ A    | With no load, worst code (0xF1C) on the input                                                                                                                                 |
| DNL <sup>(3)</sup>                    | Differential non linearity<br>Difference between two consecutive code-1LSB)                                                                       | -   | -   | $\pm 0.5$               | LSB        | Given for a 10-bit input code                                                                                                                                                 |
|                                       |                                                                                                                                                   | -   | -   | $\pm 2$                 | LSB        | Given for a 12-bit input code                                                                                                                                                 |
| INL <sup>(3)</sup>                    | Integral non linearity<br>(difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023) | -   | -   | $\pm 1$                 | LSB        | Given for a 10-bit input code                                                                                                                                                 |
|                                       |                                                                                                                                                   | -   | -   | $\pm 4$                 | LSB        | Given for a 12-bit input code                                                                                                                                                 |
| Offset <sup>(3)</sup>                 | Offset error<br>(difference between measured value at Code (0x800) and the ideal value = $V_{DDA}/2$ )                                            | -   | -   | $\pm 10$                | mV         | -                                                                                                                                                                             |
|                                       |                                                                                                                                                   | -   | -   | $\pm 3$                 | LSB        | Given for a 10-bit input code at $V_{DDA} = 3.6$ V                                                                                                                            |
|                                       |                                                                                                                                                   | -   | -   | $\pm 12$                | LSB        | Given for a 12-bit input code at $V_{DDA} = 3.6$ V                                                                                                                            |
| Gain error <sup>(3)</sup>             | Gain error                                                                                                                                        | -   | -   | $\pm 0.5$               | %          | Given for a 12-bit input code                                                                                                                                                 |

Table 71. DAC characteristics (continued)

| Symbol                      | Parameter                                                                                                                                                         | Min | Typ | Max | Unit          | Comments                                                                                                                              |
|-----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|---------------|---------------------------------------------------------------------------------------------------------------------------------------|
| $t_{\text{SETTLING}}^{(3)}$ | Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value $\pm 1\text{LSB}$ ) | -   | 3   | 4   | $\mu\text{s}$ | $C_{\text{LOAD}} \leq 50\text{ pF}$ , $R_{\text{LOAD}} \geq 5\text{ k}\Omega$                                                         |
| Update rate <sup>(3)</sup>  | Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)                                                         | -   | -   | 1   | MS/s          | $C_{\text{LOAD}} \leq 50\text{ pF}$ , $R_{\text{LOAD}} \geq 5\text{ k}\Omega$                                                         |
| $t_{\text{WAKEUP}}^{(3)}$   | Wakeup time from off state (Setting the ENx bit in the DAC Control register)                                                                                      | -   | 6.5 | 10  | $\mu\text{s}$ | $C_{\text{LOAD}} \leq 50\text{ pF}$ , $R_{\text{LOAD}} \geq 5\text{ k}\Omega$<br>input code between lowest and highest possible ones. |
| PSRR+ <sup>(1)</sup>        | Power supply rejection ratio (to $V_{\text{DDA}}$ ) (static DC measurement)                                                                                       | -   | -67 | -40 | dB            | No $R_{\text{LOAD}}$ , $C_{\text{LOAD}} = 50\text{ pF}$                                                                               |

1. Guaranteed by design, not tested in production.
2. Quiescent mode refers to the state of the DAC a keeping steady value on the output, so no dynamic consumption is involved.
3. Data based on characterization results, not tested in production.

Figure 32. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC\_CR register.

## 6.3.20 Comparator characteristics

Table 72. Comparator characteristics<sup>(1)</sup>

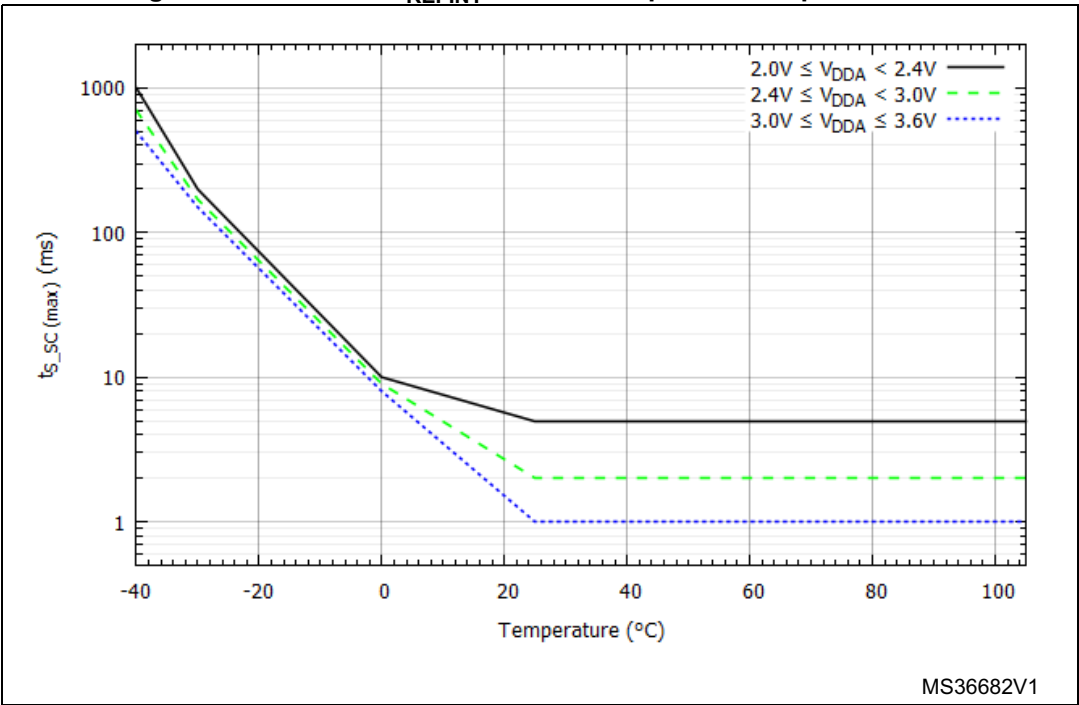
| Symbol           | Parameter                                                   | Conditions                                                 | Min                  | Typ     | Max              | Unit                  |
|------------------|-------------------------------------------------------------|------------------------------------------------------------|----------------------|---------|------------------|-----------------------|
| $V_{DDA}$        | Analog supply voltage                                       | $V_{REFINT}$ scaler not in use                             | 1.65                 | -       | 3.6              | V                     |
|                  |                                                             | $V_{REFINT}$ scaler in use                                 | 2                    | -       | 3.6              |                       |
| $V_{IN}$         | Comparator input voltage range                              | -                                                          | 0                    | -       | $V_{DDA}$        |                       |
| $V_{BG}$         | Scaler input voltage                                        | -                                                          | -                    | 1.2     | -                |                       |
| $V_{SC}$         | Scaler offset voltage                                       | -                                                          | -                    | $\pm 5$ | $\pm 10$         | mV                    |
| $t_{S\_SC}$      | $V_{REFINT}$ scaler startup time from power down            | First $V_{REFINT}$ scaler activation after device power on | -                    | -       | 1 <sup>(2)</sup> | s                     |
|                  |                                                             | Next activations                                           | -                    | -       | 0.2              | ms                    |
| $t_{START}$      | Comparator startup time                                     | Startup time to reach propagation delay specification      | -                    | -       | 60               | $\mu$ s               |
| $t_D$            | Propagation delay for 200 mV step with 100 mV overdrive     | Ultra-low-power mode                                       | -                    | 2       | 4.5              | $\mu$ s               |
|                  |                                                             | Low-power mode                                             | -                    | 0.7     | 1.5              |                       |
|                  |                                                             | Medium power mode                                          | -                    | 0.3     | 0.6              |                       |
|                  |                                                             | High speed mode                                            | $V_{DDA} \geq 2.7$ V |         | -                | ns                    |
|                  |                                                             |                                                            | $V_{DDA} < 2.7$ V    |         | -                |                       |
|                  | Propagation delay for full range step with 100 mV overdrive | Ultra-low-power mode                                       | -                    | 2       | 7                | $\mu$ s               |
|                  |                                                             | Low-power mode                                             | -                    | 0.7     | 2.1              |                       |
|                  |                                                             | Medium power mode                                          | -                    | 0.3     | 1.2              |                       |
|                  |                                                             | High speed mode                                            | $V_{DDA} \geq 2.7$ V |         | -                | ns                    |
|                  |                                                             |                                                            | $V_{DDA} < 2.7$ V    |         | -                |                       |
| $V_{offset}$     | Comparator offset error                                     | -                                                          | -                    | $\pm 4$ | $\pm 10$         | mV                    |
| $dV_{offset}/dT$ | Offset error temperature coefficient                        | -                                                          | -                    | 18      | -                | $\mu$ V/ $^{\circ}$ C |
| $I_{DD(Comp)}$   | COMP current consumption                                    | Ultra-low-power mode                                       | -                    | 1.2     | 1.5              | $\mu$ A               |
|                  |                                                             | Low-power mode                                             | -                    | 3       | 5                |                       |
|                  |                                                             | Medium power mode                                          | -                    | 10      | 15               |                       |
|                  |                                                             | High speed mode                                            | -                    | 75      | 100              |                       |

Table 72. Comparator characteristics<sup>(1)</sup> (continued)

| Symbol    | Parameter             | Conditions                               | Min                   | Typ | Max | Unit |
|-----------|-----------------------|------------------------------------------|-----------------------|-----|-----|------|
| $V_{hys}$ | Comparator hysteresis | No hysteresis<br>(COMPxHYST[1:0]=00)     | -                     | 0   | -   | mV   |
|           |                       | Low hysteresis<br>(COMPxHYST[1:0]=01)    | High speed mode       | 8   | 13  |      |
|           |                       |                                          | All other power modes |     | 10  |      |
|           |                       | Medium hysteresis<br>(COMPxHYST[1:0]=10) | High speed mode       | 15  | 26  |      |
|           |                       |                                          | All other power modes |     | 19  |      |
|           |                       | High hysteresis<br>(COMPxHYST[1:0]=11)   | High speed mode       | 31  | 49  |      |
|           |                       |                                          | All other power modes |     | 40  |      |

1. Data based on characterization results, not tested in production.
2. For more details and conditions, see [Figure 33](#) Maximum  $V_{REFINT}$  scaler startup time from power down.

Figure 33. Maximum  $V_{REFINT}$  scaler startup time from power down



## 6.3.21 Operational amplifier characteristics

Table 73. Operational amplifier characteristics<sup>(1)</sup>

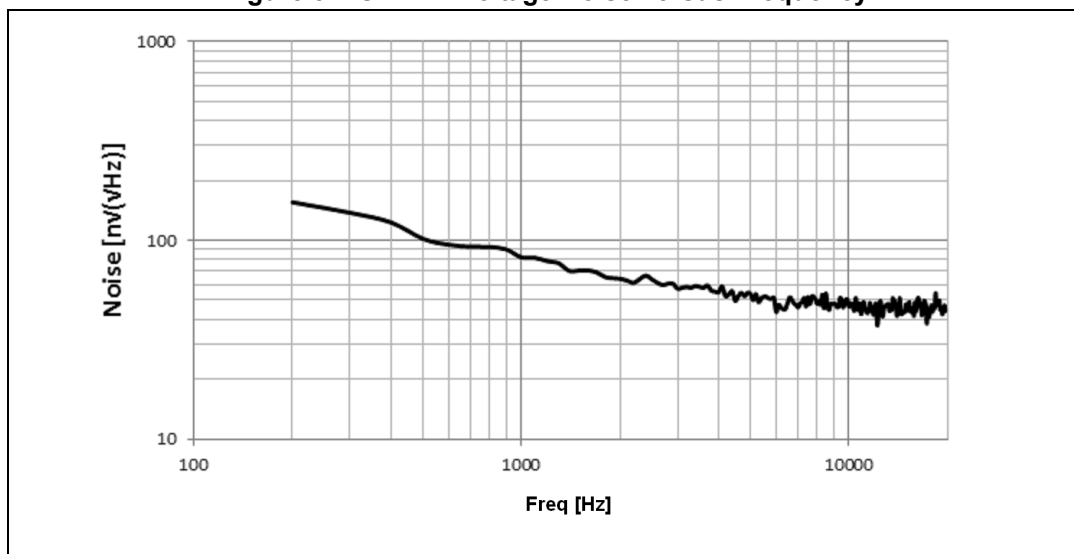
| Symbol                 | Parameter                                                                                         |                           | Condition                                                                  | Min | Typ | Max              | Unit  |
|------------------------|---------------------------------------------------------------------------------------------------|---------------------------|----------------------------------------------------------------------------|-----|-----|------------------|-------|
| V <sub>DDA</sub>       | Analog supply voltage                                                                             |                           | -                                                                          | 2.4 | -   | 3.6              | V     |
| CMIR                   | Common mode input range                                                                           |                           | -                                                                          | 0   | -   | V <sub>DDA</sub> | V     |
| V <sub>I</sub> OFFSET  | Input offset voltage                                                                              | Maximum calibration range | 25°C, No Load on output.                                                   | -   | -   | 4                | mV    |
|                        |                                                                                                   |                           | All voltage/Temp.                                                          | -   | -   | 6                |       |
|                        |                                                                                                   | After offset calibration  | 25°C, No Load on output.                                                   | -   | -   | 1.6              |       |
|                        |                                                                                                   |                           | All voltage/Temp.                                                          | -   | -   | 3                |       |
| ΔV <sub>I</sub> OFFSET | Input offset voltage drift                                                                        |                           | -                                                                          | -   | 5   | -                | μV/°C |
| I <sub>LOAD</sub>      | Drive current                                                                                     |                           | -                                                                          | -   | -   | 500              | μA    |
| IDDOPAMP               | Consumption                                                                                       |                           | No load, quiescent mode                                                    | -   | 690 | 1450             | μA    |
| CMRR                   | Common mode rejection ratio                                                                       |                           | -                                                                          | -   | 90  | -                | dB    |
| PSRR                   | Power supply rejection ratio                                                                      |                           | DC                                                                         | 73  | 117 | -                | dB    |
| GBW                    | Bandwidth                                                                                         |                           | -                                                                          | -   | 8.2 | -                | MHz   |
| SR                     | Slew rate                                                                                         |                           | -                                                                          | -   | 4.7 | -                | V/μs  |
| R <sub>LOAD</sub>      | Resistive load                                                                                    |                           | -                                                                          | 4   | -   | -                | kΩ    |
| C <sub>LOAD</sub>      | Capacitive load                                                                                   |                           | -                                                                          | -   | -   | 50               | pF    |
| V <sub>OH</sub> SAT    | High saturation voltage                                                                           |                           | R <sub>load</sub> = min, Input at V <sub>DDA</sub> .                       | -   | -   | 100              | mV    |
|                        |                                                                                                   |                           | R <sub>load</sub> = 20K, Input at V <sub>DDA</sub> .                       | -   | -   | 20               |       |
| V <sub>OL</sub> SAT    | Low saturation voltage                                                                            |                           | Rload = min, input at 0V                                                   | -   | -   | 100              |       |
|                        |                                                                                                   |                           | Rload = 20K, input at 0V.                                                  | -   | -   | 20               |       |
| φm                     | Phase margin                                                                                      |                           | -                                                                          | -   | 62  | -                | °     |
| t <sub>OFFTRIM</sub>   | Offset trim time: during calibration, minimum time needed between two steps to have 1 mV accuracy |                           | -                                                                          | -   | -   | 2                | ms    |
| t <sub>WAKEUP</sub>    | Wake up time from OFF state.                                                                      |                           | C <sub>LOAD</sub> ≤50 pf, R <sub>LOAD</sub> ≥ 4 kΩ, Follower configuration | -   | 2.8 | 5                | μs    |

Table 73. Operational amplifier characteristics<sup>(1)</sup> (continued)

| Symbol               | Parameter                                                   | Condition                                       | Min | Typ      | Max                 | Unit                   |
|----------------------|-------------------------------------------------------------|-------------------------------------------------|-----|----------|---------------------|------------------------|
| PGA gain             | Non inverting gain value                                    | -                                               | -   | 2        | -                   | -                      |
|                      |                                                             |                                                 | -   | 4        | -                   | -                      |
|                      |                                                             |                                                 | -   | 8        | -                   | -                      |
|                      |                                                             |                                                 | -   | 16       | -                   | -                      |
| R <sub>network</sub> | R2/R1 internal resistance values in PGA mode <sup>(2)</sup> | Gain=2                                          | -   | 5.4/5.4  | -                   | kΩ                     |
|                      |                                                             | Gain=4                                          | -   | 16.2/5.4 | -                   |                        |
|                      |                                                             | Gain=8                                          | -   | 37.8/5.4 | -                   |                        |
|                      |                                                             | Gain=16                                         | -   | 40.5/2.7 | -                   |                        |
| PGA gain error       | PGA gain error                                              | -                                               | -1% | -        | 1%                  |                        |
| I <sub>bias</sub>    | OPAMP input bias current                                    | -                                               | -   | -        | ±0.2 <sup>(3)</sup> | μA                     |
| PGA BW               | PGA bandwidth for different non inverting gain              | PGA Gain = 2,<br>Cload = 50pF,<br>Rload = 4 KΩ  | -   | 4        | -                   | MHz                    |
|                      |                                                             | PGA Gain = 4,<br>Cload = 50pF,<br>Rload = 4 KΩ  | -   | 2        | -                   |                        |
|                      |                                                             | PGA Gain = 8,<br>Cload = 50pF,<br>Rload = 4 KΩ  | -   | 1        | -                   |                        |
|                      |                                                             | PGA Gain = 16,<br>Cload = 50pF,<br>Rload = 4 KΩ | -   | 0.5      | -                   |                        |
| e <sub>n</sub>       | Voltage noise density                                       | @ 1KHz, Output loaded with 4 KΩ                 | -   | 109      | -                   | $\frac{nV}{\sqrt{Hz}}$ |
|                      |                                                             | @ 10KHz, Output loaded with 4 KΩ                | -   | 43       | -                   |                        |

1. Guaranteed by design, not tested in production.
2. R2 is the internal resistance between OPAMP output and OPAMP inverting input.  
R1 is the internal resistance between OPAMP inverting input and ground.  
The PGA gain = 1+R2/R1
3. Mostly TTa I/O leakage, when used in analog mode.

Figure 34. OPAMP Voltage Noise versus Frequency



### 6.3.22 Temperature sensor characteristics

Table 74. TS characteristics

| Symbol                   | Parameter                                      | Min  | Typ     | Max     | Unit  |
|--------------------------|------------------------------------------------|------|---------|---------|-------|
| $T_L^{(1)}$              | $V_{SENSE}$ linearity with temperature         | -    | $\pm 1$ | $\pm 2$ | °C    |
| Avg_Slope <sup>(1)</sup> | Average slope                                  | 4.0  | 4.3     | 4.6     | mV/°C |
| $V_{25}$                 | Voltage at 25 °C                               | 1.34 | 1.43    | 1.52    | V     |
| $t_{START}^{(1)}$        | Startup time                                   | 4    | -       | 10      | μs    |
| $T_{S\_temp}^{(1)(2)}$   | ADC sampling time when reading the temperature | 2.2  | -       | -       | μs    |

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

Table 75. Temperature sensor calibration values

| Calibration value name | Description                                                         | Memory address            |
|------------------------|---------------------------------------------------------------------|---------------------------|
| TS_CAL1                | TS ADC raw data acquired at temperature of 30 °C, $V_{DDA} = 3.3$ V | 0x1FFF F7B8 - 0x1FFF F7B9 |
| TS_CAL2                | TS ADC raw data acquired at temperature of 110 °C $V_{DDA} = 3.3$ V | 0x1FFF F7C2 - 0x1FFF F7C3 |

### 6.3.23 $V_{BAT}$ monitoring characteristics

Table 76.  $V_{BAT}$  monitoring characteristics

| Symbol                 | Parameter                                                    | Min | Typ | Max | Unit |
|------------------------|--------------------------------------------------------------|-----|-----|-----|------|
| R                      | Resistor bridge for $V_{BAT}$                                | -   | 50  | -   | KΩ   |
| Q                      | Ratio on $V_{BAT}$ measurement                               | -   | 2   | -   |      |
| $Er^{(1)}$             | Error on Q                                                   | -1  | -   | +1  | %    |
| $T_{S\_vbat}^{(1)(2)}$ | ADC sampling time when reading the $V_{BAT}$<br>1mV accuracy | 2.2 | -   | -   | μs   |

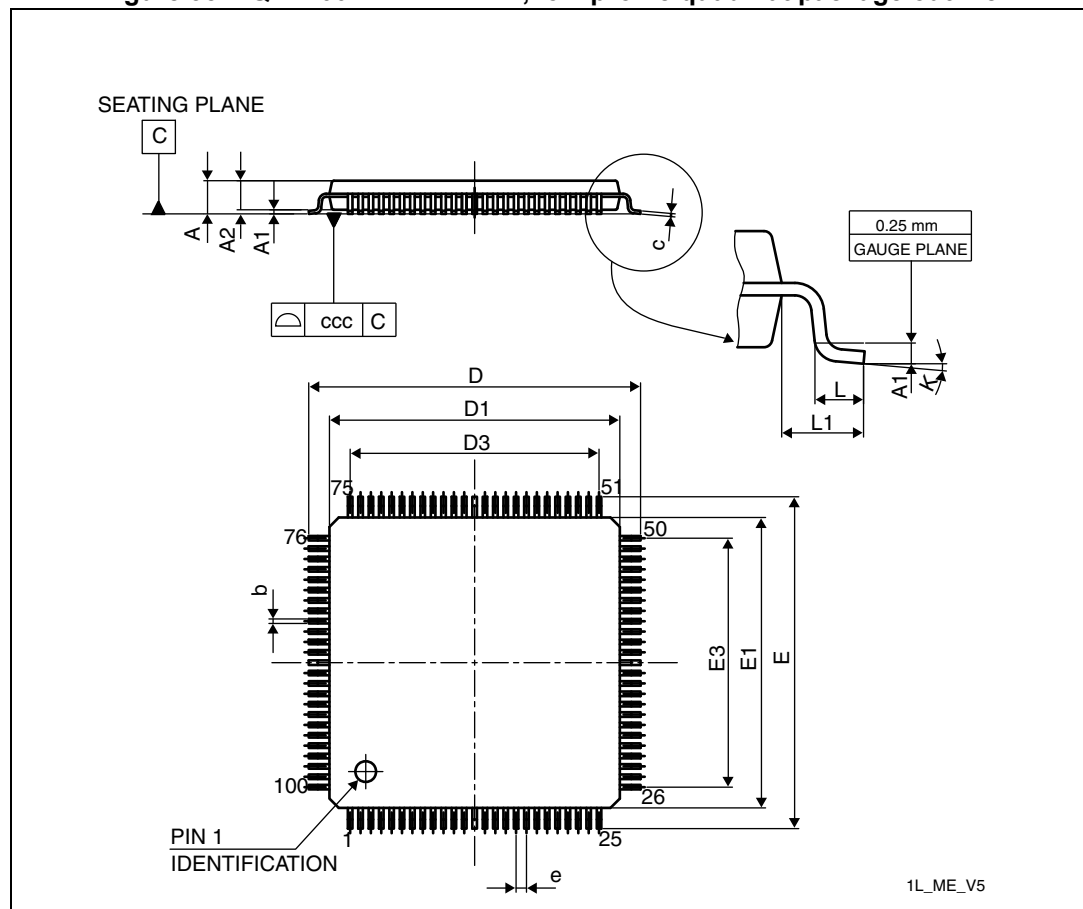
1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

## 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 7.1 LQFP100 – 14 x 14 mm, low-profile quad flat package information

Figure 35. LQFP100 – 14 x 14 mm, low-profile quad flat package outline



1. Drawing is not to scale.

Table 77. LQFP100 – 14 x 14 mm, low-profile quad flat package mechanical data

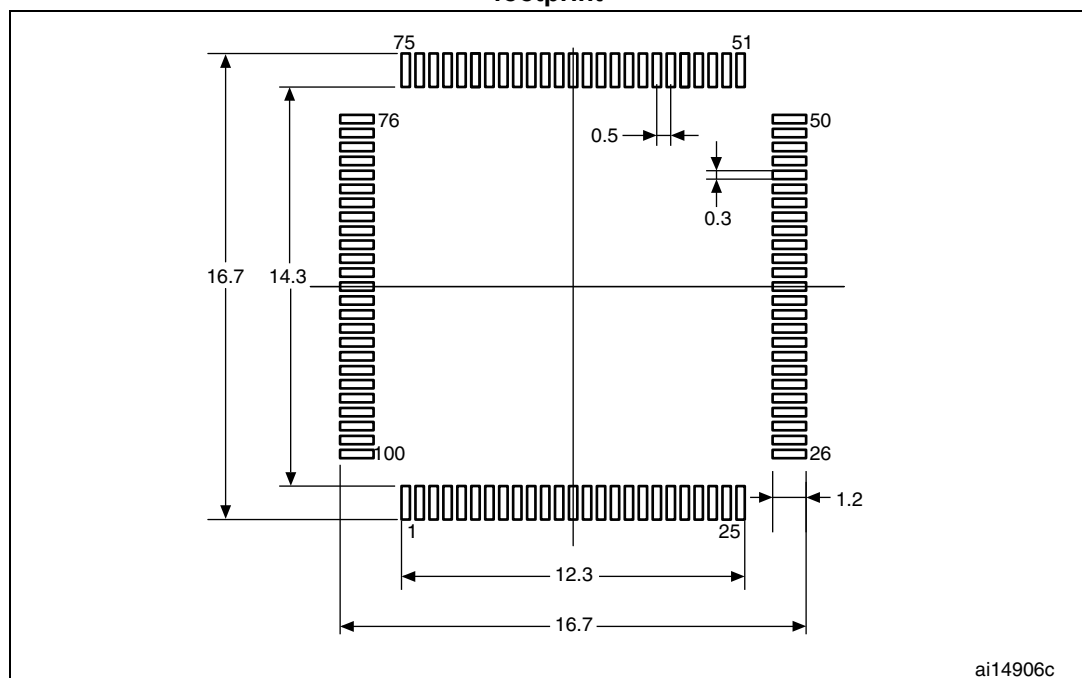
| Symbol | millimeters |     |      | inches <sup>(1)</sup> |     |        |
|--------|-------------|-----|------|-----------------------|-----|--------|
|        | Min         | Typ | Max  | Min                   | Typ | Max    |
| A      | -           | -   | 1.60 | -                     | -   | 0.063  |
| A1     | 0.05        | -   | 0.15 | 0.002                 | -   | 0.0059 |

Table 77. LQPF100 – 14 x 14 mm, low-profile quad flat package mechanical data (continued)

| Symbol | millimeters |       |      | inches <sup>(1)</sup> |        |        |
|--------|-------------|-------|------|-----------------------|--------|--------|
|        | Min         | Typ   | Max  | Min                   | Typ    | Max    |
| A2     | 1.35        | 1.40  | 1.45 | 0.0531                | 0.0551 | 0.0571 |
| b      | 0.17        | 0.22  | 0.27 | 0.0067                | 0.0087 | 0.0106 |
| c      | 0.09        | -     | 0.2  | 0.0035                | -      | 0.0079 |
| D      | 15.80       | 16.00 | 16.2 | 0.622                 | 0.6299 | 0.6378 |
| D1     | 13.80       | 14.00 | 14.2 | 0.5433                | 0.5512 | 0.5591 |
| D3     | -           | 12.00 | -    | -                     | 0.4724 | -      |
| E      | 15.80       | 16.00 | 16.2 | 0.622                 | 0.6299 | 0.6378 |
| E1     | 13.80       | 14.00 | 14.2 | 0.5433                | 0.5512 | 0.5591 |
| E3     | -           | 12.00 | -    | -                     | 0.4724 | -      |
| e      | -           | 0.50  | -    | -                     | 0.0197 | -      |
| L      | 0.45        | 0.60  | 0.75 | 0.0177                | 0.0236 | 0.0295 |
| L1     | -           | 1.00  | -    | -                     | 0.0394 | -      |
| K      | 0°          | 3.5°  | 7°   | 0°                    | 3.5°   | 7°     |
| ccc    | -           | -     | 0.08 | -                     | -      | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 36. LQFP100 – 14 x 14 mm, low-profile quad flat package recommended footprint

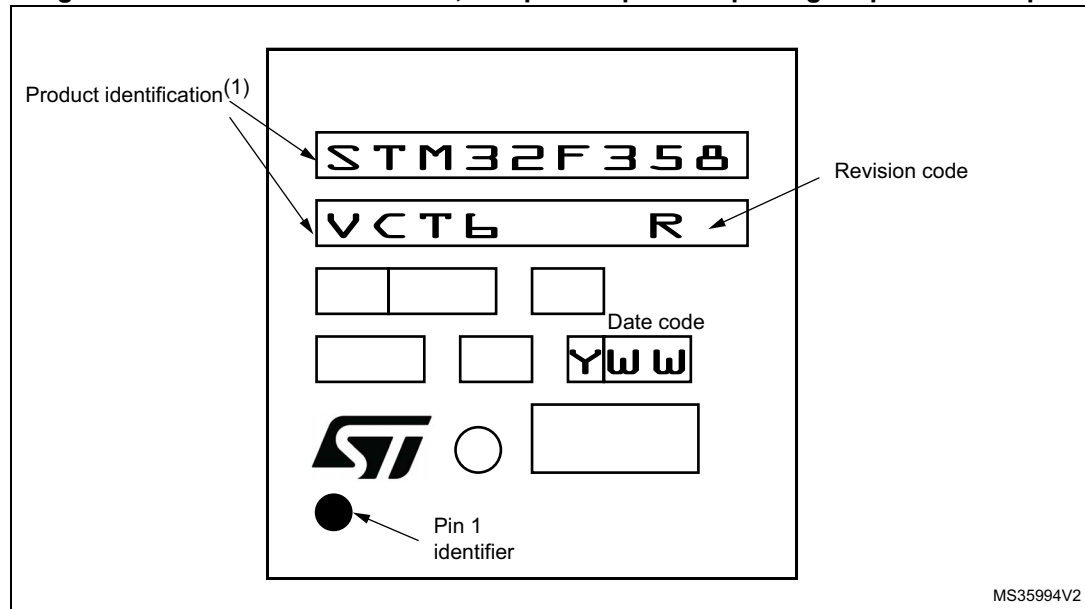


1. Dimensions are in millimeters.

### Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

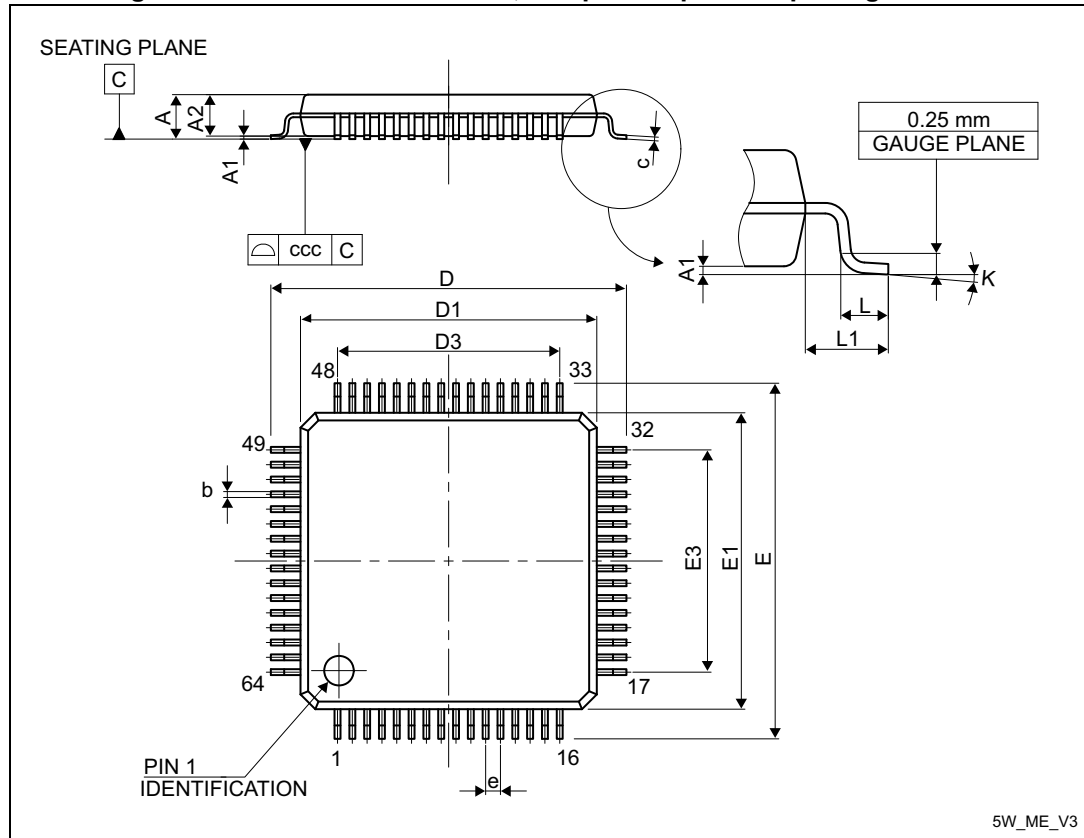
**Figure 37. LQFP100 – 14 x 14 mm, low-profile quad flat package top view example**



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

## 7.2 LQFP64 – 10 x 10 mm, low-profile quad flat package information

Figure 38. LQFP64 – 10 x 10 mm, low-profile quad flat package outline



1. Drawing is not to scale.

Table 78. LQFP64 – 10 x 10 mm, low-profile quad flat package mechanical data

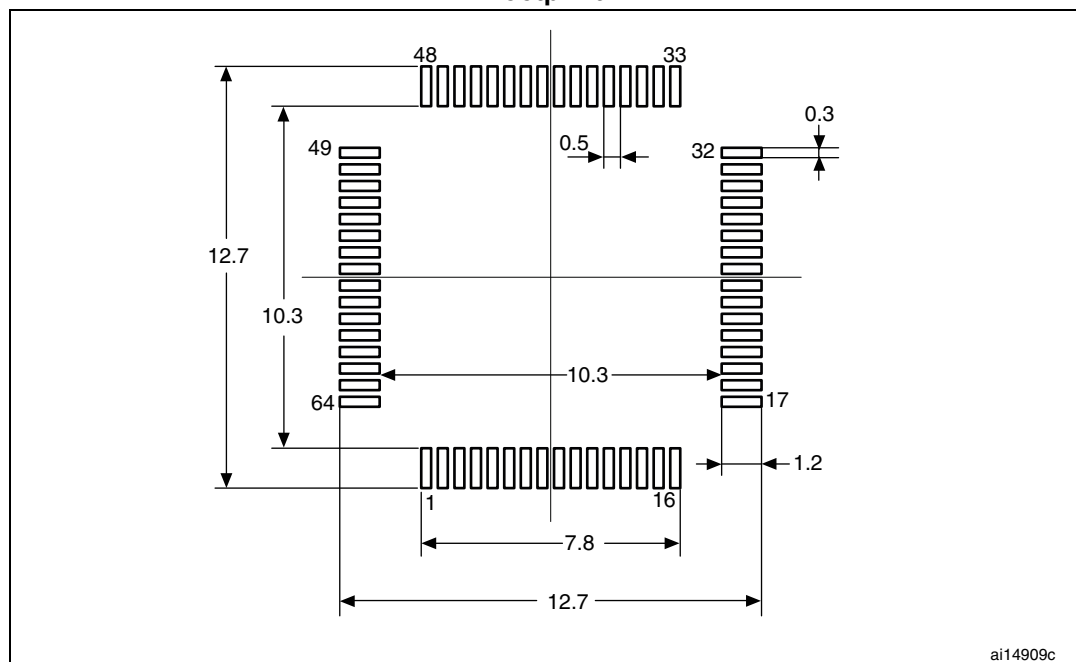
| Symbol | millimeters |       |      | inches <sup>(1)</sup> |        |        |
|--------|-------------|-------|------|-----------------------|--------|--------|
|        | Min         | Typ   | Max  | Min                   | Typ    | Max    |
| A      | -           | -     | 1.60 | -                     | -      | 0.0630 |
| A1     | 0.05        | -     | 0.15 | 0.0020                | -      | 0.0059 |
| A2     | 1.350       | 1.40  | 1.45 | 0.0531                | 0.0551 | 0.0571 |
| b      | 0.17        | 0.22  | 0.27 | 0.0067                | 0.0087 | 0.0106 |
| c      | 0.09        | -     | 0.20 | 0.0035                | -      | 0.0079 |
| D      | -           | 12.00 | -    | -                     | 0.4724 | -      |
| D1     | -           | 10.00 | -    | -                     | 0.3937 | -      |
| D3     | -           | 7.50  | -    | -                     | 0.2953 | -      |
| E      | -           | 12.00 | -    | -                     | 0.4724 | -      |

**Table 78. LQFP64 – 10 x 10 mm, low-profile quad flat package mechanical data  
(continued)**

| Symbol | millimeters |       |      | inches <sup>(1)</sup> |        |        |
|--------|-------------|-------|------|-----------------------|--------|--------|
|        | Min         | Typ   | Max  | Min                   | Typ    | Max    |
| E1     | -           | 10.00 | -    | -                     | 0.3937 | -      |
| E3     | -           | 7.50  | -    | -                     | 0.2953 | -      |
| e      | -           | 0.50  | -    | -                     | 0.0197 | -      |
| K      | 0°          | 3.5°  | 7°   | 0°                    | 3.5°   | 7°     |
| L      | 0.45        | 0.60  | 0.75 | 0.0177                | 0.0236 | 0.0295 |
| L1     | -           | 1.00  | -    | -                     | 0.0394 | -      |
| ccc    | -           | -     | 0.08 | -                     | -      | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 39. LQFP64 – 10 x 10 mm, low-profile quad flat package recommended footprint**

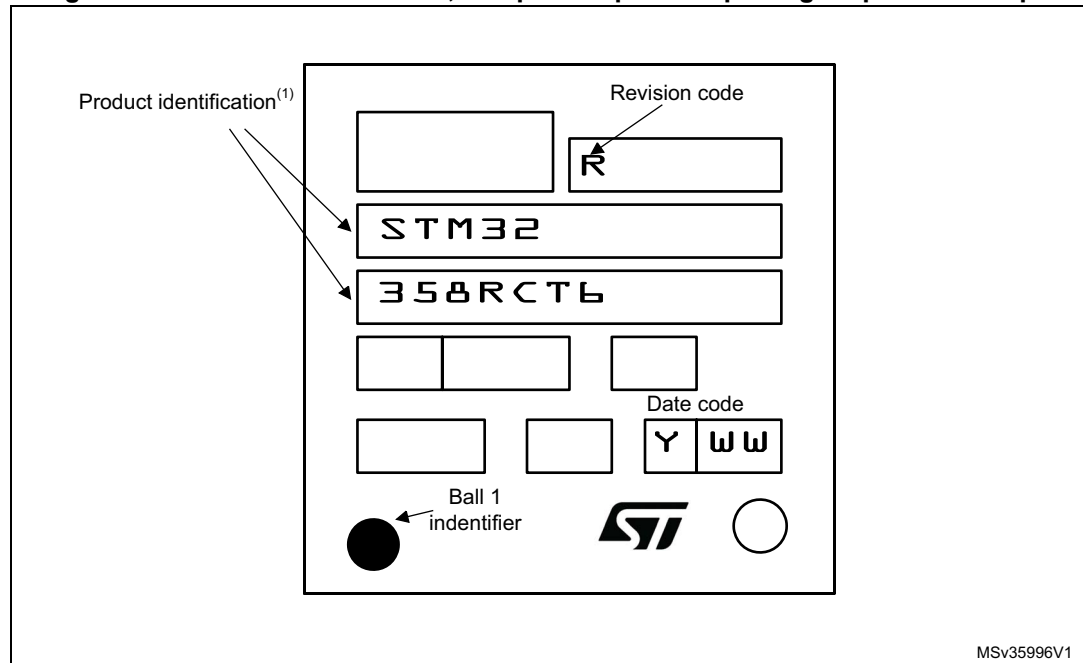


1. Dimensions are in millimeters.

## Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

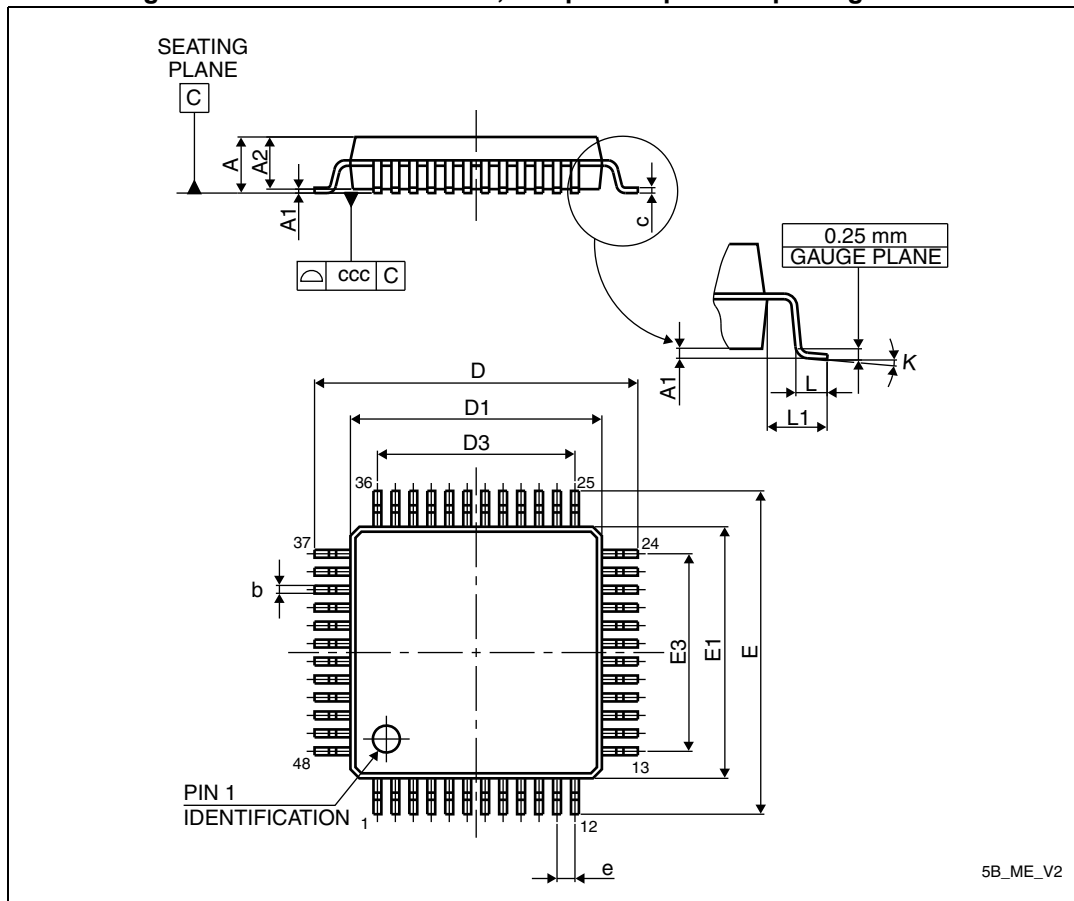
**Figure 40. LQFP64 – 10 x 10 mm, low-profile quad flat package top view example**



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

### 7.3 LQFP48 – 7 x 7 mm, low-profile quad flat package information

Figure 41. LQFP48 – 7 x 7 mm, low-profile quad flat package outline



1. Drawing is not to scale.

Table 79. LQFP48 – 7 x 7 mm, low-profile quad flat package mechanical data

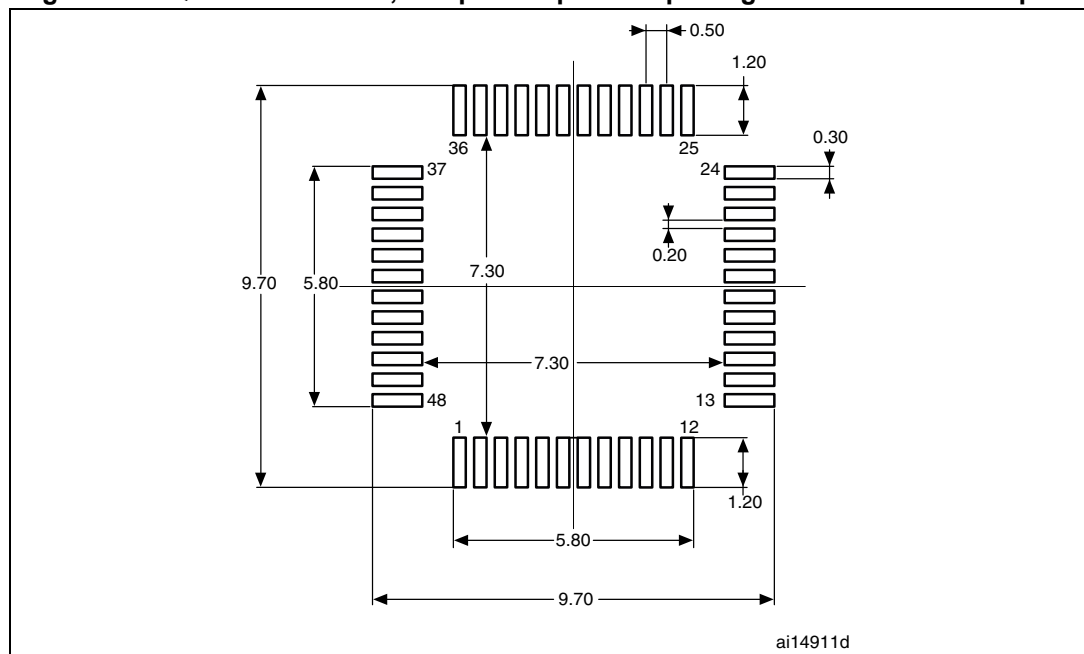
| Symbol | millimeters |      |      | inches <sup>(1)</sup> |        |        |
|--------|-------------|------|------|-----------------------|--------|--------|
|        | Min         | Typ  | Max  | Min                   | Typ    | Max    |
| A      | -           | -    | 1.60 | -                     | -      | 0.0630 |
| A1     | 0.05        | -    | 0.15 | 0.0020                | -      | 0.0059 |
| A2     | 1.35        | 1.40 | 1.45 | 0.0531                | 0.0551 | 0.0571 |
| b      | 0.17        | 0.22 | 0.27 | 0.0067                | 0.0087 | 0.0106 |
| c      | 0.09        | -    | 0.20 | 0.0035                | -      | 0.0079 |
| D      | 8.80        | 9.00 | 9.20 | 0.3465                | 0.3543 | 0.3622 |
| D1     | 6.80        | 7.00 | 7.20 | 0.2677                | 0.2756 | 0.2835 |
| D3     | -           | 5.50 | -    | -                     | 0.2165 | -      |
| E      | 8.80        | 9.00 | 9.20 | 0.3465                | 0.3543 | 0.3622 |

**Table 79. LQFP48 – 7 x 7 mm, low-profile quad flat package mechanical data (continued)**

| Symbol | millimeters |      |      | inches <sup>(1)</sup> |        |        |
|--------|-------------|------|------|-----------------------|--------|--------|
|        | Min         | Typ  | Max  | Min                   | Typ    | Max    |
| E1     | 6.80        | 7.00 | 7.20 | 0.2677                | 0.2756 | 0.2835 |
| E3     | -           | 5.50 | -    | -                     | 0.2165 | -      |
| e      | -           | 0.50 | -    | -                     | 0.0197 | -      |
| L      | 0.45        | 0.60 | 0.75 | 0.0177                | 0.0236 | 0.0295 |
| L1     | -           | 1.00 | -    | -                     | 0.0394 | -      |
| K      | 0°          | 3.5° | 7°   | 0°                    | 3.5°   | 7°     |
| ccc    | -           | -    | 0.08 | -                     | -      | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 42. LQFP48 - 7 x 7 mm, low-profile quad flat package recommended footprint**

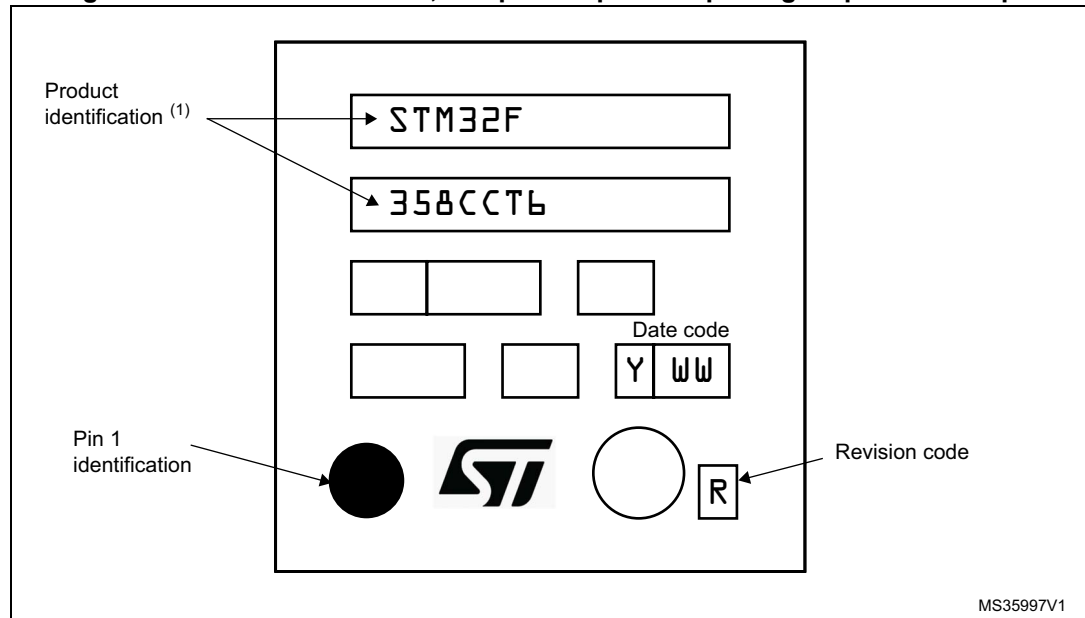


1. Dimensions are in millimeters.

### Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

**Figure 43. LQFP48 - 7 x 7 mm, low-profile quad flat package top view example**



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

## 7.4 Thermal characteristics

The maximum chip junction temperature ( $T_{Jmax}$ ) must never exceed the values given in [Table 24: General operating conditions on page 56](#).

The maximum chip-junction temperature,  $T_J$  max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- $T_A$  max is the maximum ambient temperature in °C,
- $\Theta_{JA}$  is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D$  max is the sum of  $P_{INT}$  max and  $P_{I/O}$  max ( $P_D \text{ max} = P_{INT} \text{ max} + P_{I/O} \text{ max}$ ),
- $P_{INT}$  max is the product of  $I_{DD}$  and  $V_{DD}$ , expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$  max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual  $V_{OL} / I_{OL}$  and  $V_{OH} / I_{OH}$  of the I/Os at low and high level in the application.

**Table 80. Package thermal characteristics**

| Symbol        | Parameter                                                                         | Value | Unit |
|---------------|-----------------------------------------------------------------------------------|-------|------|
| $\Theta_{JA}$ | <b>Thermal resistance junction-ambient</b><br>LQFP64 - 10 × 10 mm / 0.5 mm pitch  | 45    | °C/W |
|               | <b>Thermal resistance junction-ambient</b><br>LQFP48 - 7 × 7 mm                   | 55    |      |
|               | <b>Thermal resistance junction-ambient</b><br>LQFP100 - 14 × 14 mm / 0.5 mm pitch | 41    |      |

### 7.4.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from [www.jedec.org](http://www.jedec.org)

## 7.4.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in [Section 8: Part numbering](#).

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F358xC devices at the maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

### Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature  $T_{Amax} = 82\text{ °C}$  (measured according to JESD51-2),  
 $I_{DDmax} = 50\text{ mA}$ ,  $V_{DD} = 3.5\text{ V}$ , maximum 3 I/Os used at the same time in output at low level with  $I_{OL} = 8\text{ mA}$ ,  $V_{OL} = 0.4\text{ V}$  and maximum 2 I/Os used at the same time in output at low level with  $I_{OL} = 20\text{ mA}$ ,  $V_{OL} = 1.3\text{ V}$

$$P_{INTmax} = 50\text{ mA} \times 3.5\text{ V} = 175\text{ mW}$$

$$P_{IOmax} = 3 \times 8\text{ mA} \times 0.4\text{ V} + 2 \times 20\text{ mA} \times 1.3\text{ V} = 61.6\text{ mW}$$

This gives:  $P_{INTmax} = 175\text{ mW}$  and  $P_{IOmax} = 61.6\text{ mW}$ :

$$P_{Dmax} = 175 + 61.6 = 236.6\text{ mW}$$

Thus:  $P_{Dmax} = 236.6\text{ mW}$

Using the values obtained in [Table 80](#)  $T_{Jmax}$  is calculated as follows:

– For LQFP64,  $45\text{ °C/W}$

$$T_{Jmax} = 82\text{ °C} + (45\text{ °C/W} \times 236.6\text{ mW}) = 82\text{ °C} + 10.65\text{ °C} = 92.65\text{ °C}$$

This is within the range of the suffix 6 version parts ( $-40 < T_J < 105\text{ °C}$ ).

In this case, parts must be ordered at least with the temperature range suffix 6 (see [Section 8: Part numbering](#)).

**Example 2: High-temperature application**

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature  $T_J$  remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature  $T_{Amax} = 115\text{ °C}$  (measured according to JESD51-2),  
 $I_{DDmax} = 20\text{ mA}$ ,  $V_{DD} = 3.5\text{ V}$ , maximum 9 I/Os used at the same time in output at low level with  $I_{OL} = 8\text{ mA}$ ,  $V_{OL} = 0.4\text{ V}$

$$P_{INTmax} = 20\text{ mA} \times 3.5\text{ V} = 70\text{ mW}$$

$$P_{IOmax} = 9 \times 8\text{ mA} \times 0.4\text{ V} = 28.8\text{ mW}$$

This gives:  $P_{INTmax} = 70\text{ mW}$  and  $P_{IOmax} = 28.8\text{ mW}$ :

$$P_{Dmax} = 70 + 28.8 = 98.8\text{ mW}$$

Thus:  $P_{Dmax} = 98.8\text{ mW}$

Using the values obtained in [Table 80](#)  $T_{Jmax}$  is calculated as follows:

– For LQFP100,  $41\text{ °C/W}$

$$T_{Jmax} = 115\text{ °C} + (41\text{ °C/W} \times 98.8\text{ mW}) = 115\text{ °C} + 4.05\text{ °C} = 119.05\text{ °C}$$

This is within the range of the suffix 7 version parts ( $-40 < T_J < 125\text{ °C}$ ).

In this case, parts must be ordered at least with the temperature range suffix 7 (see [Section 8: Part numbering](#)).

# 8 Part numbering

Table 81. Ordering information scheme

|                                                                                                   |       |   |     |   |   |   |   |     |
|---------------------------------------------------------------------------------------------------|-------|---|-----|---|---|---|---|-----|
| Example:                                                                                          | STM32 | F | 358 | R | C | T | 6 | xxx |
| <b>Device family</b>                                                                              |       |   |     |   |   |   |   |     |
| STM32 = ARM-based 32-bit microcontroller                                                          |       |   |     |   |   |   |   |     |
| <b>Product type</b>                                                                               |       |   |     |   |   |   |   |     |
| F = general-purpose                                                                               |       |   |     |   |   |   |   |     |
| <b>Device subfamily</b>                                                                           |       |   |     |   |   |   |   |     |
| 358 = STM32F358                                                                                   |       |   |     |   |   |   |   |     |
| <b>Pin count</b>                                                                                  |       |   |     |   |   |   |   |     |
| C = 48 pins<br>R = 64 pins<br>V = 100 pins                                                        |       |   |     |   |   |   |   |     |
| <b>Flash memory size</b>                                                                          |       |   |     |   |   |   |   |     |
| C = 256 Kbytes of Flash memory                                                                    |       |   |     |   |   |   |   |     |
| <b>Package</b>                                                                                    |       |   |     |   |   |   |   |     |
| T = LQFP                                                                                          |       |   |     |   |   |   |   |     |
| <b>Temperature range</b>                                                                          |       |   |     |   |   |   |   |     |
| 6 = Industrial temperature range, −40 to 85 °C<br>7 = Industrial temperature range, −40 to 105 °C |       |   |     |   |   |   |   |     |
| <b>Options</b>                                                                                    |       |   |     |   |   |   |   |     |
| xxx = programmed parts<br>TR = tape and reel                                                      |       |   |     |   |   |   |   |     |

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

## 9 Revision history

**Table 82. Document revision history**

| Date        | Revision | Changes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 17-Apr-2014 | 1        | Initial release.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 10-Dec-2014 | 2        | <p>Updated core description in cover page.</p> <p>Updated <a href="#">Figure 1: STM32F358xC block diagram</a>.</p> <p>Updated HSI characteristics <a href="#">Table 42: HSI oscillator characteristics</a> and <a href="#">Figure 17: HSI oscillator accuracy characterization results for soldered parts</a>.</p> <p>Updated <a href="#">Table 29: Typical and maximum current consumption from the VDDA supply</a>.</p> <p>Updated <a href="#">Table 51: I/O current injection susceptibility</a> adding 'on NPOR pin'.</p> <p>Updated <a href="#">Table 37: Low-power mode wakeup timings</a>.</p> <p>Updated <a href="#">Figure 18: TC and TTa I/O input characteristics</a> and <a href="#">Figure 19: Five volt tolerant (FT and FTf) I/O input characteristics</a>.</p> <p>Updated <a href="#">Table 13: STM32F358xC pin definitions</a> adding note for I/Os featuring an analog output function (DAC_OUT, OPAMP_OUT).</p> <p>Updated <a href="#">Table 64: ADC characteristics</a> adding IDDA &amp; IREF consumptions.</p> <p>Added <a href="#">Figure 28: ADC typical current consumption on VDDA pin</a> and <a href="#">Figure 29: ADC typical current consumption on VREF+ pin</a>.</p> <p>Added <a href="#">Section 3.8: Interconnect matrix</a>.</p> <p>Updated <a href="#">Section 6.3.5: Wakeup time from low-power mode</a> removing standby mode.</p> <p>Added note for <a href="#">Table 31: Typical and maximum VDDA consumption in Stop mode</a> and <a href="#">Table 30: Typical and maximum VDD consumption in Stop mode</a>.</p> <p>Updated <a href="#">Section 7: Package information</a> with new LQFP100, LQFP64, LQFP48 package markings.</p> <p>Updated <a href="#">Table 13: STM32F358xC pin definitions</a> and alternate functions tables replacing usart_rts by usart_rts_de.</p> |

Table 82. Document revision history (continued)

| Date        | Revision | Changes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 30-Jan-2015 | 3        | Updated <a href="#">Section 6.3.20: Comparator characteristics</a> modifying ts_sc, V <sub>DDA</sub> characteristics in <a href="#">Table 76</a> and adding <a href="#">Figure 36: Maximum VREFINT scaler startup time from power down</a> .<br>Updated I <sub>DD</sub> data current consumption in <a href="#">Table 40: HSE oscillator characteristics</a> .                                                                                                                                                                                                                                                                                                                              |
| 17-Apr-2015 | 4        | Updated <a href="#">Table 36: Peripheral current consumption</a> with 12.6uA/MHz-BusMatrix, 7.6uA/MHz-DMA1, 6.1uA/MHz-DMA2 new current values.<br>Updated <a href="#">Section 7: Package information</a> : with new package information structure adding 1 sub paragraph for each package.<br>Updated <a href="#">Figure 40: LQFP100 – 14 x 14 mm, low-profile quad flat package top view example</a> removing gate mark.<br>Added note for all package device markings: “the following figure gives an example of topside marking orientation versus pin 1 identifier location”.<br>Updated <a href="#">Table 82: LQFP64 – 10 x 10 mm, low-profile quad flat package mechanical data</a> . |

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