

ARM®-based Cortex®-M7 32b MCU+FPU, 428DMIPS, up to 1MB Flash/320+16+ 4KB RAM, crypto, USB OTG HS/FS, ethernet, 18 TIMs, 3 ADCs, 25 com itf, cam & LCD

Data brief

## Features

- Core: ARM® 32-bit Cortex®-M7 CPU with FPU, adaptive real-time accelerator (ART Accelerator™) and L1 cache: 4KB data cache and 4KB instruction cache, allowing 0-wait state execution from embedded Flash memory and external memories, frequency up to 200 MHz, MPU, 428 DMIPS/2.14 DMIPS/MHz (Dhrystone 2.1), and DSP instructions.
- Memories
  - Up to 1MB of Flash memory
  - SRAM: 320KB (including 64KB of data TCM RAM for critical real time data) + 16KB of instruction TCM RAM (for critical real time routines) + 4KB of backup SRAM (available in the lowest power modes)
  - Flexible external memory controller with up to 32-bit data bus: SRAM, PSRAM, SDRAM/LPDDR SDRAM, NOR/NAND memories
- Dual mode Quad SPI
- LCD parallel interface, 8080/6800 modes
- LCD-TFT controller up to XGA resolution with dedicated Chrom-ART Accelerator™ for enhanced graphic content creation (DMA2D)
- Clock, reset and supply management
  - 1.7 V to 3.6 V application supply and I/Os
  - POR, PDR, PVD and BOR
  - Dedicated USB power
  - 4-to-26 MHz crystal oscillator
  - Internal 16 MHz factory-trimmed RC (1% accuracy)
  - 32 kHz oscillator for RTC with calibration
  - Internal 32 kHz RC with calibration
- Low power
  - Sleep, Stop and Standby modes
  - V<sub>BAT</sub> supply for RTC, 32×32 bit backup registers + 4KB backup SRAM
- 3×12-bit, 2.4 MSPS ADC: up to 24 channels and 7.2 MSPS in triple interleaved mode
- 2×12-bit D/A converters
- General-purpose DMA: 16-stream DMA controller with FIFOs and burst support
- Up to 18 timers: up to thirteen 16-bit (1x low power 16-bit timer available in stop mode) and two 32-bit timers, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input. All 15 timers running up to 200 MHz. 2x watchdogs, SysTick timer

|                                                                                   |                                                                                     |                                                                                     |
|-----------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|
|  |  |  |
| LQFP100 (14 × 14 mm)                                                              | UFPGA176 (10 × 10 mm)                                                               | WLCSP143                                                                            |
| LQFP144 (20 × 20 mm)                                                              | TBGA216 (13 × 13 mm)                                                                |                                                                                     |
| LQFP176 (24 × 24 mm)                                                              |                                                                                     |                                                                                     |
| LQFP208 (28 × 28 mm)                                                              |                                                                                     |                                                                                     |

- Debug mode
  - SWD & JTAG interfaces
  - Cortex®-M7 Trace Macrocell™
- Up to 168 I/O ports with interrupt capability
  - Up to 164 fast I/Os up to 100 MHz
  - Up to 166 5 V-tolerant I/Os
- Up to 25 communication interfaces
  - Up to 4× I<sup>2</sup>C interfaces (SMBus/PMBus)
  - Up to 4 USARTs/4 UARTs (12.5 Mbit/s, ISO7816 interface, LIN, IrDA, modem control)
  - Up to 6 SPIs (up to 50 Mbits/s), 3 with muxed simplex I<sup>2</sup>S for audio class accuracy via internal audio PLL or external clock
  - 2 × SAI (serial audio interface)
  - 2 × CAN (2.0B Active) and SDMMC interface
  - SPDIF-IN interface
  - HDMI-CEC
- Advanced connectivity
  - USB 2.0 full-speed device/host/OTG controller with on-chip PHY
  - USB 2.0 high-speed/full-speed device/host/OTG controller with dedicated DMA, on-chip full-speed PHY and ULPI
  - 10/100 Ethernet MAC with dedicated DMA: supports IEEE 1588v2 hardware, MII/RMII
- 8- to 14-bit parallel camera interface up to 54 Mbytes/s
- Cryptographic acceleration: hardware acceleration for AES 128, 192, 256, Triple DES, HASH (MD5, SHA-1, SHA-2), and HMAC
- True random number generator
- CRC calculation unit
- RTC: subsecond accuracy, hardware calendar
- 96-bit unique ID

Table 1. Device summary

| Reference   | Part number                                                                                                                      |
|-------------|----------------------------------------------------------------------------------------------------------------------------------|
| STM32F756xx | STM32F756VG, STM32F756ZG, STM32F756IG, STM32F756BG, STM32F756NG, STM32F756IE, STM32F756VE, STM32F756ZE, STM32F756BE, STM32F756NE |

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# 1 Description

The STM32F756xx devices are based on the high-performance ARM® Cortex®-M7 32-bit RISC core operating at up to 200 MHz frequency. The Cortex®-M7 core features a single floating point unit (SFPU) precision which supports all ARM® single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32F756xx devices incorporate high-speed embedded memories with Flash memory up to 1 Mbyte, 320 KB of SRAM (including 64 KB of Data TCM RAM for critical real time data), 16 KB of instruction TCM RAM (for critical real time routines), 4 KB of backup SRAM available in the lowest power modes, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses, a 32-bit multi-AHB bus matrix and a multi layer AXI interconnect supporting internal and external memories access.

All devices offer three 12-bit ADCs, two DACs, a low-power RTC, twelve general-purpose 16-bit timers including two PWM timers for motor control, two general-purpose 32-bit timers, a true random number generator (RNG), and a cryptographic acceleration cell. They also feature standard and advanced communication interfaces.

- Up to four I<sup>2</sup>Cs
- Six SPIs, three I<sup>2</sup>Ss in duplex mode. To achieve audio class accuracy, the I<sup>2</sup>S peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization.
- Four USARTs plus four UARTs
- An USB OTG full-speed and a USB OTG high-speed with full-speed capability (with the ULPI),
- Two CANs
- Two SAI serial audio interfaces
- An SDMMC host interface
- Ethernet and camera interface
- LCD-TFT display controller
- Chrom-ART Accelerator™.
- SPDIF-Rx interface
- HDMI-CEC

Advanced peripherals include an SDMMC interface, a flexible memory control (FMC) interface, a Quad SPI flash memories interface, a camera interface for CMOS sensors and a cryptographic acceleration cell. Refer to [Table 2: STM32F756xx features and peripheral counts](#) for the list of peripherals available on each part number.

The STM32F756xx devices operate in the –40 to +105 °C temperature range from a 1.7 to 3.6 V power supply. A dedicated supply input for USB (OTG\_FS and OTG\_HS) is available on all packages except LQFP100 for greater power supply choice.

The supply voltage can drop to 1.7 V with the use of an external power supply supervisor (refer to [Section 2.17.2: Internal reset OFF](#)). A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F756xx devices offer devices in 7 packages ranging from 100 pins to 216 pins. The set of included peripherals changes with the device chosen.

These features make the STM32F756xx microcontrollers suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances
- Mobile applications, Internet of Things
- Wearable devices: smartwatches.

Figure 2 shows the general block diagram of the device family

**Table 2. STM32F756xx features and peripheral counts**

| Peripherals                    |                        | STM32F756Vx                  |      | STM32F756Zx                  |      | STM32F756Ix |      | STM32F756Bx |      | STM32F756Nx |      |
|--------------------------------|------------------------|------------------------------|------|------------------------------|------|-------------|------|-------------|------|-------------|------|
| Flash memory in Kbytes         |                        | 512                          | 1024 | 512                          | 1024 | 512         | 1024 | 512         | 1024 | 512         | 1024 |
| SRAM in Kbytes                 | System                 | 320(240+16+64)               |      |                              |      |             |      |             |      |             |      |
|                                | Instruction            | 16                           |      |                              |      |             |      |             |      |             |      |
|                                | Backup                 | 4                            |      |                              |      |             |      |             |      |             |      |
| FMC memory controller          |                        | Yes <sup>(1)</sup>           |      |                              |      |             |      |             |      |             |      |
| Ethernet                       |                        | Yes                          |      |                              |      |             |      |             |      |             |      |
| Timers                         | General-purpose        | 10                           |      |                              |      |             |      |             |      |             |      |
|                                | Advanced-control       | 2                            |      |                              |      |             |      |             |      |             |      |
|                                | Basic                  | 2                            |      |                              |      |             |      |             |      |             |      |
|                                | Low-power              | 1                            |      |                              |      |             |      |             |      |             |      |
| Random number generator        |                        | Yes                          |      |                              |      |             |      |             |      |             |      |
| Communication interfaces       | SPI / I <sup>2</sup> S | 4/3 (simplex) <sup>(2)</sup> |      | 6/3 (simplex) <sup>(2)</sup> |      |             |      |             |      |             |      |
|                                | I <sup>2</sup> C       | 4                            |      |                              |      |             |      |             |      |             |      |
|                                | USART/UART             | 4/4                          |      |                              |      |             |      |             |      |             |      |
|                                | USB OTG FS             | Yes                          |      |                              |      |             |      |             |      |             |      |
|                                | USB OTG HS             | Yes                          |      |                              |      |             |      |             |      |             |      |
|                                | CAN                    | 2                            |      |                              |      |             |      |             |      |             |      |
|                                | SAI                    | 2                            |      |                              |      |             |      |             |      |             |      |
|                                | SPDIF-RX               | 4 inputs                     |      |                              |      |             |      |             |      |             |      |
|                                | SDMMC                  | Yes                          |      |                              |      |             |      |             |      |             |      |
| Camera interface               |                        | Yes                          |      |                              |      |             |      |             |      |             |      |
| LCD-TFT                        |                        | Yes                          |      |                              |      |             |      |             |      |             |      |
| Chrom-ART Accelerator™ (DMA2D) |                        | Yes                          |      |                              |      |             |      |             |      |             |      |
| Cryptography                   |                        | Yes                          |      |                              |      |             |      |             |      |             |      |
| GPIOs                          |                        | 82                           |      | 114                          |      | 140         |      | 168         |      |             |      |
| 12-bit ADC                     |                        | 3                            |      |                              |      |             |      |             |      |             |      |
| Number of channels             |                        | 16                           |      | 24                           |      |             |      |             |      |             |      |



Table 2. STM32F756xx features and peripheral counts (continued)

| Peripherals                      | STM32F756Vx                                          | STM32F756Zx         | STM32F756Ix         | STM32F756Bx | STM32F756Nx |
|----------------------------------|------------------------------------------------------|---------------------|---------------------|-------------|-------------|
| 12-bit DAC<br>Number of channels | Yes<br>2                                             |                     |                     |             |             |
| Maximum CPU frequency            | 200 MHz                                              |                     |                     |             |             |
| Operating voltage                | 1.7 to 3.6 V <sup>(3)</sup>                          |                     |                     |             |             |
| Operating temperatures           | Ambient temperatures: –40 to +85 °C / –40 to +105 °C |                     |                     |             |             |
|                                  | Junction temperature: –40 to + 125 °C                |                     |                     |             |             |
| Package                          | LQFP100                                              | WLCSP143<br>LQFP144 | UFBGA176<br>LQFP176 | LQFP208     | TFBGA216    |

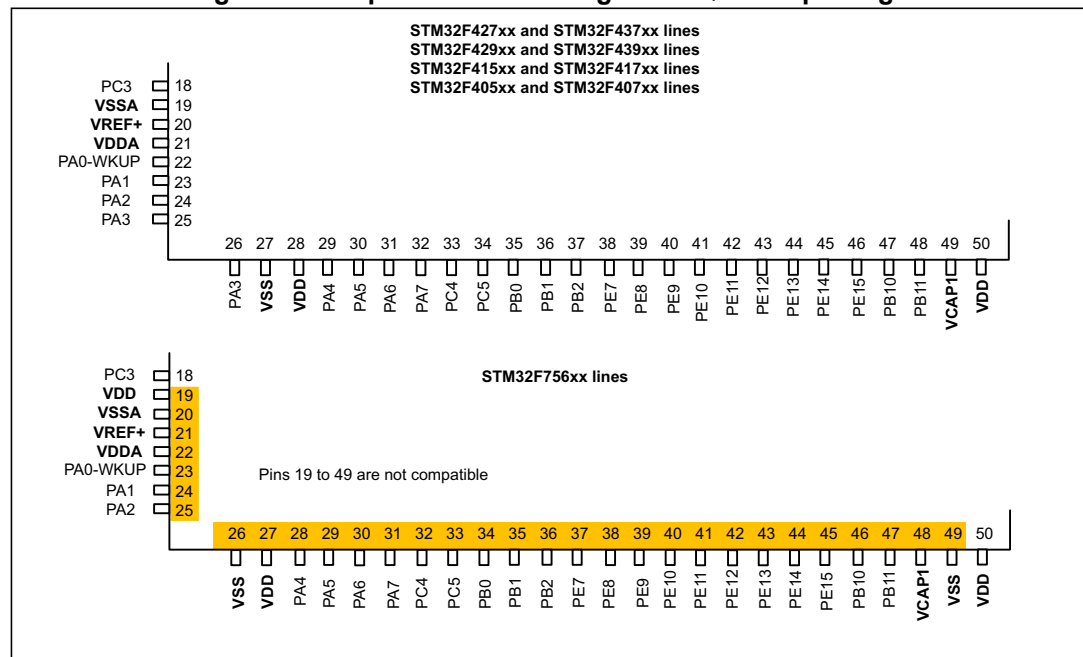
1. For the LQFP100 package, only FMC Bank1 is available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select.
2. The SPI1, SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
3. VDD/VDDA minimum value of 1.7 V is obtained when the internal reset is OFF (refer to [Section 2.17.2: Internal reset OFF](#)).

## 1.1 Full compatibility throughout the family

The STM32F756xx devices are fully pin-to-pin, compatible with the STM32F4xx devices, allowing the user to try different peripherals, and reaching higher performances (higher frequency) for a greater degree of freedom during the development cycle.

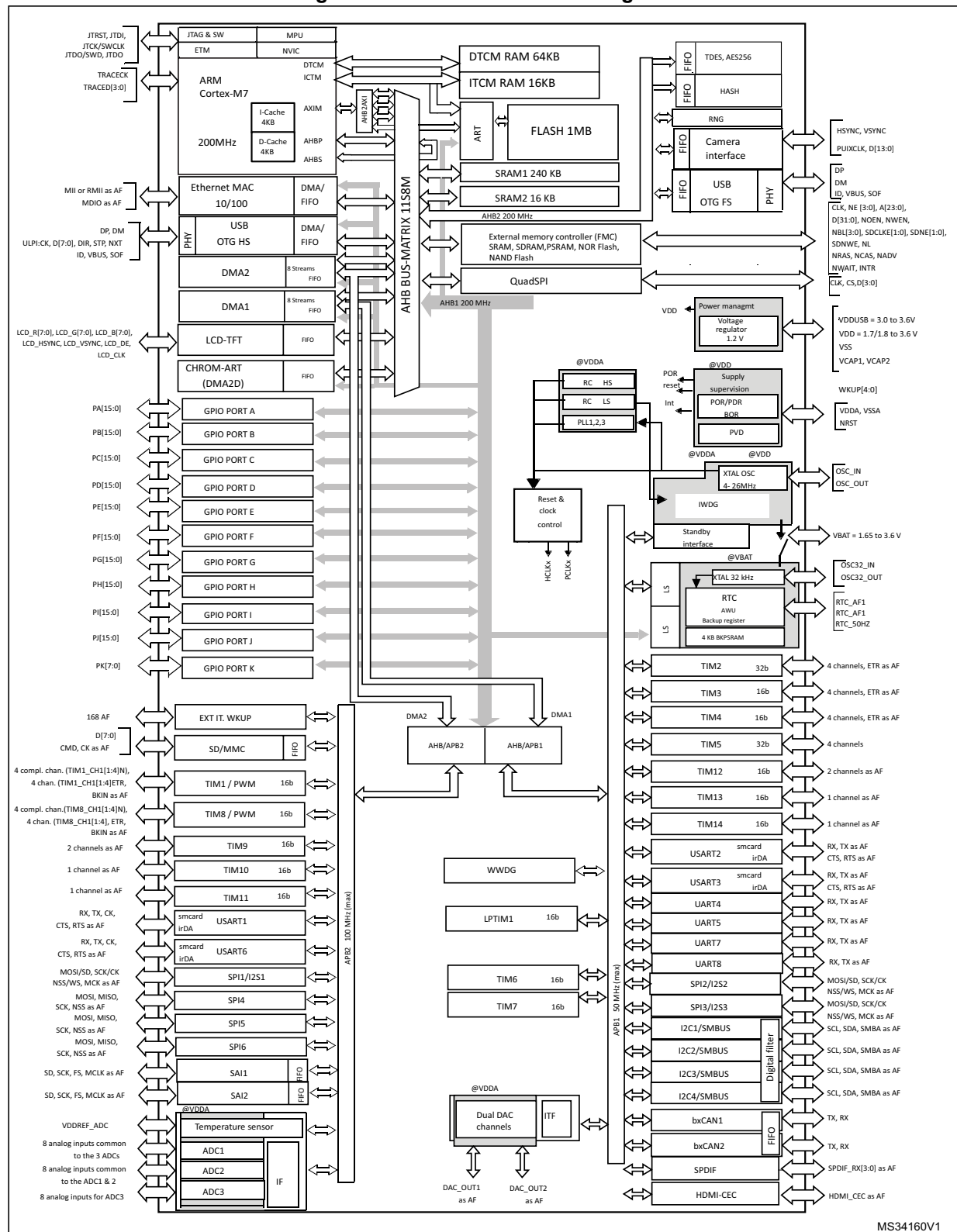
*Figure 1* give compatible board designs between the STM32F4xx families.

**Figure 1. Compatible board design for LQFP100 package**



The STM32F75x LQFP144, LQFP176, LQFP208, TFBGA216, UFBGA176, WLCSP143 packages are fully pin to pin compatible with STM32F4xx devices.

Figure 2. STM32F756xx block diagram



1. The timers connected to APB2 are clocked from TIMxCLK up to 200 MHz, while the timers connected to APB1 are clocked from TIMxCLK either up to 100 MHz or 200 MHz depending on TIMPRE bit configuration in the RCC\_DCKCFGR register.

## 2 Functional overview

### 2.1 ARM® Cortex®-M7 with FPU

The ARM® Cortex®-M7 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and low interrupt latency.

The Cortex®-M7 processor is a highly efficient high-performance featuring:

- Six-stage dual-issue pipeline
- Dynamic branch prediction
- Harvard caches (4kB of I-cache and 4kB of D-cache)
- 64-bit AXI4 interface
- 64-bit ITCM interface
- 2x32-bit DTCM interfaces

The processor supports the following memory interfaces:

- Tightly Coupled Memory (TCM) interface.
- Harvard instruction and data caches and AXI master (AXIM) interface.
- Dedicated low-latency AHB-Lite peripheral (AHBP) interface.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

*Figure 2* shows the general block diagram of the STM32F756xx family.

*Note:* Cortex®-M7 with FPU core is binary compatible with the Cortex®-M4 core.

### 2.2 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

## 2.3 Embedded Flash memory

The STM32F756xx devices embed a Flash memory of up to 1 Mbytes available for storing programs and data.

## 2.4 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

## 2.5 Embedded SRAM

All devices features:

- System SRAM up to 320Kbytes :
  - SRAM1 on AHB bus Matrix: 240Kbytes
  - SRAM2 on AHB bus Matrix: 16Kbytes
  - DTCM-RAM on TCM interface (Tightly Coupled Memory interface): 64 Kbytes for critical real time data.
- Instruction RAM (ITCM-RAM) 16Kbytes:
  - It is mapped on TCM interface and reserved only for CPU Execution/Instruction useful for critical real time routines.

The Data TCM RAM is accessible by the GP-DMA's and peripherals DMA's through specific AHB slave of the CPU. The instruction TCM RAM is reserved only for CPU. It is accessed at CPU clock speed with 0 wait states.

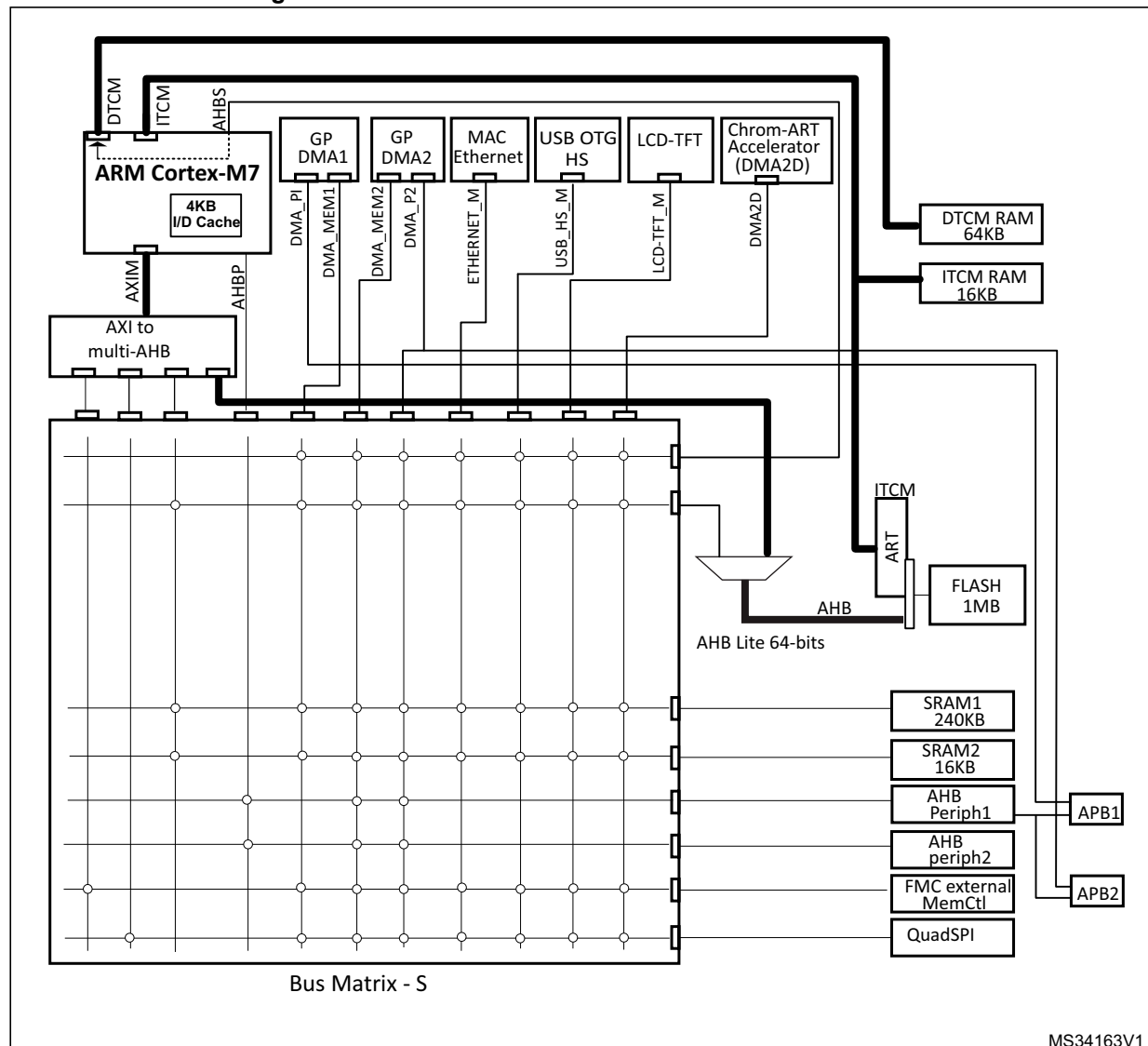
- 4 Kbytes of backup SRAM
  - This area is accessible only from the CPU. Its content is protected against possible unwanted write accesses, and is retained in Standby or VBAT mode.

## 2.6 AXI-AHB bus matrix

The STM32F756xx system architecture is based on 2 sub-systems :

- An AXI to multi AHB bridge converting AXI4 protocol to AHB-Lite protocol:
  - 3x AXI to 32-bit AHB bridges connected to AHB bus matrix
  - 1x AXI to 64-bit AHB bridge connected to the embedded flash
- A multi-AHB Bus-Matrix
  - The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMA's, Ethernet, USB HS, LCD-TFT, and DMA2D) and the slaves (Flash memory, RAM, FMC, Quad SPI, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 3. STM32F756xx AXI-AHB bus matrix architecture



1. The above figure has large wires for 64-bits bus and thin wires for 32-bits bus.

## 2.7 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals:

- SPI and I<sup>2</sup>S
- I<sup>2</sup>C
- USART
- General-purpose, basic and advanced-control timers TIMx
- DAC
- SDMMC
- Cryptographic acceleration
- Camera interface (DCMI)
- ADC
- SAI
- SPDIF-RX
- Quad SPI
- HDMI-CEC

## 2.8 Flexible memory controller (FMC)

The Flexible memory controller (FMC) includes three memory controllers:

- The NOR/PSRAM memory controller
- The NAND/memory controller
- The Synchronous DRAM (SDRAM/Mobile LPDDR SDRAM) controller

The main features of the FMC controller are the following:

- Interface with static-memory mapped devices including:
  - Static random access memory (SRAM)
  - NOR Flash memory/OneNAND Flash memory
  - PSRAM (4 memory banks)
  - NAND Flash memory with ECC hardware to check up to 8 Kbytes of data
- Interface with synchronous DRAM (SDRAM/Mobile LPDDR SDRAM) memories
- 8-,16-,32-bit data bus width
- Independent Chip Select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO
- Read FIFO for SDRAM controller
- The Maximum FMC\_CLK/FMC\_SDCLK frequency for synchronous accesses is HCLK/2.

### LCD parallel interface

The FMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

## 2.9 Quad SPI memory interface (QUADSPI)

All STM32F75xx devices embed a Quad SPI memory interface, which is a specialized communication interface targetting Single, Dual or Quad SPI flash memories. It can work in:

- Direct mode through registers
- External flash status register polling mode
- Memory mapped mode.

Up to 256 Mbytes external flash are memory mapped, supporting 8, 16 and 32-bit access. Code execution is supported.

The opcode and the frame format are fully programmable. Communication can be either in Single Data Rate or Dual Data Rate.

## 2.10 LCD-TFT controller

The LCD-TFT display controller provides a 24-bit parallel digital RGB (Red, Green, Blue) and delivers all signals to interface directly to a broad range of LCD and TFT panels up to XGA (1024x768) resolution with the following features:

- 2 displays layers with dedicated FIFO (64x32-bit)
- Color Look-Up table (CLUT) up to 256 colors (256x24-bit) per layer
- Up to 8 Input color formats selectable per layer
- Flexible blending between two layers using alpha value (per pixel or constant)
- Flexible programmable parameters for each layer
- Color keying (transparency color)
- Up to 4 programmable interrupt events.

## 2.11 Chrom-ART Accelerator™ (DMA2D)

The Chrom-Art Accelerator™ (DMA2D) is a graphic accelerator which offers advanced bit blitting, row data copy and pixel format conversion. It supports the following functions:

- Rectangle filling with a fixed color
- Rectangle copy
- Rectangle copy with pixel format conversion
- Rectangle composition with blending and pixel format conversion.

Various image format coding are supported, from indirect 4bpp color mode up to 32bpp direct color. It embeds dedicated memory to store color lookup tables.



An interrupt can be generated when an operation is complete or at a programmed watermark.

All the operations are fully automatized and are running independently from the CPU or the DMAs.

## 2.12 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 97 maskable interrupt channels plus the 16 interrupt lines of the Cortex<sup>®</sup>-M7 with FPU core.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

## 2.13 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 24 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 168 GPIOs can be connected to the 16 external interrupt lines.

## 2.14 Clocks and startup

On reset the 16 MHz internal HSI RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy. The application can then select as system clock either the RC oscillator or an external 4-26 MHz clock source. This clock can be monitored for failure. If a failure is detected, the system automatically switches back to the internal RC oscillator and a software interrupt is generated (if enabled). This clock source is input to a PLL thus allowing to increase the frequency up to 200 MHz. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example if an indirectly used external oscillator fails).

Several prescalers allow the configuration of the two AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the two AHB buses is 200 MHz while the maximum frequency of the high-speed APB domains is 100 MHz. The maximum allowed frequency of the low-speed APB domain is 50 MHz.

The devices embed two dedicated PLL (PLLI2S and PLLSAI) which allow to achieve audio class performance. In this case, the I<sup>2</sup>S and SAI master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

## 2.15 Boot modes

At startup, the boot memory space is selected by the BOOT0 pin and BOOT\_ADDx option bytes, allowing to program any boot memory address from 0x0000 0000 to 0x3FFF FFFF which includes:

- All Flash address space mapped on ITCM or AXIM interface
- All RAM address space: ITCM, DTCM RAMs and SRAMs mapped on AXIM interface
- The System memory bootloader

The boot loader is located in system memory. It is used to reprogram the Flash memory through a serial interface.

## 2.16 Power supply schemes

- $V_{DD} = 1.7$  to  $3.6$  V: external power supply for I/Os and the internal regulator (when enabled), provided externally through  $V_{DD}$  pins.
- $V_{SSA}$ ,  $V_{DDA} = 1.7$  to  $3.6$  V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL.  $V_{DDA}$  and  $V_{SSA}$  must be connected to  $V_{DD}$  and  $V_{SS}$ , respectively.
- VDDUSB can be connected either to VDD or an external independent power supply (3.0 to 3.6V) for USB transceivers. For example, when device is powered at 1.8V, an independent power supply 3.3V can be connected to VDDUSB.
- $V_{BAT} = 1.65$  to  $3.6$  V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when  $V_{DD}$  is not present.

*Note:*  $V_{DD}/V_{DDA}$  minimum value of 1.7 V is obtained when the internal reset is OFF (refer to [Section 2.17.2: Internal reset OFF](#)). Refer to [Table 3: Voltage regulator configuration mode versus device operating mode](#) to identify the packages supporting this option.

## 2.17 Power supply supervisor

### 2.17.1 Internal reset ON

On packages embedding the PDR\_ON pin, the power supply supervisor is enabled by holding PDR\_ON high. On the other packages, the power supply supervisor is always enabled.

The device has an integrated power-on reset (POR)/ power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry. At power-on, POR/PDR is always active and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is reached, the option byte loading process starts, either to confirm or modify default BOR thresholds, or to disable BOR permanently. Three BOR thresholds are available through option bytes. The device remains in reset mode when  $V_{DD}$  is below a specified threshold,  $V_{POR/PDR}$  or  $V_{BOR}$ , without the need for an external reset circuit.

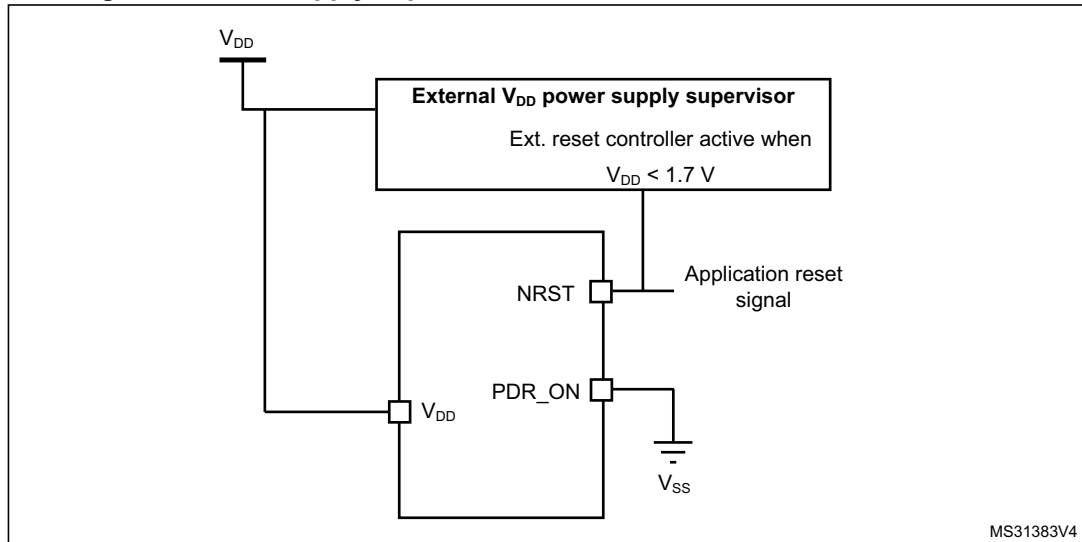
The device also features an embedded programmable voltage detector (PVD) that monitors the  $V_{DD}/V_{DDA}$  power supply and compares it to the  $V_{PVD}$  threshold. An interrupt can be generated when  $V_{DD}/V_{DDA}$  drops below the  $V_{PVD}$  threshold and/or when  $V_{DD}/V_{DDA}$  is higher than the  $V_{PVD}$  threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

### 2.17.2 Internal reset OFF

This feature is available only on packages featuring the PDR\_ON pin. The internal power-on reset (POR) / power-down reset (PDR) circuitry is disabled through the PDR\_ON pin.

An external power supply supervisor should monitor  $V_{DD}$  and NRST and should maintain the device in reset mode as long as  $V_{DD}$  is below a specified threshold. PDR\_ON should be connected to  $V_{SS}$ . Refer to [Figure 4: Power supply supervisor interconnection with internal reset OFF](#).

**Figure 4. Power supply supervisor interconnection with internal reset OFF**



The  $V_{DD}$  specified threshold, below which the device must be maintained under reset, is 1.7 V (see [Figure 5](#)).

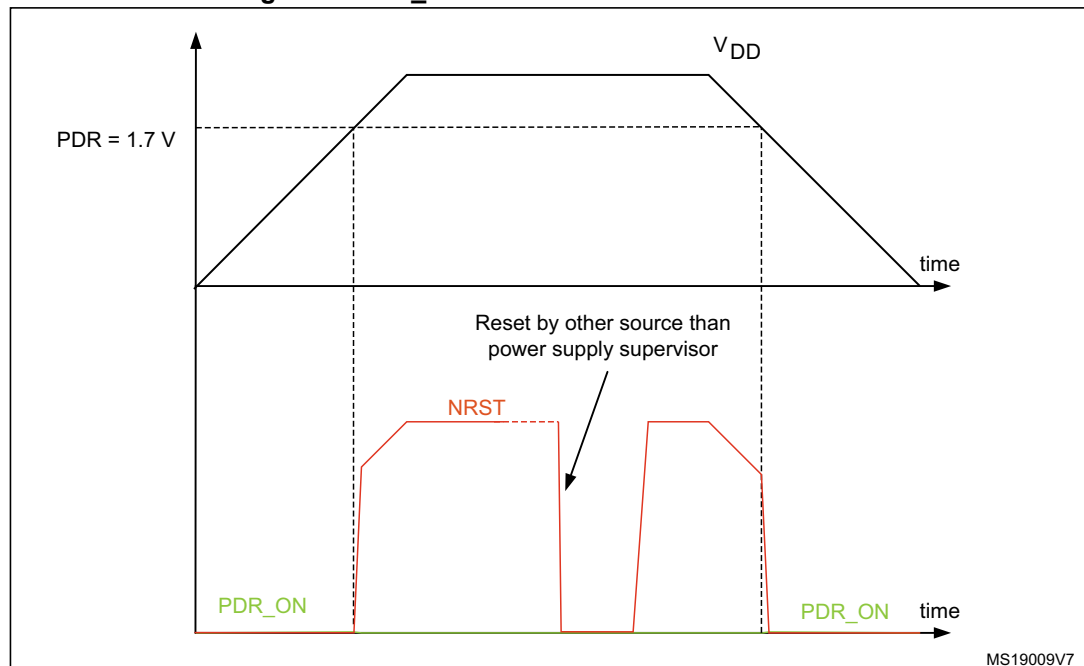
A comprehensive set of power-saving mode allows to design low-power applications.

When the internal reset is OFF, the following integrated features are no more supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled
- The brownout reset (BOR) circuitry must be disabled
- The embedded programmable voltage detector (PVD) is disabled
- $V_{BAT}$  functionality is no more available and  $V_{BAT}$  pin should be connected to  $V_{DD}$ .

All packages, except for the LQFP100, allow to disable the internal reset through the PDR\_ON signal when connected to  $V_{SS}$ .

Figure 5. PDR\_ON control with internal reset OFF



## 2.18 Voltage regulator

The regulator has four operating modes:

- Regulator ON
  - Main regulator mode (MR)
  - Low power regulator (LPR)
  - Power-down
- Regulator OFF

### 2.18.1 Regulator ON

On packages embedding the BYPASS\_REG pin, the regulator is enabled by holding BYPASS\_REG low. On all other packages, the regulator is always enabled.

There are three power modes configured by software when the regulator is ON:

- MR mode used in Run/sleep modes or in Stop modes
  - In Run/Sleep mode
 

The MR mode is used either in the normal mode (default mode) or the over-drive mode (enabled by software). Different voltages scaling are provided to reach the best compromise between maximum frequency and dynamic power consumption.

The over-drive mode allows operating at a higher frequency than the normal mode for a given voltage scaling.

- In Stop modes

The MR can be configured in two ways during stop mode:

MR operates in normal mode (default mode of MR in stop mode)

MR operates in under-drive mode (reduced leakage mode).

- LPR is used in the Stop modes:

The LP regulator mode is configured by software when entering Stop mode.

Like the MR mode, the LPR can be configured in two ways during stop mode:

- LPR operates in normal mode (default mode when LPR is ON)
- LPR operates in under-drive mode (reduced leakage mode).

- Power-down is used in Standby mode.

The Power-down mode is activated only when entering in Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost.

Refer to [Table 3](#) for a summary of voltage regulator modes versus device operating modes.

Two external ceramic capacitors should be connected on  $V_{CAP\_1}$  and  $V_{CAP\_2}$  pin.

All packages have the regulator ON feature.

**Table 3. Voltage regulator configuration mode versus device operating mode<sup>(1)</sup>**

| Voltage regulator configuration | Run mode | Sleep mode | Stop mode | Standby mode |
|---------------------------------|----------|------------|-----------|--------------|
| Normal mode                     | MR       | MR         | MR or LPR | -            |
| Over-drive mode <sup>(2)</sup>  | MR       | MR         | -         | -            |
| Under-drive mode                | -        | -          | MR or LPR | -            |
| Power-down mode                 | -        | -          | -         | Yes          |

1. '-' means that the corresponding configuration is not available.

2. The over-drive mode is not available when  $V_{DD} = 1.7$  to  $2.1$  V.

## 2.18.2 Regulator OFF

This feature is available only on packages featuring the `BYPASS_REG` pin. The regulator is disabled by holding `BYPASS_REG` high. The regulator OFF mode allows to supply externally a  $V_{12}$  voltage source through  $V_{CAP\_1}$  and  $V_{CAP\_2}$  pins.

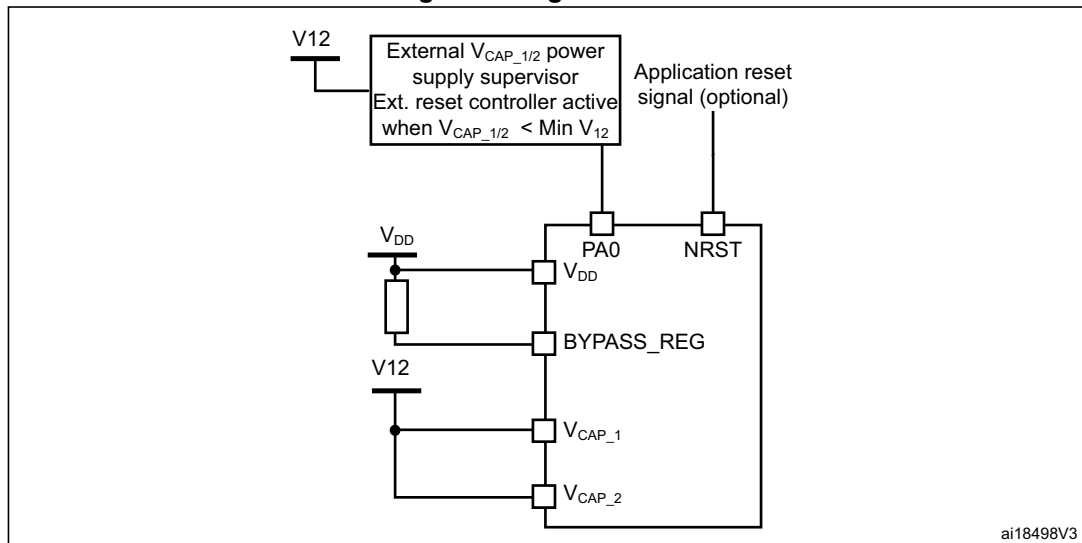
Since the internal voltage scaling is not managed internally, the external voltage value must be aligned with the targeted maximum frequency. The two  $2.2\ \mu\text{F}$  ceramic capacitors should be replaced by two  $100\ \text{nF}$  decoupling capacitors.

When the regulator is OFF, there is no more internal monitoring on  $V_{12}$ . An external power supply supervisor should be used to monitor the  $V_{12}$  of the logic power domain. `PA0` pin should be used for this purpose, and act as power-on reset on  $V_{12}$  power domain.

In regulator OFF mode, the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset a part of the  $V_{12}$  logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used under power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection under reset or pre-reset is required.
- The over-drive and under-drive modes are not available.
- The Standby mode is not available.

**Figure 6. Regulator OFF**

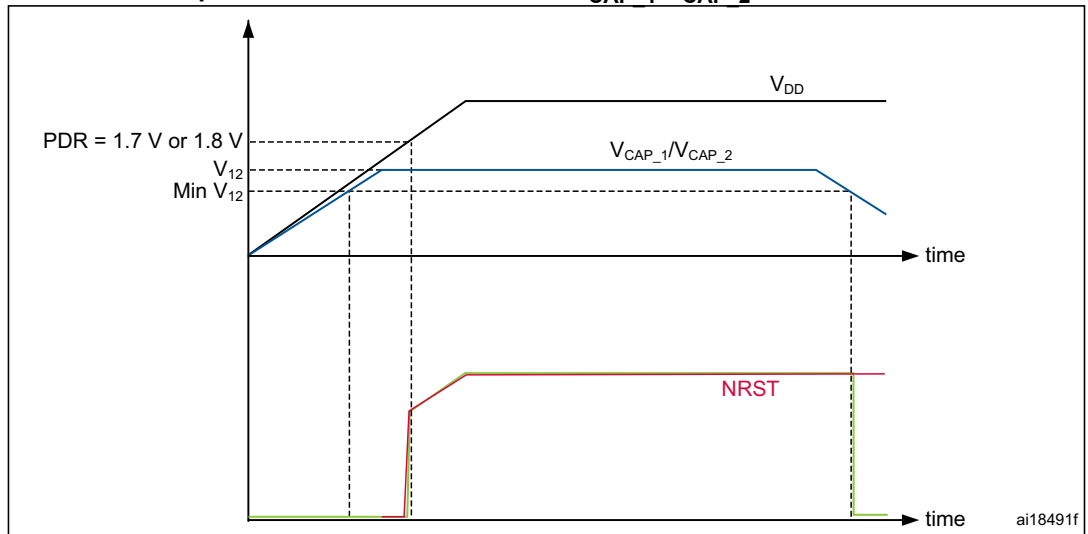


The following conditions must be respected:

- $V_{DD}$  should always be higher than  $V_{CAP\_1}$  and  $V_{CAP\_2}$  to avoid current injection between power domains.
- If the time for  $V_{CAP\_1}$  and  $V_{CAP\_2}$  to reach  $V_{12}$  minimum value is faster than the time for  $V_{DD}$  to reach 1.7 V, then PA0 should be kept low to cover both conditions: until  $V_{CAP\_1}$  and  $V_{CAP\_2}$  reach  $V_{12}$  minimum value and until  $V_{DD}$  reaches 1.7 V (see [Figure 7](#)).
- Otherwise, if the time for  $V_{CAP\_1}$  and  $V_{CAP\_2}$  to reach  $V_{12}$  minimum value is slower than the time for  $V_{DD}$  to reach 1.7 V, then PA0 could be asserted low externally (see [Figure 8](#)).
- If  $V_{CAP\_1}$  and  $V_{CAP\_2}$  go below  $V_{12}$  minimum value and  $V_{DD}$  is higher than 1.7 V, then a reset must be asserted on PA0 pin.

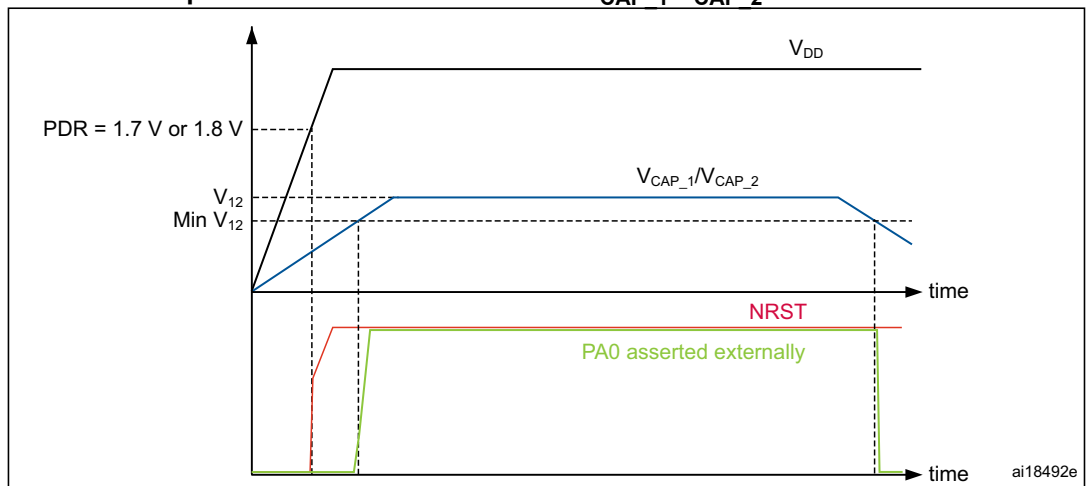
**Note:** The minimum value of  $V_{12}$  depends on the maximum frequency targeted in the application.

**Figure 7. Startup in regulator OFF: slow  $V_{DD}$  slope  
- power-down reset risen after  $V_{CAP\_1}/V_{CAP\_2}$  stabilization**



1. This figure is valid whatever the internal reset mode (ON or OFF).

**Figure 8. Startup in regulator OFF mode: fast  $V_{DD}$  slope  
- power-down reset risen before  $V_{CAP\_1}/V_{CAP\_2}$  stabilization**



1. This figure is valid whatever the internal reset mode (ON or OFF).

### 2.18.3 Regulator ON/OFF and internal reset ON/OFF availability

**Table 4. Regulator ON/OFF and internal reset ON/OFF availability**

| Package                                        | Regulator ON                         | Regulator OFF                        | Internal reset ON                | Internal reset OFF               |
|------------------------------------------------|--------------------------------------|--------------------------------------|----------------------------------|----------------------------------|
| LQFP100                                        | Yes                                  | No                                   | Yes                              | No                               |
| LQFP144,<br>LQFP208                            |                                      |                                      | Yes<br>PDR_ON set to<br>$V_{DD}$ | Yes<br>PDR_ON set to<br>$V_{SS}$ |
| LQFP176,<br>WLCSP143,<br>UFBGA176,<br>TFBGA216 | Yes<br>BYPASS_REG set<br>to $V_{SS}$ | Yes<br>BYPASS_REG set<br>to $V_{DD}$ |                                  |                                  |

## 2.19 Real-time clock (RTC), backup SRAM and backup registers

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to  $V_{BAT}$  mode.
- 17-bit auto-reload wakeup timer (WUT) for periodic events with programmable resolution and period.

The RTC and the 32 backup registers are supplied through a switch that takes power either from the  $V_{DD}$  supply when present or from the  $V_{BAT}$  pin.

The backup registers are 32-bit registers used to store 128 bytes of user application data when  $V_{DD}$  power is not present. They are not reset by a system or power reset, or when the device wakes up from Standby mode.

The RTC clock sources can be:

- A 32.768 kHz external crystal (LSE)
- An external resonator or oscillator (LSE)
- The internal low power RC oscillator (LSI, with typical frequency of 32 kHz)
- The high-speed external clock (HSE) divided by 32.



The RTC is functional in  $V_{BAT}$  mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in  $V_{BAT}$  mode, but is functional in all low-power modes.

All RTC events (Alarm, WakeUp Timer, Timestamp or Tamper) can generate an interrupt and wakeup the device from the low-power modes.

## 2.20 Low-power modes

The devices support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

The Stop mode achieves the lowest power consumption while retaining the contents of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled.

The voltage regulator can be put either in main regulator mode (MR) or in low-power mode (LPR). Both modes can be configured as follows (see [Table 5: Voltage regulator modes in stop mode](#)):

- Normal mode (default mode when MR or LPR is enabled)
- Under-drive mode.

The device can be woken up from the Stop mode by any of the EXTI line (the EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm / wakeup / tamper / time stamp events, the USB OTG FS/HS wakeup or the Ethernet wakeup and LPTIM1 asynchronous interrupt).

**Table 5. Voltage regulator modes in stop mode**

| Voltage regulator configuration | Main regulator (MR)    | Low-power regulator (LPR) |
|---------------------------------|------------------------|---------------------------|
| Normal mode                     | MR ON                  | LPR ON                    |
| Under-drive mode                | MR in under-drive mode | LPR in under-drive mode   |

- **Standby mode**

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, the SRAM and register contents are lost except for registers in the backup domain and the backup SRAM when selected.

The device exits the Standby mode when an external reset (NRST pin), an IWDG reset, a rising or falling edge on one of the 6 WKUP pins (PA0, PA2, PC1, PC13, PI8, PI11), or an RTC alarm / wakeup / tamper /time stamp event occurs.

The standby mode is not supported when the embedded voltage regulator is bypassed and the 1.2 V domain is controlled by an external power.

## 2.21 V<sub>BAT</sub> operation

The V<sub>BAT</sub> pin allows to power the device V<sub>BAT</sub> domain from an external battery, an external supercapacitor, or from V<sub>DD</sub> when no external battery and an external supercapacitor are present.

V<sub>BAT</sub> operation is activated when V<sub>DD</sub> is not present.

The V<sub>BAT</sub> pin supplies the RTC, the backup registers and the backup SRAM.

*Note: When the microcontroller is supplied from V<sub>BAT</sub>, external interrupts and RTC alarm/events do not exit it from V<sub>BAT</sub> operation.*

*When PDR\_ON pin is connected to V<sub>SS</sub> (Internal Reset OFF), the V<sub>BAT</sub> functionality is no more available and V<sub>BAT</sub> pin should be connected to V<sub>DD</sub>.*

## 2.22 Timers and watchdogs

The devices include two advanced-control timers, eight general-purpose timers, two basic timers and two watchdog timers.

All timer counters can be frozen in debug mode.

[Table 6](#) compares the features of the advanced-control, general-purpose and basic timers.

Table 6. Timer feature comparison

| Timer type       | Timer        | Counter resolution | Counter type      | Prescaler factor                | DMA request generation | Capture/compare channels | Complementary output | Max interface clock (MHz) | Max timer clock (MHz) <sup>(1)</sup> |
|------------------|--------------|--------------------|-------------------|---------------------------------|------------------------|--------------------------|----------------------|---------------------------|--------------------------------------|
| Advanced-control | TIM1, TIM8   | 16-bit             | Up, Down, Up/down | Any integer between 1 and 65536 | Yes                    | 4                        | Yes                  | 100                       | 200                                  |
| General purpose  | TIM2, TIM5   | 32-bit             | Up, Down, Up/down | Any integer between 1 and 65536 | Yes                    | 4                        | No                   | 50                        | 100/200                              |
|                  | TIM3, TIM4   | 16-bit             | Up, Down, Up/down | Any integer between 1 and 65536 | Yes                    | 4                        | No                   | 50                        | 100/200                              |
|                  | TIM9         | 16-bit             | Up                | Any integer between 1 and 65536 | No                     | 2                        | No                   | 100                       | 200                                  |
|                  | TIM10, TIM11 | 16-bit             | Up                | Any integer between 1 and 65536 | No                     | 1                        | No                   | 100                       | 200                                  |
|                  | TIM12        | 16-bit             | Up                | Any integer between 1 and 65536 | No                     | 2                        | No                   | 50                        | 100/200                              |
|                  | TIM13, TIM14 | 16-bit             | Up                | Any integer between 1 and 65536 | No                     | 1                        | No                   | 50                        | 100/200                              |
| Basic            | TIM6, TIM7   | 16-bit             | Up                | Any integer between 1 and 65536 | Yes                    | 0                        | No                   | 50                        | 100/200                              |

1. The maximum timer clock is either 100 or 200 MHz depending on TIMPRE bit configuration in the RCC\_DCKCFGR register.

### 2.22.1 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1, TIM8) can be seen as three-phase PWM generators multiplexed on 6 channels. They have complementary PWM outputs with programmable

inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100%).

The advanced-control timer can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

TIM1 and TIM8 support independent DMA request generation.

### 2.22.2 General-purpose timers (TIMx)

There are ten synchronizable general-purpose timers embedded in the STM32F756xx devices (see [Table 6](#) for differences).

- **TIM2, TIM3, TIM4, TIM5**

The STM32F756xx include 4 full-featured general-purpose timers: TIM2, TIM5, TIM3, and TIM4. The TIM2 and TIM5 timers are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. The TIM3 and TIM4 timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

The TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8 via the Timer Link feature for synchronization or event chaining.

Any of these general-purpose timers can be used to generate PWM outputs.

TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

- **TIM9, TIM10, TIM11, TIM12, TIM13, and TIM14**

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10, TIM11, TIM13, and TIM14 feature one independent channel, whereas TIM9 and TIM12 have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers. They can also be used as simple time bases.

### 2.22.3 Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger and waveform generation. They can also be used as a generic 16-bit time base.

TIM6 and TIM7 support independent DMA request generation.

### 2.22.4 Low-power timer (LPTIM1)

The low-power timer has an independent clock and is running also in Stop mode if it is clocked by LSE, LSI or an external clock. It is able to wakeup the devices from Stop mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous / one-shot mode
- Selectable software / hardware input trigger
- Selectable clock source:
  - Internal clock source: LSE, LSI, HSI or APB clock
  - External clock source over LPTIM input (working even with no internal clock source running, used by the Pulse Counter Application)
- Programmable digital glitch filter
- Encoder mode

### 2.22.5 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

### 2.22.6 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

### 2.22.7 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

## 2.23 Inter-integrated circuit interface (I<sup>2</sup>C)

The device embeds 4 I2C. Refer to table [Table 7: I2C implementation](#) for the features implementation.

The I<sup>2</sup>C bus interface handles communications between the microcontroller and the serial I<sup>2</sup>C bus. It controls all I<sup>2</sup>C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- I<sup>2</sup>C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System Management Bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (Packet Error Checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power System Management Protocol (PMBus<sup>TM</sup>) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming.
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

**Table 7. I2C implementation**

| I2C features <sup>(1)</sup>                   | I2C1 | I2C2 | I2C3 | I2C4 |
|-----------------------------------------------|------|------|------|------|
| Standard-mode (up to 100 kbit/s)              | X    | X    | X    | X    |
| Fast-mode (up to 400 kbit/s)                  | X    | X    | X    | X    |
| Programmable analog and digital noise filters | X    | X    | X    | X    |
| SMBus/PMBus hardware support                  | X    | X    | X    | X    |
| Independent clock                             | X    | X    | X    | X    |

1. X: supported

## 2.24 Universal synchronous/asynchronous receiver transmitters (USART)

The device embeds USART. Refer to [Table 8: USART implementation](#) for the features implementation.

The universal synchronous asynchronous receiver transmitter (USART) offers a flexible means of full-duplex data exchange with external equipment requiring an industry standard NRZ asynchronous serial data format.

The USART peripheral supports:

- Full-duplex asynchronous communications
- Configurable oversampling method by 16 or 8 to give flexibility between speed and clock tolerance
- Dual clock domain allowing convenient baud rate programming independent from the PCLK reprogramming
- A common programmable transmit and receive baud rate of up to 12.5 Mbit/s when the clock frequency is 100 MHz and oversampling is by 8.
- Auto baud rate detection
- Programmable data word length (7 or 8 or 9 bits) word length
- Programmable data order with MSB-first or LSB-first shifting
- Programmable parity (odd, even, no parity)
- Configurable stop bits (1 or 1.5 or 2 stop bits)
- Synchronous mode and clock output for synchronous communications
- Single-wire half-duplex communications
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration
- Hardware flow control for modem and RS-485 transceiver
- Multiprocessor communications
- LIN master synchronous break send capability and LIN slave break detection capability
- IrDA SIR encoder decoder supporting 3/16 bit duration for normal mode
- Smartcard mode ( T=0 and T=1 asynchronous protocols for Smartcards as defined in the ISO/IEC 7816-3 standard )
- Support for Modbus communication

The table below summarizes the implementation of all U(S)ARTs instances

**Table 8. USART implementation**

| features <sup>(1)</sup>               | USART1/2/3/6    | UART4/5/7/8 |
|---------------------------------------|-----------------|-------------|
| Data Length                           | 7, 8 and 9 bits |             |
| Hardware flow control for modem       | X               | X           |
| Continuous communication using DMA    | X               | X           |
| Multiprocessor communication          | X               | X           |
| Synchronous mode                      | X               |             |
| Smartcard mode                        | X               |             |
| Single-wire half-duplex communication | X               | X           |
| IrDA SIR ENDEC block                  | X               | X           |
| LIN mode                              | X               | X           |
| Dual clock domain                     | X               | X           |
| Receiver timeout interrupt            | X               | X           |
| Modbus communication                  | X               | X           |

Table 8. USART implementation (continued)

| features <sup>(1)</sup>  | USART1/2/3/6 | UART4/5/7/8 |
|--------------------------|--------------|-------------|
| Auto baud rate detection | X            | X           |
| Driver Enable            | X            | X           |

1. X: supported

## 2.25 Serial peripheral interface (SPI)/inter- integrated sound interfaces (I2S)

The devices feature up to six SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1, SPI4, SPI5, and SPI6 can communicate at up to 50 Mbits/s, SPI2 and SPI3 can communicate at up to 25 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable from 4 to 16 bits. The SPI interfaces support NSS pulse mode, TI mode and Hardware CRC calculation. All SPIs can be served by the DMA controller.

Three standard I<sup>2</sup>S interfaces (multiplexed with SPI1, SPI2 and SPI3) are available. They can be operated in master or slave mode, in simplex communication modes, and can be configured to operate with a 16-/32-bit resolution as an input or output channel. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I<sup>2</sup>S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

All I2Sx can be served by the DMA controller.

## 2.26 Serial audio interface (SAI)

The devices embed two serial audio interfaces.

The serial audio interface is based on two independent audio subblocks which can operate as transmitter or receiver with their FIFO. Many audio protocols are supported by each block: I2S standards, LSB or MSB-justified, PCM/DSP, TDM, AC'97 and SPDIF output, supporting audio sampling frequencies from 8 kHz up to 192 kHz. Both subblocks can be configured in master or in slave mode.

In master mode, the master clock can be output to the external DAC/CODEC at 256 times of the sampling frequency.

The two sub-blocks can be configured in synchronous mode when full-duplex mode is required.

SAI1 and SAI2 can be served by the DMA controller

## 2.27 SPDIF-RX Receiver Interface (SPDIF-RX)

The SPDIF-RX peripheral, is designed to receive an S/PDIF flow compliant with IEC-60958 and IEC-61937. These standards support simple stereo streams up to high sample rate, and compressed multi-channel surround sound, such as those defined by Dolby or DTS (up to 5.1).



The main features of the SPDIF-RX are the following:

- Up to 4 inputs available
- Automatic symbol rate detection
- Maximum symbol rate: 12.288 MHz
- Stereo stream from 32 to 192 kHz supported
- Supports Audio IEC-60958 and IEC-61937, consumer applications
- Parity bit management
- Communication using DMA for audio samples
- Communication using DMA for control and user channel information
- Interrupt capabilities

The SPDIF-RX receiver provides all the necessary features to detect the symbol rate, and decode the incoming data stream. The user can select the wanted SPDIF input, and when a valid signal will be available, the SPDIF-RX will re-sample the incoming signal, decode the manchester stream, recognize frames, sub-frames and blocks elements. It delivers to the CPU decoded data, and associated status flags.

The SPDIF-RX also offers a signal named `spdif_frame_sync`, which toggles at the S/PDIF sub-frame rate that will be used to compute the exact sample rate for clock drift algorithms.

## 2.28 Audio PLL (PLLI2S)

The devices feature an additional dedicated PLL for audio I<sup>2</sup>S and SAI applications. It allows to achieve error-free I<sup>2</sup>S sampling clock accuracy without compromising on the CPU performance, while using USB peripherals.

The PLLI2S configuration can be modified to manage an I<sup>2</sup>S/SAI sample rate change without disabling the main PLL (PLL) used for CPU, USB and Ethernet interfaces.

The audio PLL can be programmed with very low error to obtain sampling rates ranging from 8 KHz to 192 KHz.

In addition to the audio PLL, a master clock input pin can be used to synchronize the I<sup>2</sup>S/SAI flow with an external PLL (or Codec output).

## 2.29 Audio and LCD PLL(PLLSAI)

An additional PLL dedicated to audio and LCD-TFT is used for SAI1 peripheral in case the PLLI2S is programmed to achieve another audio sampling frequency (49.152 MHz or 11.2896 MHz) and the audio application requires both sampling frequencies simultaneously.

The PLLSAI is also used to generate the LCD-TFT clock.

## 2.30 SD/SDIO/MMC card host interface (SDMMC)

An SDMMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit.

The interface allows data transfer at up to 50 MHz, and is compliant with the SD Memory Card Specification Version 2.0.

The SDMMC Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDMMC/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

The SDMMC can be served by the DMA controller

## 2.31 Ethernet MAC interface with dedicated DMA and IEEE 1588 support

The devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard medium-independent interface (MII) or a reduced medium-independent interface (RMII). The microcontroller requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). The PHY is connected to the device MII port using 17 signals for MII or 9 signals for RMII, and can be clocked using the 25 MHz (MII) from the microcontroller.

The devices include the following features:

- Supports 10 and 100 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 2 Kbytes.
- Supports hardware PTP (precision time protocol) in accordance with IEEE 1588 2008 (PTP V2) with the time stamp comparator connected to the TIM2 input
- Triggers interrupt when system time becomes greater than target time

## 2.32 Controller area network (bxCAN)

The two CANs are compliant with the 2.0A and B (active) specifications with a bitrate up to 1 Mbit/s. They can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three transmit mailboxes, two receive FIFOs with 3 stages and 28 shared scalable filter banks (all of them can be used even if one CAN is used). 256 bytes of SRAM are allocated for each CAN.

## 2.33 Universal serial bus on-the-go full-speed (OTG\_FS)

The device embeds an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 2.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The major features are:

- Combined Rx and Tx FIFO size of 1.28 KB with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 1 bidirectional control endpoint + 5 IN endpoints + 5 OUT endpoints
- 12 host channels with periodic OUT support
- Software configurable to OTG1.3 and OTG2.0 modes of operation
- USB 2.0 LPM (Link Power Management) support
- Internal FS OTG PHY support
- HNP/SNP/IP inside (no need for any external resistor)

For OTG/Host modes, a power switch is needed in case bus-powered devices are connected

## 2.34 Universal serial bus on-the-go high-speed (OTG\_HS)

The device embeds a USB OTG high-speed (up to 480 Mb/s) device/host/OTG peripheral. The USB OTG HS supports both full-speed and high-speed operations. It integrates the transceivers for full-speed operation (12 MB/s) and features a UTMI low-pin interface (ULPI) for high-speed operation (480 MB/s). When using the USB OTG HS in HS mode, an external PHY device connected to the ULPI is required.

The USB OTG HS peripheral is compliant with the USB 2.0 specification and with the OTG 2.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The major features are:

- Combined Rx and Tx FIFO size of 4 KB with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 8 bidirectional endpoints
- 16 host channels with periodic OUT support
- Software configurable to OTG1.3 and OTG2.0 modes of operation
- USB 2.0 LPM (Link Power Management) support
- Internal FS OTG PHY support
- External HS or HS OTG operation supporting ULPI in SDR mode. The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.
- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- for OTG/Host modes, a power switch is needed in case bus-powered devices are connected

## 2.35 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The device embeds a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI-CEC controller to wakeup the MCU from Stop mode on data reception.

## 2.36 Digital camera interface (DCMI)

The devices embed a camera interface that can connect with camera modules and CMOS sensors through an 8-bit to 14-bit parallel interface, to receive video data. The camera interface can sustain a data transfer rate up to 54 Mbyte/s at 54 MHz. It features:

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication can be 8-, 10-, 12- or 14-bit
- Supports 8-bit progressive video monochrome or raw bayer format, YCbCr 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Supports continuous mode or snapshot (a single frame) mode
- Capability to automatically crop the image

## 2.37 Cryptographic acceleration

The devices embed a cryptographic accelerator. This cryptographic accelerator provides a set of hardware acceleration for the advanced cryptographic algorithms usually needed to provide confidentiality, authentication, data integrity and non repudiation when exchanging messages with a peer.

- These algorithms consists of:
  - Encryption/Decryption
    - DES/TDES (data encryption standard/triple data encryption standard): ECB (electronic codebook) and CBC (cipher block chaining) chaining algorithms, 64-, 128- or 192-bit key
    - AES (advanced encryption standard): ECB, CBC, GCM, CCM, and CTR (counter mode) chaining algorithms, 128, 192 or 256-bit key
  - Universal hash
    - SHA-1 and SHA-2 (secure hash algorithms)
    - MD5
    - HMAC

The cryptographic accelerator supports DMA request generation.

## 2.38 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

## 2.39 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allowing maximum I/O toggling up to 100 MHz.

## 2.40 Analog-to-digital converters (ADCs)

Three 12-bit analog-to-digital converters are embedded and each ADC shares up to 16 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold

The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM2, TIM3, TIM4, TIM5, or TIM8 timer.

## 2.41 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 1.7 V and 3.6 V. The temperature sensor is internally connected to the same input channel as  $V_{BAT}$ , ADC1\_IN18, which is used to convert the sensor output voltage into a digital value. When the temperature sensor and  $V_{BAT}$  conversion are enabled at the same time, only  $V_{BAT}$  conversion is performed.

As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part should be used.

## 2.42 Digital-to-analog converter (DAC)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference  $V_{REF+}$

Eight DAC trigger inputs are used in the device. The DAC channels are triggered through the timer update outputs that are also connected to different DMA streams.

## 2.43 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

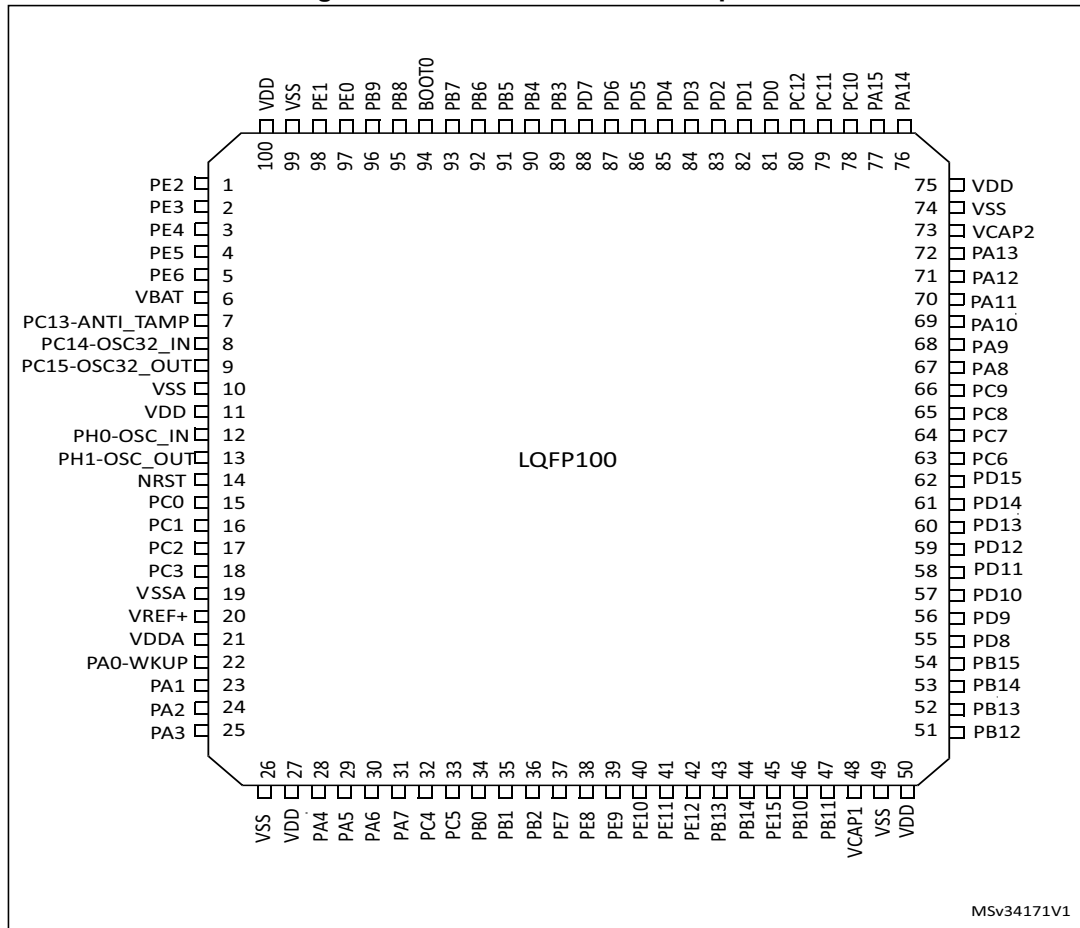
## 2.44 Embedded Trace Macrocell™

The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F756xx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

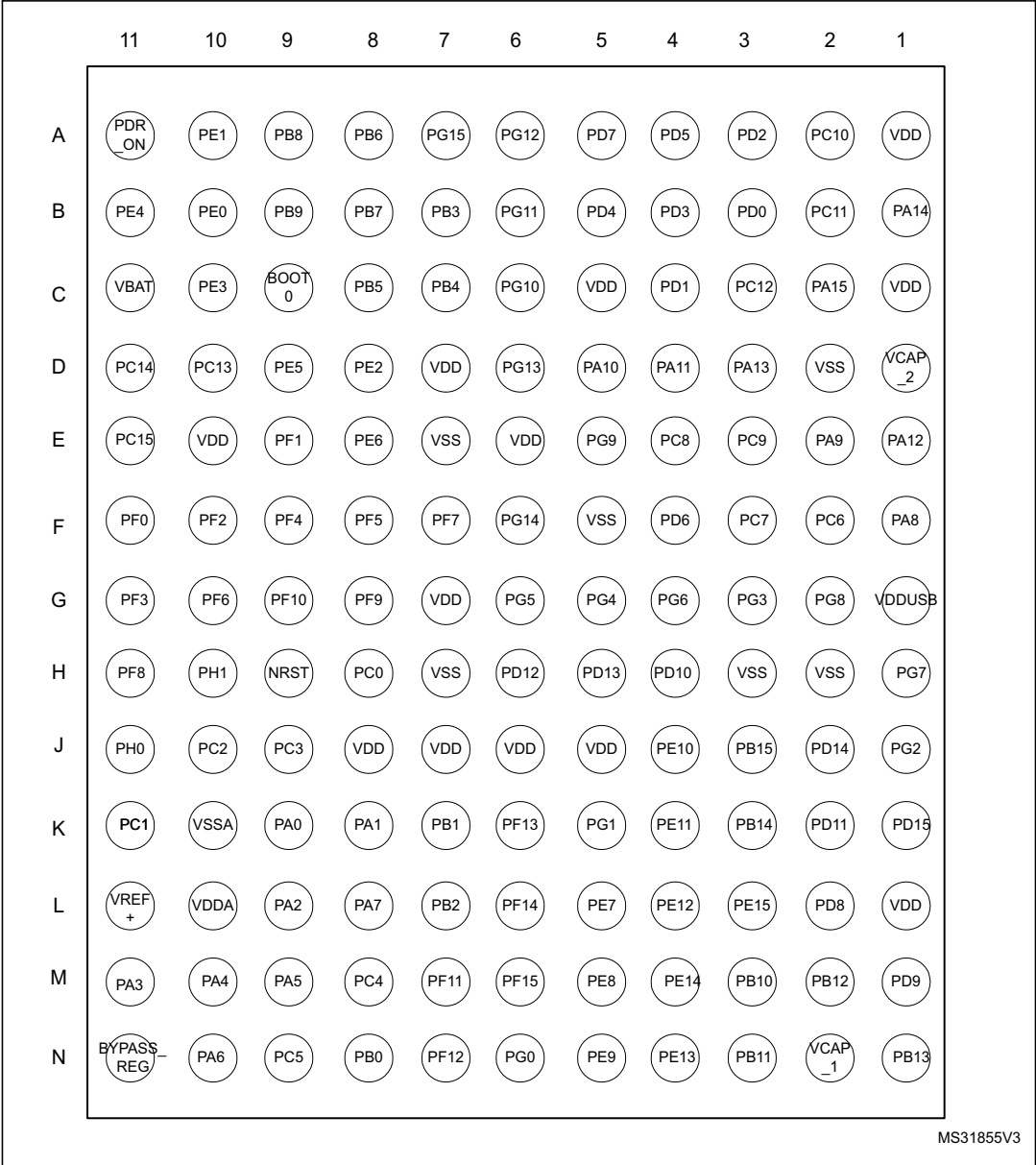
### 3 Pinouts and pin description

Figure 9. STM32F756xx LQFP100 pinout



1. The above figure shows the package top view.

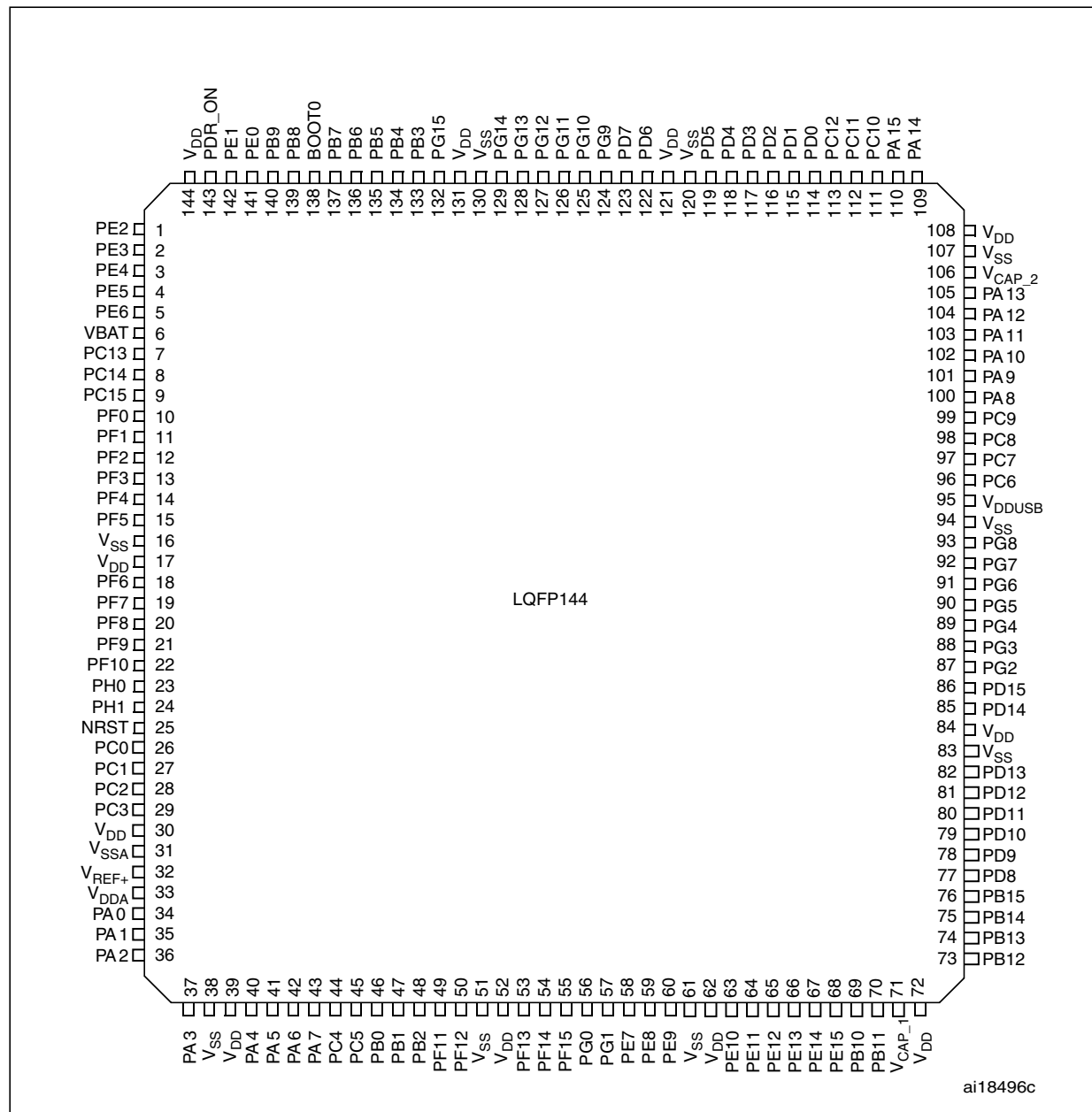
Figure 10. STM32F756xx WLCSP143 ballout



The above figure shows the package bump view.



**Figure 11. STM32F756xx LQFP144 pinout**

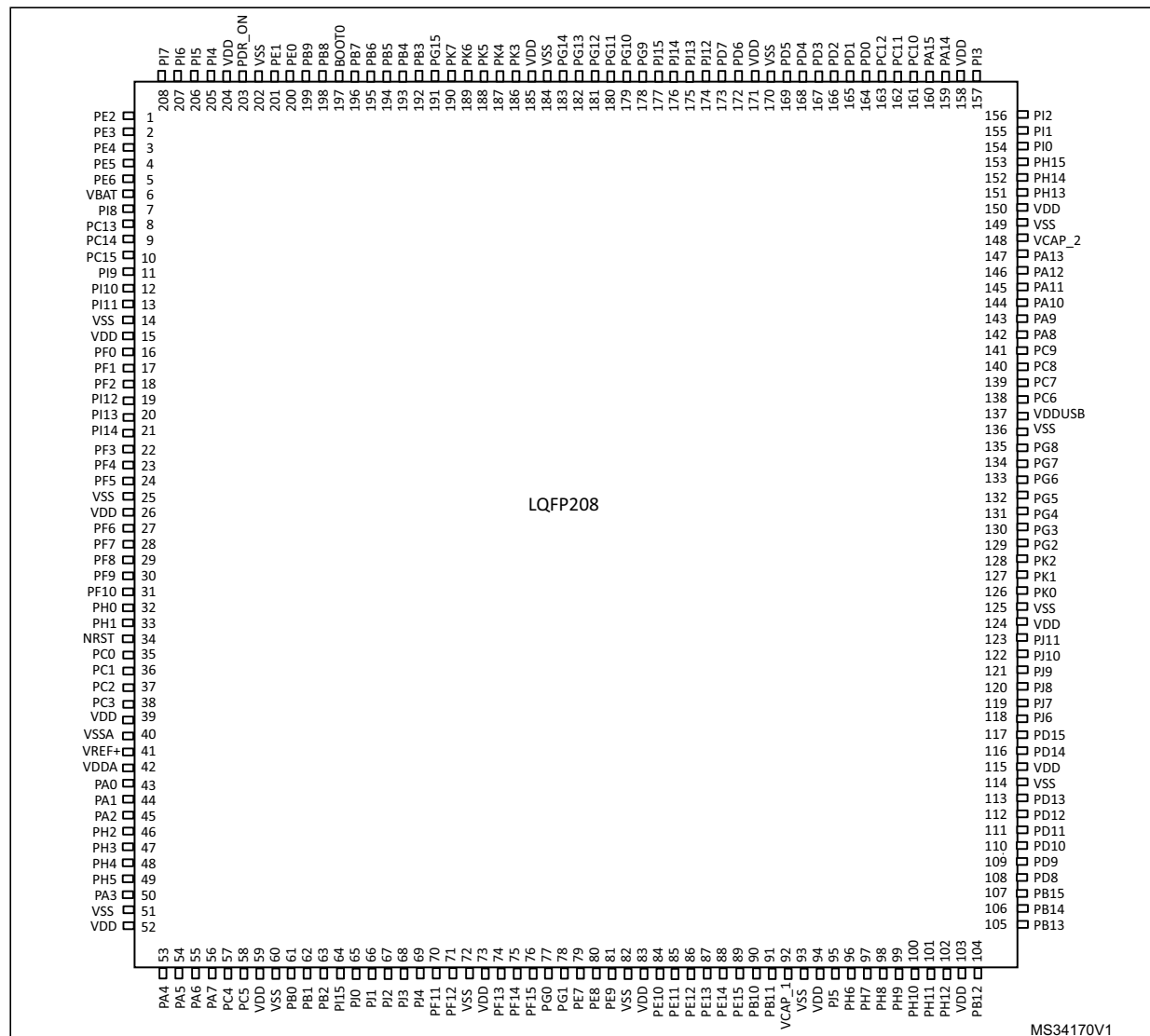


1. The above figure shows the package top view.

MS31878V2

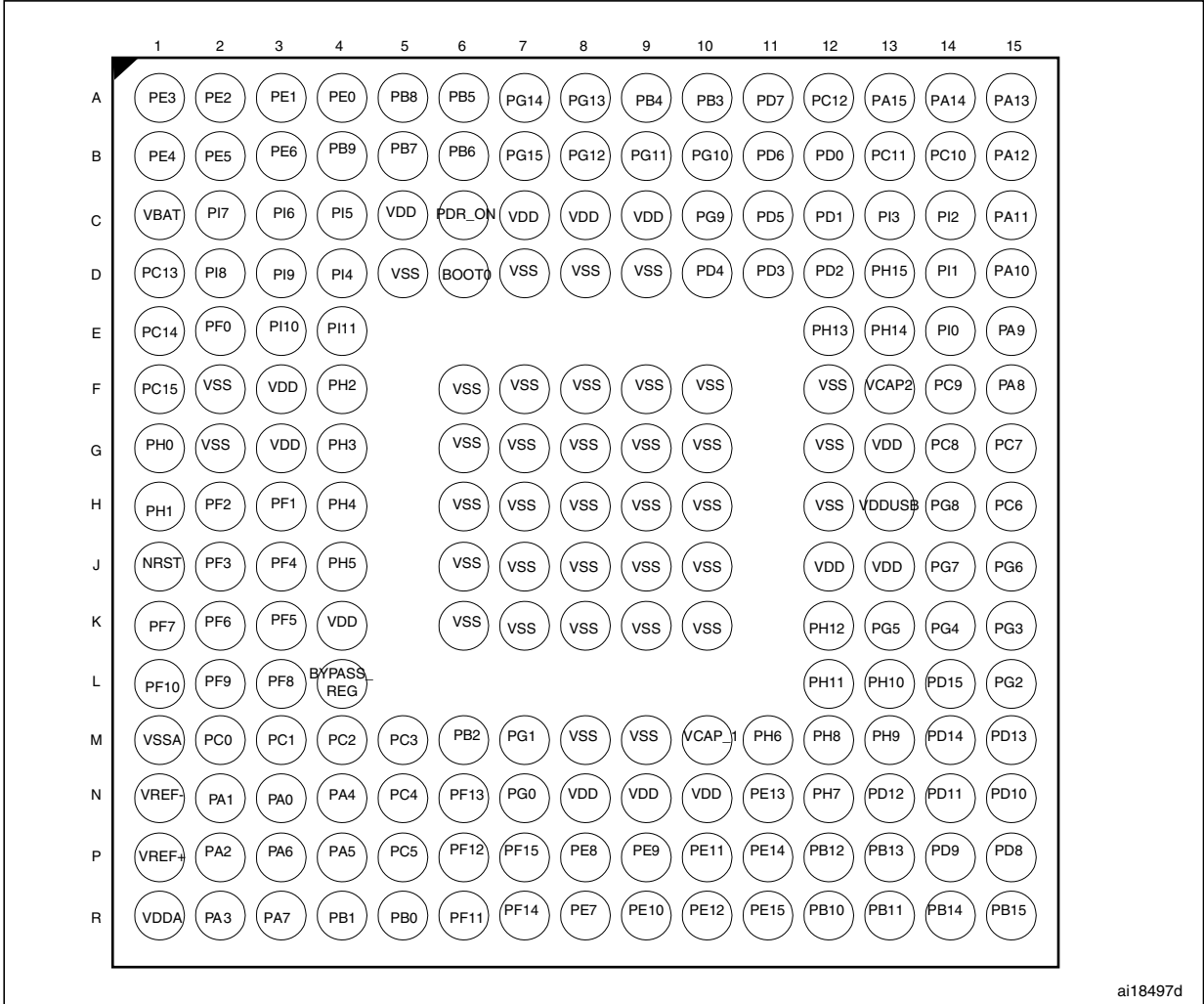
MS31878V2

Figure 13. STM32F756xx LQFP208 pinout



1. The above figure shows the package top view.

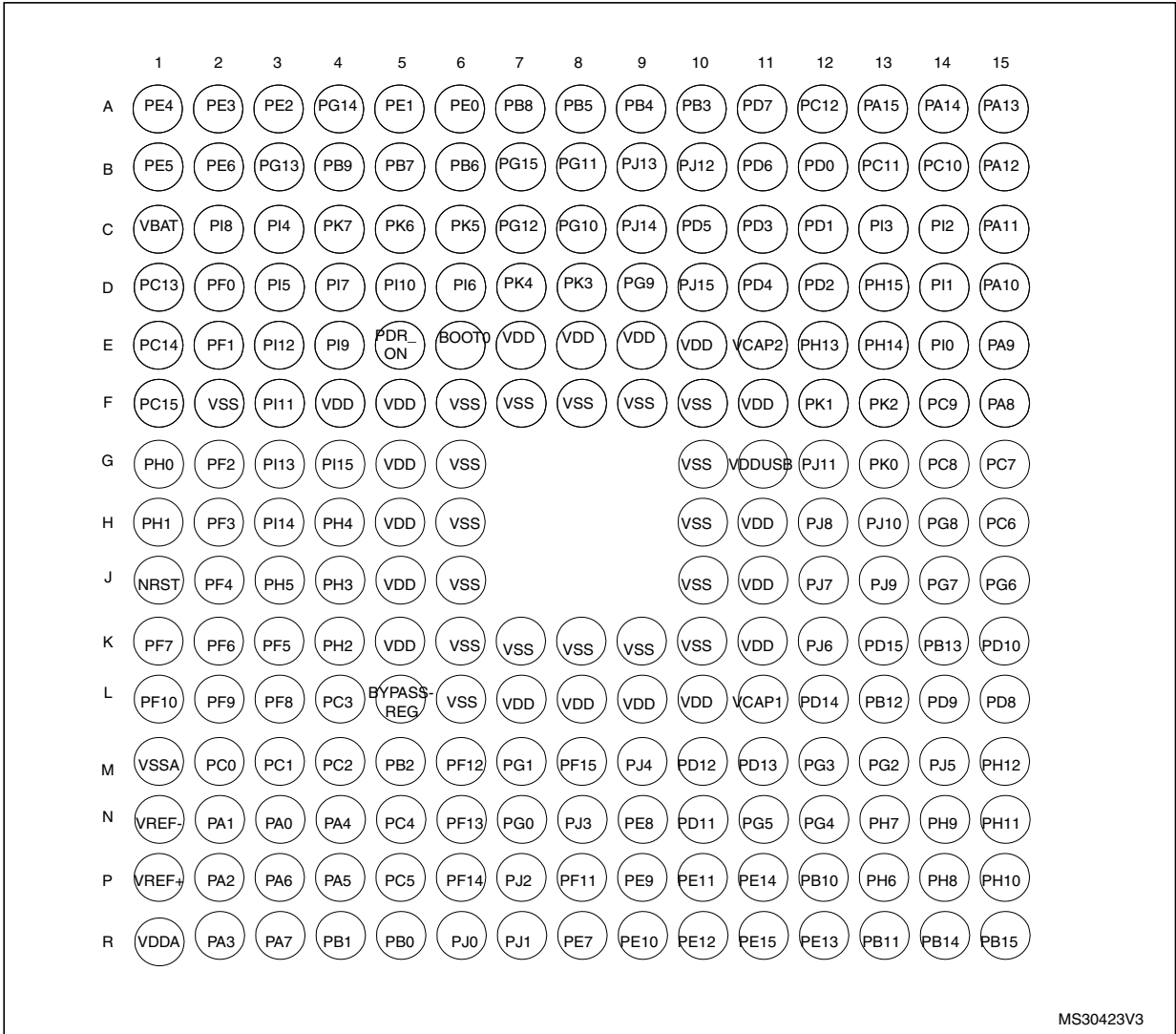
Figure 14. STM32F756xx UFBGA176 ballout



ai18497d

1. The above figure shows the package top view.

Figure 15. STM32F756xx TFBGA216 ballout



MS30423V3

1. The above figure shows the package top view.

Table 9. Legend/abbreviations used in the pinout table

| Name                 | Abbreviation                                                                                                                          | Definition                                         |
|----------------------|---------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------|
| Pin name             | Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name |                                                    |
| Pin type             | S                                                                                                                                     | Supply pin                                         |
|                      | I                                                                                                                                     | Input only pin                                     |
|                      | I/O                                                                                                                                   | Input / output pin                                 |
| I/O structure        | FT                                                                                                                                    | 5 V tolerant I/O                                   |
|                      | TTa                                                                                                                                   | 3.3 V tolerant I/O directly connected to ADC       |
|                      | B                                                                                                                                     | Dedicated BOOT0 pin                                |
|                      | RST                                                                                                                                   | Bidirectional reset pin with weak pull-up resistor |
| Notes                | Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset                                      |                                                    |
| Alternate functions  | Functions selected through GPIOx_AFR registers                                                                                        |                                                    |
| Additional functions | Functions directly selected/enabled through peripheral registers                                                                      |                                                    |

Table 10. STM32F756xx pin and ball definition

| Pin Number |          |         |          |         |         |          | Pin name<br>(function after reset) <sup>(1)</sup> | Pin type | I/O structure | Notes | Alternate functions                                                               | Additional functions |
|------------|----------|---------|----------|---------|---------|----------|---------------------------------------------------|----------|---------------|-------|-----------------------------------------------------------------------------------|----------------------|
| LQFP100    | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 |                                                   |          |               |       |                                                                                   |                      |
| 1          | D8       | 1       | A2       | 1       | 1       | A3       | PE2                                               | I/O      | FT            | -     | TRACECLK, SPI4_SCK, SAI1_MCLK_A, QUADSPI_BK1_IO2, ETH_MII_TXD3, FMC_A23, EVENTOUT | -                    |
| 2          | C10      | 2       | A1       | 2       | 2       | A2       | PE3                                               | I/O      | FT            | -     | TRACED0, SAI1_SD_B, FMC_A19, EVENTOUT                                             | -                    |
| 3          | B11      | 3       | B1       | 3       | 3       | A1       | PE4                                               | I/O      | FT            | -     | TRACED1, SPI4_NSS, SAI1_FS_A, FMC_A20, DCMI_D4, LCD_B0, EVENTOUT                  | -                    |

Table 10. STM32F756xx pin and ball definition (continued)

| Pin Number |          |         |          |         |         |          | Pin name<br>(function after reset) <sup>(1)</sup> | Pin type | I/O structure | Notes      | Alternate functions                                                                                 | Additional functions                   |
|------------|----------|---------|----------|---------|---------|----------|---------------------------------------------------|----------|---------------|------------|-----------------------------------------------------------------------------------------------------|----------------------------------------|
| LQFP100    | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 |                                                   |          |               |            |                                                                                                     |                                        |
| 4          | D9       | 4       | B2       | 4       | 4       | B1       | PE5                                               | I/O      | FT            | -          | TRACED2, TIM9_CH1, SPI4_MISO, SAI1_SCK_A, FMC_A21, DCMI_D6, LCD_G0, EVENTOUT                        | -                                      |
| 5          | E8       | 5       | B3       | 5       | 5       | B2       | PE6                                               | I/O      | FT            | -          | TRACED3, TIM1_BKIN2, TIM9_CH2, SPI4_MOSI, SAI1_SD_A, SAI2_MCK_B, FMC_A22, DCMI_D7, LCD_G1, EVENTOUT | -                                      |
| -          | -        | -       | -        | -       | -       | G6       | VSS                                               | S        | -             | -          | -                                                                                                   | -                                      |
| -          | -        | -       | -        | -       | -       | F5       | VDD                                               | S        | -             | -          | -                                                                                                   | -                                      |
| 6          | C11      | 6       | C1       | 6       | 6       | C1       | VBAT                                              | S        | -             | -          | -                                                                                                   | -                                      |
| -          | -        | -       | D2       | 7       | 7       | C2       | PI8                                               | I/O      | FT            | (2)<br>(3) | EVENTOUT                                                                                            | RTC_TAMP2/<br>RTC_TS, WKUP3            |
| 7          | D10      | 7       | D1       | 8       | 8       | D1       | PC13                                              | I/O      | FT            | (2)<br>(3) | EVENTOUT                                                                                            | RTC_TAMP1/<br>RTC_TS/RTC_OUT,<br>WKUP2 |
| 8          | D11      | 8       | E1       | 9       | 9       | E1       | PC14-<br>OSC32_I<br>N(PC14)                       | I/O      | FT            | (2)<br>(3) | EVENTOUT                                                                                            | OSC32_IN                               |
| 9          | E11      | 9       | F1       | 10      | 10      | F1       | PC15-<br>OSC32_<br>OUT(PC<br>15)                  | I/O      | FT            | (2)<br>(3) | EVENTOUT                                                                                            | OSC32_OUT                              |
| -          | -        | -       | -        | -       | -       | F2       | VSS                                               | S        | -             | -          | -                                                                                                   | -                                      |
| -          | -        | -       | -        | -       | -       | G5       | VDD                                               | S        | -             | -          | -                                                                                                   | -                                      |
| -          | -        | -       | D3       | 11      | 11      | E4       | PI9                                               | I/O      | FT            | -          | CAN1_RX, FMC_D30, LCD_VSYNC, EVENTOUT                                                               | -                                      |
| -          | -        | -       | E3       | 12      | 12      | D5       | PI10                                              | I/O      | FT            | -          | ETH_MII_RX_ER, FMC_D31, LCD_HSYNC, EVENTOUT                                                         | -                                      |

Table 10. STM32F756xx pin and ball definition (continued)

| Pin Number |          |         |          |         |         |          | Pin name<br>(function after reset) <sup>(1)</sup> | Pin type | I/O structure | Notes | Alternate functions                                                   | Additional functions |
|------------|----------|---------|----------|---------|---------|----------|---------------------------------------------------|----------|---------------|-------|-----------------------------------------------------------------------|----------------------|
| LQFP100    | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 |                                                   |          |               |       |                                                                       |                      |
| -          | -        | -       | E4       | 13      | 13      | F3       | PI11                                              | I/O      | FT            | -     | OTG_HS_ULPI_DIR, EVENTOUT                                             | WKUP4                |
| -          | E7       | -       | F2       | 14      | 14      | F2       | VSS                                               | S        | -             | -     | -                                                                     | -                    |
| -          | E10      | -       | F3       | 15      | 15      | F4       | VDD                                               | S        | -             | -     | -                                                                     | -                    |
| -          | F11      | 10      | E2       | 16      | 16      | D2       | PF0                                               | I/O      | FT            | -     | I2C2_SDA, FMC_A0, EVENTOUT                                            | -                    |
| -          | E9       | 11      | H3       | 17      | 17      | E2       | PF1                                               | I/O      | FT            | -     | I2C2_SCL, FMC_A1, EVENTOUT                                            | -                    |
| -          | F10      | 12      | H2       | 18      | 18      | G2       | PF2                                               | I/O      | FT            | -     | I2C2_SMBA, FMC_A2, EVENTOUT                                           | -                    |
| -          | -        | -       | -        | -       | 19      | E3       | PI12                                              | I/O      | FT            | -     | LCD_HSYNC, EVENTOUT                                                   | -                    |
| -          | -        | -       | -        | -       | 20      | G3       | PI13                                              | I/O      | FT            | -     | LCD_VSYNC, EVENTOUT                                                   | -                    |
| -          | -        | -       | -        | -       | 21      | H3       | PI14                                              | I/O      | FT            | -     | LCD_CLK, EVENTOUT                                                     | -                    |
| -          | G11      | 13      | J2       | 19      | 22      | H2       | PF3                                               | I/O      | FT            | -     | FMC_A3, EVENTOUT                                                      | ADC3_IN9             |
| -          | F9       | 14      | J3       | 20      | 23      | J2       | PF4                                               | I/O      | FT            | -     | FMC_A4, EVENTOUT                                                      | ADC3_IN14            |
| -          | F8       | 15      | K3       | 21      | 24      | K3       | PF5                                               | I/O      | FT            | -     | FMC_A5, EVENTOUT                                                      | ADC3_IN15            |
| 10         | H7       | 16      | G2       | 22      | 25      | H6       | VSS                                               | S        | -             | -     | -                                                                     | -                    |
| 11         | -        | 17      | G3       | 23      | 26      | H5       | VDD                                               | S        | -             | -     | -                                                                     | -                    |
| -          | G10      | 18      | K2       | 24      | 27      | K2       | PF6                                               | I/O      | FT            | -     | TIM10_CH1, SPI5_NSS, SAI1_SD_B, UART7_Rx, QUADSPI_BK1_IO3, EVENTOUT   | ADC3_IN4             |
| -          | F7       | 19      | K1       | 25      | 28      | K1       | PF7                                               | I/O      | FT            | -     | TIM11_CH1, SPI5_SCK, SAI1_MCLK_B, UART7_Tx, QUADSPI_BK1_IO2, EVENTOUT | ADC3_IN5             |



Table 10. STM32F756xx pin and ball definition (continued)

| Pin Number |          |         |          |         |         |          | Pin name<br>(function after reset) <sup>(1)</sup> | Pin type | I/O structure | Notes | Alternate functions                                                                   | Additional functions                |
|------------|----------|---------|----------|---------|---------|----------|---------------------------------------------------|----------|---------------|-------|---------------------------------------------------------------------------------------|-------------------------------------|
| LQFP100    | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 |                                                   |          |               |       |                                                                                       |                                     |
| -          | H11      | 20      | L3       | 26      | 29      | L3       | PF8                                               | I/O      | FT            | -     | SPI5_MISO,<br>SAI1_SCK_B,<br>UART7_RTS,<br>TIM13_CH1,<br>QUADSPI_BK1_IO0,<br>EVENTOUT | ADC3_IN6                            |
| -          | G8       | 21      | L2       | 27      | 30      | L2       | PF9                                               | I/O      | FT            | -     | SPI5_MOSI, SAI1_FS_B,<br>UART7_CTS,<br>TIM14_CH1,<br>QUADSPI_BK1_IO1,<br>EVENTOUT     | ADC3_IN7                            |
| -          | G9       | 22      | L1       | 28      | 31      | L1       | PF10                                              | I/O      | FT            | -     | DCMI_D11, LCD_DE,<br>EVENTOUT                                                         | ADC3_IN8                            |
| 12         | J11      | 23      | G1       | 29      | 32      | G1       | PH0-<br>OSC_IN(<br>PH0)                           | I/O      | FT            | -     | EVENTOUT                                                                              | OSC_IN <sup>(4)</sup>               |
| 13         | H10      | 24      | H1       | 30      | 33      | H1       | PH1-<br>OSC_OUT(<br>PH1)                          | I/O      | FT            | -     | EVENTOUT                                                                              | OSC_OUT <sup>(4)</sup>              |
| 14         | H9       | 25      | J1       | 31      | 34      | J1       | NRST                                              | I/O      | RS<br>T       | -     | -                                                                                     | -                                   |
| 15         | H8       | 26      | M2       | 32      | 35      | M2       | PC0                                               | I/O      | FT            | (4)   | SAI2_FS_B,<br>OTG_HS_ULPI_STP,<br>FMC_SDNWE, LCD_R5,<br>EVENTOUT                      | ADC123_IN10                         |
| 16         | K11      | 27      | M3       | 33      | 36      | M3       | PC1                                               | I/O      | FT            | (4)   | TRACED0,<br>SPI2_MOSI/I2S2_SD,<br>SAI1_SD_A, ETH_MDC,<br>EVENTOUT                     | ADC123_IN11,<br>RTC_TAMP3,<br>WKUP5 |
| 17         | J10      | 28      | M4       | 34      | 37      | M4       | PC2                                               | I/O      | FT            | (4)   | SPI2_MISO,<br>OTG_HS_ULPI_DIR,<br>ETH_MII_TXD2,<br>FMC_SDNE0,<br>EVENTOUT             | ADC123_IN12                         |

Table 10. STM32F756xx pin and ball definition (continued)

| Pin Number |          |         |          |         |         |          | Pin name<br>(function after reset) <sup>(1)</sup> | Pin type | I/O structure | Notes | Alternate functions                                                                                                                            | Additional functions                |
|------------|----------|---------|----------|---------|---------|----------|---------------------------------------------------|----------|---------------|-------|------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------|
| LQFP100    | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 |                                                   |          |               |       |                                                                                                                                                |                                     |
| 18         | J9       | 29      | M5       | 35      | 38      | L4       | PC3                                               | I/O      | FT            | (4)   | SPI2_MOSI/I2S2_SD,<br>OTG_HS_ULPI_NXT,<br>ETH_MII_TX_CLK,<br>FMC_SDCKE0,<br>EVENTOUT                                                           | ADC123_IN13                         |
| -          | G7       | 30      | G3       | 36      | 39      | J5       | VDD                                               | S        | -             | -     | -                                                                                                                                              | -                                   |
| -          | -        | -       | -        | -       | -       | J6       | VSS                                               | S        | -             | -     | -                                                                                                                                              | -                                   |
| 19         | K10      | 31      | M1       | 37      | 40      | M1       | VSSA                                              | S        | -             | -     | -                                                                                                                                              | -                                   |
| -          | -        | -       | N1       | -       | -       | N1       | VREF-                                             | S        | -             | -     | -                                                                                                                                              | -                                   |
| 20         | L11      | 32      | P1       | 38      | 41      | P1       | VREF+                                             | S        | -             | -     | -                                                                                                                                              | -                                   |
| 21         | L10      | 33      | R1       | 39      | 42      | R1       | VDDA                                              | S        | -             | -     | -                                                                                                                                              | -                                   |
| 22         | K9       | 34      | N3       | 40      | 43      | N3       | PA0-<br>WKUP(PA0)                                 | I/O      | FT            | (5)   | TIM2_CH1/TIM2_ETR,<br>TIM5_CH1, TIM8_ETR,<br>USART2_CTS,<br>UART4_TX, SAI2_SD_B,<br>ETH_MII_CRS,<br>EVENTOUT                                   | ADC123_IN0,<br>WKUP0 <sup>(4)</sup> |
| 23         | K8       | 35      | N2       | 41      | 44      | N2       | PA1                                               | I/O      | FT            | (4)   | TIM2_CH2, TIM5_CH2,<br>USART2_RTS,<br>UART4_RX,<br>QUADSPI_BK1_IO3,<br>SAI2_MCK_B,<br>ETH_MII_RX_CLK/ETH_<br>RMII_REF_CLK,<br>LCD_R2, EVENTOUT | ADC123_IN1                          |
| 24         | L9       | 36      | P2       | 42      | 45      | P2       | PA2                                               | I/O      | FT            | (4)   | TIM2_CH3, TIM5_CH3,<br>TIM9_CH1, USART2_TX,<br>SAI2_SCK_B,<br>ETH_MDIO, LCD_R1,<br>EVENTOUT                                                    | ADC123_IN2,<br>WKUP1                |
| -          | -        | -       | F4       | 43      | 46      | K4       | PH2                                               | I/O      | FT            |       | LPTIM1_IN2,<br>QUADSPI_BK2_IO0,<br>SAI2_SCK_B,<br>ETH_MII_CRS,<br>FMC_SDCKE0, LCD_R0,<br>EVENTOUT                                              | -                                   |

Table 10. STM32F756xx pin and ball definition (continued)

| Pin Number |          |         |          |         |         |          | Pin name<br>(function after reset) <sup>(1)</sup> | Pin type | I/O structure | Notes | Alternate functions                                                                                          | Additional functions   |
|------------|----------|---------|----------|---------|---------|----------|---------------------------------------------------|----------|---------------|-------|--------------------------------------------------------------------------------------------------------------|------------------------|
| LQFP100    | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 |                                                   |          |               |       |                                                                                                              |                        |
| -          | -        | -       | G4       | 44      | 47      | J4       | PH3                                               | I/O      | FT            | -     | QUADSPI_BK2_IO1,<br>SAI2_MCK_B,<br>ETH_MII_COL,<br>FMC_SDNE0, LCD_R1,<br>EVENTOUT                            | -                      |
| -          | -        | -       | H4       | 45      | 48      | H4       | PH4                                               | I/O      | FT            | -     | I2C2_SCL,<br>OTG_HS_ULPI_NXT,<br>EVENTOUT                                                                    | -                      |
| -          | -        | -       | J4       | 46      | 49      | J3       | PH5                                               | I/O      | FT            | -     | I2C2_SDA, SPI5_NSS,<br>FMC_SDNWE,<br>EVENTOUT                                                                | -                      |
| 25         | M11      | 37      | R2       | 47      | 50      | R2       | PA3                                               | I/O      | FT            | (4)   | TIM2_CH4, TIM5_CH4,<br>TIM9_CH2, USART2_RX,<br>OTG_HS_ULPI_D0,<br>ETH_MII_COL, LCD_B5,<br>EVENTOUT           | ADC123_IN3             |
| 26         | -        | 38      | -        | -       | 51      | K6       | VSS                                               | S        | -             | -     | -                                                                                                            | -                      |
| -          | N11      | -       | L4       | 48      | -       | L5       | BYPASS_REG                                        | I        | FT            | -     | -                                                                                                            | -                      |
| 27         | J8       | 39      | K4       | 49      | 52      | K5       | VDD                                               | S        | -             | -     | -                                                                                                            | -                      |
| 28         | M10      | 40      | N4       | 50      | 53      | N4       | PA4                                               | I/O      | TTa           | (4)   | SPI1_NSS/I2S1_WS,<br>SPI3_NSS/I2S3_WS,<br>USART2_CK,<br>OTG_HS_SOF,<br>DCMI_HSYNC,<br>LCD_VSYNC,<br>EVENTOUT | ADC12_IN4,<br>DAC_OUT1 |
| 29         | M9       | 41      | P4       | 51      | 54      | P4       | PA5                                               | I/O      | TTa           | (4)   | TIM2_CH1/TIM2_ETR,<br>TIM8_CH1N,<br>SPI1_SCK/I2S1_CK,<br>OTG_HS_ULPI_CK,<br>LCD_R4, EVENTOUT                 | ADC12_IN5,<br>DAC_OUT2 |
| 30         | N10      | 42      | P3       | 52      | 55      | P3       | PA6                                               | I/O      | FT            | (4)   | TIM1_BKIN, TIM3_CH1,<br>TIM8_BKIN, SPI1_MISO,<br>TIM13_CH1,<br>DCMI_PIXCLK, LCD_G2,<br>EVENTOUT              | ADC12_IN6              |

Table 10. STM32F756xx pin and ball definition (continued)

| Pin Number |          |         |          |         |         |          | Pin name<br>(function after reset) <sup>(1)</sup> | Pin type | I/O structure | Notes | Alternate functions                                                                                              | Additional functions |
|------------|----------|---------|----------|---------|---------|----------|---------------------------------------------------|----------|---------------|-------|------------------------------------------------------------------------------------------------------------------|----------------------|
| LQFP100    | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 |                                                   |          |               |       |                                                                                                                  |                      |
| 31         | L8       | 43      | R3       | 53      | 56      | R3       | PA7                                               | I/O      | FT            | (4)   | TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI/I2S1_SD, TIM14_CH1, ETH_MII_RX_DV/ETH_RMII_CRS_DV, FMC_SDNWE, EVENTOUT | ADC12_IN7            |
| 32         | M8       | 44      | N5       | 54      | 57      | N5       | PC4                                               | I/O      | FT            | (4)   | I2S1_MCK, SPDIF_RX2, ETH_MII_RXD0/ETH_RMII_RXD0, FMC_SDNE0, EVENTOUT                                             | ADC12_IN14           |
| 33         | N9       | 45      | P5       | 55      | 58      | P5       | PC5                                               | I/O      | FT            | (4)   | SPDIF_RX3, ETH_MII_RXD1/ETH_RMII_RXD1, FMC_SDCKE0, EVENTOUT                                                      | ADC12_IN15           |
| -          | J7       | -       | -        | -       | 59      | L7       | VDD                                               | S        | -             | -     | -                                                                                                                | -                    |
| -          | -        | -       | -        | -       | 60      | L6       | VSS                                               | S        | -             | -     | -                                                                                                                | -                    |
| 34         | N8       | 46      | R5       | 56      | 61      | R5       | PB0                                               | I/O      | FT            | (4)   | TIM1_CH2N, TIM3_CH3, TIM8_CH2N, UART4_CTS, LCD_R3, OTG_HS_ULPI_D1, ETH_MII_RXD2, EVENTOUT                        | ADC12_IN8            |
| 35         | K7       | 47      | R4       | 57      | 62      | R4       | PB1                                               | I/O      | FT            | (4)   | TIM1_CH3N, TIM3_CH4, TIM8_CH3N, LCD_R6, OTG_HS_ULPI_D2, ETH_MII_RXD3, EVENTOUT                                   | ADC12_IN9            |
| 36         | L7       | 48      | M6       | 58      | 63      | M5       | PB2                                               | I/O      | FT            | -     | SAI1_SD_A, SPI3_MOSI/I2S3_SD, QUADSPI_CLK, EVENTOUT                                                              | -                    |
| -          | -        | -       | -        | -       | 64      | G4       | PI15                                              | I/O      | FT            | -     | LCD_R0, EVENTOUT                                                                                                 | -                    |
| -          | -        | -       | -        | -       | 65      | R6       | PJ0                                               | I/O      | FT            | -     | LCD_R1, EVENTOUT                                                                                                 | -                    |
| -          | -        | -       | -        | -       | 66      | R7       | PJ1                                               | I/O      | FT            | -     | LCD_R2, EVENTOUT                                                                                                 | -                    |
| -          | -        | -       | -        | -       | 67      | P7       | PJ2                                               | I/O      | FT            | -     | LCD_R3, EVENTOUT                                                                                                 | -                    |

Table 10. STM32F756xx pin and ball definition (continued)

| Pin Number |          |         |          |         |         |          | Pin name<br>(function after reset) <sup>(1)</sup> | Pin type | I/O structure | Notes | Alternate functions                                              | Additional functions |
|------------|----------|---------|----------|---------|---------|----------|---------------------------------------------------|----------|---------------|-------|------------------------------------------------------------------|----------------------|
| LQFP100    | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 |                                                   |          |               |       |                                                                  |                      |
| -          | -        | -       | -        | -       | 68      | N8       | PJ3                                               | I/O      | FT            | -     | LCD_R4, EVENTOUT                                                 | -                    |
| -          | -        | -       | -        | -       | 69      | M9       | PJ4                                               | I/O      | FT            | -     | LCD_R5, EVENTOUT                                                 | -                    |
| -          | M7       | 49      | R6       | 59      | 70      | P8       | PF11                                              | I/O      | FT            | -     | SPI5_MOSI, SAI2_SD_B,<br>FMC_SDNRAS,<br>DCMI_D12, EVENTOUT       | -                    |
| -          | N7       | 50      | P6       | 60      | 71      | M6       | PF12                                              | I/O      | FT            | -     | FMC_A6, EVENTOUT                                                 | -                    |
| -          | -        | 51      | M8       | 61      | 72      | K7       | VSS                                               | S        | -             | -     | -                                                                | -                    |
| -          | -        | 52      | N8       | 62      | 73      | L8       | VDD                                               | S        | -             | -     | -                                                                | -                    |
| -          | K6       | 53      | N6       | 63      | 74      | N6       | PF13                                              | I/O      | FT            | -     | I2C4_SMBA, FMC_A7,<br>EVENTOUT                                   | -                    |
| -          | L6       | 54      | R7       | 64      | 75      | P6       | PF14                                              | I/O      | FT            | -     | I2C4_SCL, FMC_A8,<br>EVENTOUT                                    | -                    |
| -          | M6       | 55      | P7       | 65      | 76      | M8       | PF15                                              | I/O      | FT            | -     | I2C4_SDA, FMC_A9,<br>EVENTOUT                                    | -                    |
| -          | N6       | 56      | N7       | 66      | 77      | N7       | PG0                                               | I/O      | FT            | -     | FMC_A10, EVENTOUT                                                | -                    |
| -          | K5       | 57      | M7       | 67      | 78      | M7       | PG1                                               | I/O      | FT            | -     | FMC_A11, EVENTOUT                                                | -                    |
| 37         | L5       | 58      | R8       | 68      | 79      | R8       | PE7                                               | I/O      | FT            | -     | TIM1_ETR, UART7_Rx,<br>QUADSPI_BK2_IO0,<br>FMC_D4, EVENTOUT      | -                    |
| 38         | M5       | 59      | P8       | 69      | 80      | N9       | PE8                                               | I/O      | FT            | -     | TIM1_CH1N, UART7_Tx,<br>QUADSPI_BK2_IO1,<br>FMC_D5, EVENTOUT     | -                    |
| 39         | N5       | 60      | P9       | 70      | 81      | P9       | PE9                                               | I/O      | FT            | -     | TIM1_CH1, UART7_RTS,<br>QUADSPI_BK2_IO2,<br>FMC_D6, EVENTOUT     | -                    |
| -          | H3       | 61      | M9       | 71      | 82      | K8       | VSS                                               | S        | -             | -     | -                                                                | -                    |
| -          | J5       | 62      | N9       | 72      | 83      | L9       | VDD                                               | S        | -             | -     | -                                                                | -                    |
| 40         | J4       | 63      | R9       | 73      | 84      | R9       | PE10                                              | I/O      | FT            | -     | TIM1_CH2N,<br>UART7_CTS,<br>QUADSPI_BK2_IO3,<br>FMC_D7, EVENTOUT | -                    |
| 41         | K4       | 64      | P10      | 74      | 85      | P10      | PE11                                              | I/O      | FT            | -     | TIM1_CH2, SPI4_NSS,<br>SAI2_SD_B, FMC_D8,<br>LCD_G3, EVENTOUT    | -                    |

Table 10. STM32F756xx pin and ball definition (continued)

| Pin Number |          |         |          |         |         |          | Pin name<br>(function after reset) <sup>(1)</sup> | Pin type | I/O structure | Notes | Alternate functions                                                                              | Additional functions |
|------------|----------|---------|----------|---------|---------|----------|---------------------------------------------------|----------|---------------|-------|--------------------------------------------------------------------------------------------------|----------------------|
| LQFP100    | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 |                                                   |          |               |       |                                                                                                  |                      |
| 42         | L4       | 65      | R10      | 75      | 86      | R10      | PE12                                              | I/O      | FT            | -     | TIM1_CH3N, SPI4_SCK, SAI2_SCK_B, FMC_D9, LCD_B4, EVENTOUT                                        | -                    |
| 43         | N4       | 66      | N11      | 76      | 87      | R12      | PE13                                              | I/O      | FT            | -     | TIM1_CH3, SPI4_MISO, SAI2_FS_B, FMC_D10, LCD_DE, EVENTOUT                                        | -                    |
| 44         | M4       | 67      | P11      | 77      | 88      | P11      | PE14                                              | I/O      | FT            | -     | TIM1_CH4, SPI4_MOSI, SAI2_MCK_B, FMC_D11, LCD_CLK, EVENTOUT                                      | -                    |
| 45         | L3       | 68      | R11      | 78      | 89      | R11      | PE15                                              | I/O      | FT            | -     | TIM1_BKIN, FMC_D12, LCD_R7, EVENTOUT                                                             | -                    |
| 46         | M3       | 69      | R12      | 79      | 90      | P12      | PB10                                              | I/O      | FT            | -     | TIM2_CH3, I2C2_SCL, SPI2_SCK/I2S2_CK, USART3_TX, OTG_HS_ULPI_D3, ETH_MII_RX_ER, LCD_G4, EVENTOUT | -                    |
| 47         | N3       | 70      | R13      | 80      | 91      | R13      | PB11                                              | I/O      | FT            | -     | TIM2_CH4, I2C2_SDA, USART3_RX, OTG_HS_ULPI_D4, ETH_MII_TX_EN/ETH_R MII_TX_EN, LCD_G5, EVENTOUT   | -                    |
| 48         | N2       | 71      | M10      | 81      | 92      | L11      | VCAP_1                                            | S        | -             | -     | -                                                                                                | -                    |
| 49         | H2       | -       | -        | -       | 93      | K9       | VSS                                               | S        | -             | -     | -                                                                                                | -                    |
| 50         | J6       | 72      | N10      | 82      | 94      | L10      | VDD                                               | S        | -             | -     | -                                                                                                | -                    |
| -          | -        | -       | -        | -       | 95      | M14      | PJ5                                               | I/O      | FT            | -     | LCD_R6, EVENTOUT                                                                                 | -                    |
| -          | -        | -       | M11      | 83      | 96      | P13      | PH6                                               | I/O      | FT            | -     | I2C2_SMBA, SPI5_SCK, TIM12_CH1, ETH_MII_RXD2, FMC_SDNE1, DCMI_D8, EVENTOUT                       | -                    |
| -          | -        | -       | N12      | 84      | 97      | N13      | PH7                                               | I/O      | FT            | -     | I2C3_SCL, SPI5_MISO, ETH_MII_RXD3, FMC_SDCKE1, DCMI_D9, EVENTOUT                                 | -                    |

Table 10. STM32F756xx pin and ball definition (continued)

| Pin Number |          |         |          |         |         |          | Pin name<br>(function after reset) <sup>(1)</sup> | Pin type | I/O structure | Notes | Alternate functions                                                                                                         | Additional functions |
|------------|----------|---------|----------|---------|---------|----------|---------------------------------------------------|----------|---------------|-------|-----------------------------------------------------------------------------------------------------------------------------|----------------------|
| LQFP100    | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 |                                                   |          |               |       |                                                                                                                             |                      |
| -          | -        | -       | M12      | 85      | 98      | P14      | PH8                                               | I/O      | FT            | -     | I2C3_SDA, FMC_D16, DCMI_HSYNC, LCD_R2, EVENTOUT                                                                             | -                    |
| -          | -        | -       | M13      | 86      | 99      | N14      | PH9                                               | I/O      | FT            | -     | I2C3_SMBA, TIM12_CH2, FMC_D17, DCMI_D0, LCD_R3, EVENTOUT                                                                    | -                    |
| -          | -        | -       | L13      | 87      | 100     | P15      | PH10                                              | I/O      | FT            | -     | TIM5_CH1, I2C4_SMBA, FMC_D18, DCMI_D1, LCD_R4, EVENTOUT                                                                     | -                    |
| -          | -        | -       | L12      | 88      | 101     | N15      | PH11                                              | I/O      | FT            | -     | TIM5_CH2, I2C4_SCL, FMC_D19, DCMI_D2, LCD_R5, EVENTOUT                                                                      | -                    |
| -          | -        | -       | K12      | 89      | 102     | M15      | PH12                                              | I/O      | FT            | -     | TIM5_CH3, I2C4_SDA, FMC_D20, DCMI_D3, LCD_R6, EVENTOUT                                                                      | -                    |
| -          | -        | -       | H12      | 90      | -       | K10      | VSS                                               | S        | -             | -     | -                                                                                                                           | -                    |
| -          | -        | -       | J12      | 91      | 103     | K11      | VDD                                               | S        | -             | -     | -                                                                                                                           | -                    |
| 51         | M2       | 73      | P12      | 92      | 104     | L13      | PB12                                              | I/O      | FT            | -     | TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, USART3_CK, CAN2_RX, OTG_HS_ULPI_D5, ETH_MII_TXD0/ETH_RMII_TXD0, OTG_HS_ID, EVENTOUT | -                    |
| 52         | N1       | 74      | P13      | 93      | 105     | K14      | PB13                                              | I/O      | FT            | -     | TIM1_CH1N, SPI2_SCK/I2S2_CK, USART3_CTS, CAN2_TX, OTG_HS_ULPI_D6, ETH_MII_TXD1/ETH_RMII_TXD1, EVENTOUT                      | OTG_HS_VBUS          |

Table 10. STM32F756xx pin and ball definition (continued)

| Pin Number |          |         |          |         |         |          | Pin name<br>(function after reset) <sup>(1)</sup> | Pin type | I/O structure | Notes | Alternate functions                                                                                                 | Additional functions |
|------------|----------|---------|----------|---------|---------|----------|---------------------------------------------------|----------|---------------|-------|---------------------------------------------------------------------------------------------------------------------|----------------------|
| LQFP100    | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 |                                                   |          |               |       |                                                                                                                     |                      |
| 53         | K3       | 75      | R14      | 94      | 106     | R14      | PB14                                              | I/O      | FT            | -     | TIM1_CH2N,<br>TIM8_CH2N,<br>SPI2_MISO,<br>USART3_RTS,<br>TIM12_CH1,<br>OTG_HS_DM,<br>EVENTOUT                       | -                    |
| 54         | J3       | 76      | R15      | 95      | 107     | R15      | PB15                                              | I/O      | FT            | -     | RTC_REFIN,<br>TIM1_CH3N,<br>TIM8_CH3N,<br>SPI2_MOSI/I2S2_SD,<br>TIM12_CH2,<br>OTG_HS_DP,<br>EVENTOUT                | -                    |
| 55         | L2       | 77      | P15      | 96      | 108     | L15      | PD8                                               | I/O      | FT            | -     | USART3_TX,<br>SPDIF_RX1, FMC_D13,<br>EVENTOUT                                                                       | -                    |
| 56         | M1       | 78      | P14      | 97      | 109     | L14      | PD9                                               | I/O      | FT            | -     | USART3_RX, FMC_D14,<br>EVENTOUT                                                                                     | -                    |
| 57         | H4       | 79      | N15      | 98      | 110     | K15      | PD10                                              | I/O      | FT            | -     | USART3_CK, FMC_D15,<br>LCD_B3, EVENTOUT                                                                             | -                    |
| 58         | K2       | 80      | N14      | 99      | 111     | N10      | PD11                                              | I/O      | FT            | -     | I2C4_SMBA,<br>USART3_CTS,<br>QUADSPI_BK1_IO0,<br>SAI2_SD_A,<br>FMC_A16/FMC_CLE,<br>EVENTOUT                         | -                    |
| 59         | H6       | 81      | N13      | 100     | 112     | M10      | PD12                                              | I/O      | FT            | -     | TIM4_CH1, LPTIM1_IN1,<br>I2C4_SCL,<br>USART3_RTS,<br>QUADSPI_BK1_IO1,<br>SAI2_FS_A,<br>FMC_A17/FMC_ALE,<br>EVENTOUT | -                    |
| 60         | H5       | 82      | M15      | 101     | 113     | M11      | PD13                                              | I/O      | FT            | -     | TIM4_CH2,<br>LPTIM1_OUT, I2C4_SDA,<br>QUADSPI_BK1_IO3,<br>SAI2_SCK_A, FMC_A18,<br>EVENTOUT                          | -                    |



Table 10. STM32F756xx pin and ball definition (continued)

| Pin Number |          |         |          |         |         |          | Pin name<br>(function after reset) <sup>(1)</sup> | Pin type | I/O structure | Notes | Alternate functions                             | Additional functions |
|------------|----------|---------|----------|---------|---------|----------|---------------------------------------------------|----------|---------------|-------|-------------------------------------------------|----------------------|
| LQFP100    | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 |                                                   |          |               |       |                                                 |                      |
| -          | -        | 83      | -        | 102     | 114     | J10      | VSS                                               | S        | -             | -     | -                                               | -                    |
| -          | L1       | 84      | J13      | 103     | 115     | J11      | VDD                                               | S        | -             | -     | -                                               | -                    |
| 61         | J2       | 85      | M14      | 104     | 116     | L12      | PD14                                              | I/O      | FT            | -     | TIM4_CH3, UART8_CTS, FMC_D0, EVENTOUT           | -                    |
| 62         | K1       | 86      | L14      | 105     | 117     | K13      | PD15                                              | I/O      | FT            | -     | TIM4_CH4, UART8_RTS, FMC_D1, EVENTOUT           | -                    |
| -          | -        | -       | -        | -       | 118     | K12      | PJ6                                               | I/O      | FT            | -     | LCD_R7, EVENTOUT                                | -                    |
| -          | -        | -       | -        | -       | 119     | J12      | PJ7                                               | I/O      | FT            | -     | LCD_G0, EVENTOUT                                | -                    |
| -          | -        | -       | -        | -       | 120     | H12      | PJ8                                               | I/O      | FT            | -     | LCD_G1, EVENTOUT                                | -                    |
| -          | -        | -       | -        | -       | 121     | J13      | PJ9                                               | I/O      | FT            | -     | LCD_G2, EVENTOUT                                | -                    |
| -          | -        | -       | -        | -       | 122     | H13      | PJ10                                              | I/O      | FT            | -     | LCD_G3, EVENTOUT                                | -                    |
| -          | -        | -       | -        | -       | 123     | G12      | PJ11                                              | I/O      | FT            | -     | LCD_G4, EVENTOUT                                | -                    |
| -          | -        | -       | -        | -       | 124     | H11      | VDD                                               | S        | -             | -     | -                                               | -                    |
| -          | -        | -       | -        | -       | 125     | H10      | VSS                                               | S        | -             | -     | -                                               | -                    |
| -          | -        | -       | -        | -       | 126     | G13      | PK0                                               | I/O      | FT            | -     | LCD_G5, EVENTOUT                                | -                    |
| -          | -        | -       | -        | -       | 127     | F12      | PK1                                               | I/O      | FT            | -     | LCD_G6, EVENTOUT                                | -                    |
| -          | -        | -       | -        | -       | 128     | F13      | PK2                                               | I/O      | FT            | -     | LCD_G7, EVENTOUT                                | -                    |
| -          | J1       | 87      | L15      | 106     | 129     | M13      | PG2                                               | I/O      | FT            | -     | FMC_A12, EVENTOUT                               | -                    |
| -          | G3       | 88      | K15      | 107     | 130     | M12      | PG3                                               | I/O      | FT            | -     | FMC_A13, EVENTOUT                               | -                    |
| -          | G5       | 89      | K14      | 108     | 131     | N12      | PG4                                               | I/O      | FT            | -     | FMC_A14/FMC_BA0, EVENTOUT                       | -                    |
| -          | G6       | 90      | K13      | 109     | 132     | N11      | PG5                                               | I/O      | FT            | -     | FMC_A15/FMC_BA1, EVENTOUT                       | -                    |
| -          | G4       | 91      | J15      | 110     | 133     | J15      | PG6                                               | I/O      | FT            | -     | DCMI_D12, LCD_R7, EVENTOUT                      | -                    |
| -          | H1       | 92      | J14      | 111     | 134     | J14      | PG7                                               | I/O      | FT            | -     | USART6_CK, FMC_INT, DCMI_D13, LCD_CLK, EVENTOUT | -                    |

Table 10. STM32F756xx pin and ball definition (continued)

| Pin Number |          |         |          |         |         |          | Pin name<br>(function after reset) <sup>(1)</sup> | Pin type | I/O structure | Notes | Alternate functions                                                                                   | Additional functions |
|------------|----------|---------|----------|---------|---------|----------|---------------------------------------------------|----------|---------------|-------|-------------------------------------------------------------------------------------------------------|----------------------|
| LQFP100    | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 |                                                   |          |               |       |                                                                                                       |                      |
| -          | G2       | 93      | H14      | 112     | 135     | H14      | PG8                                               | I/O      | FT            | -     | SPI6_NSS, SPDIF_RX2, USART6_RTS, ETH_PPS_OUT, FMC_SDCLK, EVENTOUT                                     | -                    |
| -          | D2       | 94      | G12      | 113     | 136     | G10      | VSS                                               | S        | -             | -     | -                                                                                                     | -                    |
| -          | G1       | 95      | H13      | 114     | 137     | G11      | VDDUSB                                            | S        | -             | -     | -                                                                                                     | -                    |
| 63         | F2       | 96      | H15      | 115     | 138     | H15      | PC6                                               | I/O      | FT            | -     | TIM3_CH1, TIM8_CH1, I2S2_MCK, USART6_TX, SDMMC_D6, DCMI_D0, LCD_HSYNC, EVENTOUT                       | -                    |
| 64         | F3       | 97      | G15      | 116     | 139     | G15      | PC7                                               | I/O      | FT            | -     | TIM3_CH2, TIM8_CH2, I2S3_MCK, USART6_RX, SDMMC_D7, DCMI_D1, LCD_G6, EVENTOUT                          | -                    |
| 65         | E4       | 98      | G14      | 117     | 140     | G14      | PC8                                               | I/O      | FT            | -     | TRACED1, TIM3_CH3, TIM8_CH3, UART5_RTS, USART6_CK, SDMMC_D0, DCMI_D2, EVENTOUT                        | -                    |
| 66         | E3       | 99      | F14      | 118     | 141     | F14      | PC9                                               | I/O      | FT            | -     | MCO2, TIM3_CH4, TIM8_CH4, I2C3_SDA, I2S_CKIN, UART5_CTS, QUADSPI_BK1_IO0, SDMMC_D1, DCMI_D3, EVENTOUT | -                    |
| 67         | F1       | 100     | F15      | 119     | 142     | F15      | PA8                                               | I/O      | FT            | -     | MCO1, TIM1_CH1, TIM8_BKIN2, I2C3_SCL, USART1_CK, OTG_FS_SOF, LCD_R6, EVENTOUT                         | -                    |
| 68         | E2       | 101     | E15      | 120     | 143     | E15      | PA9                                               | I/O      | FT            | -     | TIM1_CH2, I2C3_SMBA, SPI2_SCK/I2S2_CK, USART1_TX, DCMI_D0, EVENTOUT                                   | OTG_FS_VBUS          |

Table 10. STM32F756xx pin and ball definition (continued)

| Pin Number |          |         |          |         |         |          | Pin name<br>(function after reset) <sup>(1)</sup> | Pin type | I/O structure | Notes | Alternate functions                                                   | Additional functions |
|------------|----------|---------|----------|---------|---------|----------|---------------------------------------------------|----------|---------------|-------|-----------------------------------------------------------------------|----------------------|
| LQFP100    | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 |                                                   |          |               |       |                                                                       |                      |
| 69         | D5       | 102     | D15      | 121     | 144     | D15      | PA10                                              | I/O      | FT            | -     | TIM1_CH3, USART1_RX, OTG_FS_ID, DCMI_D1, EVENTOUT                     | -                    |
| 70         | D4       | 103     | C15      | 122     | 145     | C15      | PA11                                              | I/O      | FT            | -     | TIM1_CH4, USART1_CTS, CAN1_RX, OTG_FS_DM, LCD_R4, EVENTOUT            | -                    |
| 71         | E1       | 104     | B15      | 123     | 146     | B15      | PA12                                              | I/O      | FT            | -     | TIM1_ETR, USART1_RTS, SAI2_FS_B, CAN1_TX, OTG_FS_DP, LCD_R5, EVENTOUT | -                    |
| 72         | D3       | 105     | A15      | 124     | 147     | A15      | PA13(JT MS-SWDIO)                                 | I/O      | FT            | -     | JTMS-SWDIO, EVENTOUT                                                  | -                    |
| 73         | D1       | 106     | F13      | 125     | 148     | E11      | VCAP_2                                            | S        | -             | -     | -                                                                     | -                    |
| 74         | D2       | 107     | F12      | 126     | 149     | F10      | VSS                                               | S        | -             | -     | -                                                                     | -                    |
| 75         | C1       | 108     | G13      | 127     | 150     | F11      | VDD                                               | S        | -             | -     | -                                                                     | -                    |
| -          | -        | -       | E12      | 128     | 151     | E12      | PH13                                              | I/O      | FT            | -     | TIM8_CH1N, CAN1_TX, FMC_D21, LCD_G2, EVENTOUT                         | -                    |
| -          | -        | -       | E13      | 129     | 152     | E13      | PH14                                              | I/O      | FT            | -     | TIM8_CH2N, FMC_D22, DCMI_D4, LCD_G3, EVENTOUT                         | -                    |
| -          | -        | -       | D13      | 130     | 153     | D13      | PH15                                              | I/O      | FT            | -     | TIM8_CH3N, FMC_D23, DCMI_D11, LCD_G4, EVENTOUT                        | -                    |
| -          | -        | -       | E14      | 131     | 154     | E14      | PI0                                               | I/O      | FT            | -     | TIM5_CH4, SPI2_NSS/I2S2_WS, FMC_D24, DCMI_D13, LCD_G5, EVENTOUT       | -                    |
| -          | -        | -       | D14      | 132     | 155     | D14      | PI1                                               | I/O      | FT            | -     | TIM8_BKIN2, SPI2_SCK/I2S2_CK, FMC_D25, DCMI_D8, LCD_G6, EVENTOUT      | -                    |

Table 10. STM32F756xx pin and ball definition (continued)

| Pin Number |          |         |          |         |         |          | Pin name<br>(function after reset) <sup>(1)</sup> | Pin type | I/O structure | Notes | Alternate functions                                                                         | Additional functions |
|------------|----------|---------|----------|---------|---------|----------|---------------------------------------------------|----------|---------------|-------|---------------------------------------------------------------------------------------------|----------------------|
| LQFP100    | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 |                                                   |          |               |       |                                                                                             |                      |
| -          | -        | -       | C14      | 133     | 156     | C14      | PI2                                               | I/O      | FT            | -     | TIM8_CH4, SPI2_MISO, FMC_D26, DCMI_D9, LCD_G7, EVENTOUT                                     | -                    |
| -          | -        | -       | C13      | 134     | 157     | C13      | PI3                                               | I/O      | FT            | -     | TIM8_ETR, SPI2_MOSI/I2S2_SD, FMC_D27, DCMI_D10, EVENTOUT                                    | -                    |
| -          | F5       | -       | D9       | 135     | -       | F9       | VSS                                               | S        | -             | -     | -                                                                                           | -                    |
| -          | A1       | -       | C9       | 136     | 158     | E10      | VDD                                               | S        | -             | -     | -                                                                                           | -                    |
| 76         | B1       | 109     | A14      | 137     | 159     | A14      | PA14(JT CK-SWCLK)                                 | I/O      | FT            | -     | JTCK-SWCLK, EVENTOUT                                                                        | -                    |
| 77         | C2       | 110     | A13      | 138     | 160     | A13      | PA15(JT DI)                                       | I/O      | FT            | -     | JTDI, TIM2_CH1/TIM2_ETR, HDMI-CEC, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, UART4_RTS, EVENTOUT  | -                    |
| 78         | A2       | 111     | B14      | 139     | 161     | B14      | PC10                                              | I/O      | FT            | -     | SPI3_SCK/I2S3_CK, USART3_TX, UART4_TX, QUADSPI_BK1_IO1, SDMMC_D2, DCMI_D8, LCD_R2, EVENTOUT | -                    |
| 79         | B2       | 112     | B13      | 140     | 162     | B13      | PC11                                              | I/O      | FT            | -     | SPI3_MISO, USART3_RX, UART4_RX, QUADSPI_BK2_NCS, SDMMC_D3, DCMI_D4, EVENTOUT                | -                    |
| 80         | C3       | 113     | A12      | 141     | 163     | A12      | PC12                                              | I/O      | FT            | -     | TRACED3, SPI3_MOSI/I2S3_SD, USART3_CK, UART5_TX, SDMMC_CK, DCMI_D9, EVENTOUT                | -                    |
| 81         | B3       | 114     | B12      | 142     | 164     | B12      | PD0                                               | I/O      | FT            | -     | CAN1_RX, FMC_D2, EVENTOUT                                                                   | -                    |

Table 10. STM32F756xx pin and ball definition (continued)

| Pin Number |          |         |          |         |         |          | Pin name<br>(function after reset) <sup>(1)</sup> | Pin type | I/O structure | Notes | Alternate functions                                                                     | Additional functions |
|------------|----------|---------|----------|---------|---------|----------|---------------------------------------------------|----------|---------------|-------|-----------------------------------------------------------------------------------------|----------------------|
| LQFP100    | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 |                                                   |          |               |       |                                                                                         |                      |
| 82         | C4       | 115     | C12      | 143     | 165     | C12      | PD1                                               | I/O      | FT            | -     | CAN1_TX, FMC_D3, EVENTOUT                                                               | -                    |
| 83         | A3       | 116     | D12      | 144     | 166     | D12      | PD2                                               | I/O      | FT            | -     | TRACED2, TIM3_ETR, UART5_RX, SDMMC_CMD, DCMI_D11, EVENTOUT                              | -                    |
| 84         | B4       | 117     | D11      | 145     | 167     | C11      | PD3                                               | I/O      | FT            | -     | SPI2_SCK/I2S2_CK, USART2_CTS, FMC_CLK, DCMI_D5, LCD_G7, EVENTOUT                        | -                    |
| 85         | B5       | 118     | D10      | 146     | 168     | D11      | PD4                                               | I/O      | FT            | -     | USART2_RTS, FMC_NOE, EVENTOUT                                                           | -                    |
| 86         | A4       | 119     | C11      | 147     | 169     | C10      | PD5                                               | I/O      | FT            | -     | USART2_TX, FMC_NWE, EVENTOUT                                                            | -                    |
| -          | -        | 120     | D8       | 148     | 170     | F8       | VSS                                               | S        | -             | -     | -                                                                                       | -                    |
| -          | C5       | 121     | C8       | 149     | 171     | E9       | VDD                                               | S        | -             | -     | -                                                                                       | -                    |
| 87         | F4       | 122     | B11      | 150     | 172     | B11      | PD6                                               | I/O      | FT            | -     | SPI3_MOSI/I2S3_SD, SAI1_SD_A, USART2_RX, FMC_NWAIT, DCMI_D10, LCD_B2, EVENTOUT          | -                    |
| 88         | A5       | 123     | A11      | 151     | 173     | A11      | PD7                                               | I/O      | FT            | -     | USART2_CK, SPDIF_RX0, FMC_NE1, EVENTOUT                                                 | -                    |
| -          | -        | -       | -        | -       | 174     | B10      | PJ12                                              | I/O      | FT            | -     | LCD_B0, EVENTOUT                                                                        | -                    |
| -          | -        | -       | -        | -       | 175     | B9       | PJ13                                              | I/O      | FT            | -     | LCD_B1, EVENTOUT                                                                        | -                    |
| -          | -        | -       | -        | -       | 176     | C9       | PJ14                                              | I/O      | FT            | -     | LCD_B2, EVENTOUT                                                                        | -                    |
| -          | -        | -       | -        | -       | 177     | D10      | PJ15                                              | I/O      | FT            | -     | LCD_B3, EVENTOUT                                                                        | -                    |
| -          | E5       | 124     | C10      | 152     | 178     | D9       | PG9                                               | I/O      | FT            | -     | SPDIF_RX3, USART6_RX, QUADSPI_BK2_IO2, SAI2_FS_B, FMC_NE2/FMC_NCE, DCMI_VSYNC, EVENTOUT | -                    |

Table 10. STM32F756xx pin and ball definition (continued)

| Pin Number |          |         |          |         |         |          | Pin name<br>(function after reset) <sup>(1)</sup> | Pin type | I/O structure | Notes | Alternate functions                                                                                                                  | Additional functions |
|------------|----------|---------|----------|---------|---------|----------|---------------------------------------------------|----------|---------------|-------|--------------------------------------------------------------------------------------------------------------------------------------|----------------------|
| LQFP100    | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 |                                                   |          |               |       |                                                                                                                                      |                      |
| -          | C6       | 125     | B10      | 153     | 179     | C8       | PG10                                              | I/O      | FT            | -     | LCD_G3, SAI2_SD_B,<br>FMC_NE3, DCMI_D2,<br>LCD_B2, EVENTOUT                                                                          | -                    |
| -          | B6       | 126     | B9       | 154     | 180     | B8       | PG11                                              | I/O      | FT            | -     | SPDIF_RX0,<br>ETH_MII_TX_EN/ETH_R<br>MII_TX_EN, DCMI_D3,<br>LCD_B3, EVENTOUT                                                         | -                    |
| -          | A6       | 127     | B8       | 155     | 181     | C7       | PG12                                              | I/O      | FT            | -     | LPTIM1_IN1,<br>SPI6_MISO, SPDIF_RX1,<br>USART6_RTS, LCD_B4,<br>FMC_NE4, LCD_B1,<br>EVENTOUT                                          | -                    |
| -          | D6       | 128     | A8       | 156     | 182     | B3       | PG13                                              | I/O      | FT            | -     | TRACED0, LPTIM1_OUT,<br>SPI6_SCK,<br>USART6_CTS,<br>ETH_MII_TXD0/ETH_RM<br>II_TXD0, FMC_A24,<br>LCD_R0, EVENTOUT                     | -                    |
| -          | F6       | 129     | A7       | 157     | 183     | A4       | PG14                                              | I/O      | FT            | -     | TRACED1, LPTIM1_ETR,<br>SPI6_MOSI,<br>USART6_TX,<br>QUADSPI_BK2_IO3,<br>ETH_MII_TXD1/ETH_RM<br>II_TXD1, FMC_A25,<br>LCD_B0, EVENTOUT | -                    |
| -          | -        | 130     | D7       | 158     | 184     | F7       | VSS                                               | S        | -             | -     | -                                                                                                                                    | -                    |
| -          | E6       | 131     | C7       | 159     | 185     | E8       | VDD                                               | S        | -             | -     | -                                                                                                                                    | -                    |
| -          | -        | -       | -        | -       | 186     | D8       | PK3                                               | I/O      | FT            | -     | LCD_B4, EVENTOUT                                                                                                                     | -                    |
| -          | -        | -       | -        | -       | 187     | D7       | PK4                                               | I/O      | FT            | -     | LCD_B5, EVENTOUT                                                                                                                     | -                    |
| -          | -        | -       | -        | -       | 188     | C6       | PK5                                               | I/O      | FT            | -     | LCD_B6, EVENTOUT                                                                                                                     | -                    |
| -          | -        | -       | -        | -       | 189     | C5       | PK6                                               | I/O      | FT            | -     | LCD_B7, EVENTOUT                                                                                                                     | -                    |
| -          | -        | -       | -        | -       | 190     | C4       | PK7                                               | I/O      | FT            | -     | LCD_DE, EVENTOUT                                                                                                                     | -                    |

Table 10. STM32F756xx pin and ball definition (continued)

| Pin Number |          |         |          |         |         |          | Pin name<br>(function after reset) <sup>(1)</sup> | Pin type | I/O structure | Notes | Alternate functions                                                                                                                                  | Additional functions |
|------------|----------|---------|----------|---------|---------|----------|---------------------------------------------------|----------|---------------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|
| LQFP100    | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 |                                                   |          |               |       |                                                                                                                                                      |                      |
| -          | A7       | 132     | B7       | 160     | 191     | B7       | PG15                                              | I/O      | FT            | -     | USART6_CTS,<br>FMC_SDNCAS,<br>DCMI_D13, EVENTOUT                                                                                                     | -                    |
| 89         | B7       | 133     | A10      | 161     | 192     | A10      | PB3(JTD<br>O/TRAC<br>ESWO)                        | I/O      | FT            | -     | JTDO/TRACESWO,<br>TIM2_CH2,<br>SPI1_SCK/I2S1_CK,<br>SPI3_SCK/I2S3_CK,<br>EVENTOUT                                                                    | -                    |
| 90         | C7       | 134     | A9       | 162     | 193     | A9       | PB4(NJT<br>RST)                                   | I/O      | FT            | -     | NJTRST, TIM3_CH1,<br>SPI1_MISO, SPI3_MISO,<br>SPI2_NSS/I2S2_WS,<br>EVENTOUT                                                                          | -                    |
| 91         | C8       | 135     | A6       | 163     | 194     | A8       | PB5                                               | I/O      | FT            | -     | TIM3_CH2, I2C1_SMBA,<br>SPI1_MOSI/I2S1_SD,<br>SPI3_MOSI/I2S3_SD,<br>CAN2_RX,<br>OTG_HS_ULPI_D7,<br>ETH_PPS_OUT,<br>FMC_SDCKE1,<br>DCMI_D10, EVENTOUT | -                    |
| 92         | A8       | 136     | B6       | 164     | 195     | B6       | PB6                                               | I/O      | FT            | -     | TIM4_CH1, HDMI-CEC,<br>I2C1_SCL, USART1_TX,<br>CAN2_TX,<br>QUADSPI_BK1_NCS,<br>FMC_SDNE1, DCMI_D5,<br>EVENTOUT                                       | -                    |
| 93         | B8       | 137     | B5       | 165     | 196     | B5       | PB7                                               | I/O      | FT            | -     | TIM4_CH2, I2C1_SDA,<br>USART1_RX, FMC_NL,<br>DCMI_VSYNC,<br>EVENTOUT                                                                                 | -                    |
| 94         | C9       | 138     | D6       | 166     | 197     | E6       | BOOT0                                             | I        | B             | -     | -                                                                                                                                                    | VPP                  |
| 95         | A9       | 139     | A5       | 167     | 198     | A7       | PB8                                               | I/O      | FT            | -     | TIM4_CH3, TIM10_CH1,<br>I2C1_SCL, CAN1_RX,<br>ETH_MII_TXD3,<br>SDMMC_D4, DCMI_D6,<br>LCD_B6, EVENTOUT                                                | -                    |

Table 10. STM32F756xx pin and ball definition (continued)

| Pin Number |          |         |          |         |         |          | Pin name<br>(function after reset) <sup>(1)</sup> | Pin type | I/O structure | Notes | Alternate functions                                                                           | Additional functions |
|------------|----------|---------|----------|---------|---------|----------|---------------------------------------------------|----------|---------------|-------|-----------------------------------------------------------------------------------------------|----------------------|
| LQFP100    | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 |                                                   |          |               |       |                                                                                               |                      |
| 96         | B9       | 140     | B4       | 168     | 199     | B4       | PB9                                               | I/O      | FT            | -     | TIM4_CH4, TIM11_CH1, I2C1_SDA, SPI2_NSS/I2S2_WS, CAN1_TX, SDMMC_D5, DCMI_D7, LCD_B7, EVENTOUT | -                    |
| 97         | B10      | 141     | A4       | 169     | 200     | A6       | PE0                                               | I/O      | FT            | -     | TIM4_ETR, LPTIM1_ETR, UART8_Rx, SAI2_MCK_A, FMC_NBL0, DCMI_D2, EVENTOUT                       | -                    |
| 98         | A10      | 142     | A3       | 170     | 201     | A5       | PE1                                               | I/O      | FT            | -     | LPTIM1_IN2, UART8_Tx, FMC_NBL1, DCMI_D3, EVENTOUT                                             | -                    |
| 99         | -        | -       | D5       | -       | 202     | F6       | VSS                                               | S        | -             | -     | -                                                                                             | -                    |
| -          | A11      | 143     | C6       | 171     | 203     | E5       | PDR_ON                                            | S        | -             | -     | -                                                                                             | -                    |
| 100        | D7       | 144     | C5       | 172     | 204     | E7       | VDD                                               | S        | -             | -     | -                                                                                             | -                    |
| -          | -        | -       | D4       | 173     | 205     | C3       | PI4                                               | I/O      | FT            | -     | TIM8_BKIN, SAI2_MCK_A, FMC_NBL2, DCMI_D5, LCD_B4, EVENTOUT                                    | -                    |
| -          | -        | -       | C4       | 174     | 206     | D3       | PI5                                               | I/O      | FT            | -     | TIM8_CH1, SAI2_SCK_A, FMC_NBL3, DCMI_VSYNC, LCD_B5, EVENTOUT                                  | -                    |
| -          | -        | -       | C3       | 175     | 207     | D6       | PI6                                               | I/O      | FT            | -     | TIM8_CH2, SAI2_SD_A, FMC_D28, DCMI_D6, LCD_B6, EVENTOUT                                       | -                    |
| -          | -        | -       | C2       | 176     | 208     | D4       | PI7                                               | I/O      | FT            | -     | TIM8_CH3, SAI2_FS_A, FMC_D29, DCMI_D7, LCD_B7, EVENTOUT                                       | -                    |

1. Function availability depends on the chosen device.



2. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited:
  - The speed should not exceed 2 MHz with a maximum load of 30 pF.
  - These I/Os must not be used as a current source (e.g. to drive an LED).
3. Main function after the first backup domain power-up. Later on, it depends on the contents of the RTC registers even after reset (because these registers are not reset by the main reset). For details on how to manage these I/Os, refer to the RTC register description sections in the STM32F7xxx reference manual.
4. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).
5. If the device is delivered in an WLCSP143, UFBGA176, LQFP176 or TFBGA216 package, and the BYPASS\_REG pin is set to VDD (Regulator OFF/internal reset ON mode), then PA0 is used as an internal Reset (active low).

Table 11. FMC pin definition

| Pin name | NOR/PSRAM/SRAM | NOR/PSRAM Mux | NAND16 | SDRAM |
|----------|----------------|---------------|--------|-------|
| PF0      | A0             | -             | -      | A0    |
| PF1      | A1             | -             | -      | A1    |
| PF2      | A2             | -             | -      | A2    |
| PF3      | A3             | -             | -      | A3    |
| PF4      | A4             | -             | -      | A4    |
| PF5      | A5             | -             | -      | A5    |
| PF12     | A6             | -             | -      | A6    |
| PF13     | A7             | -             | -      | A7    |
| PF14     | A8             | -             | -      | A8    |
| PF15     | A9             | -             | -      | A9    |
| PG0      | A10            | -             | -      | A10   |
| PG1      | A11            | -             | -      | A11   |
| PG2      | A12            | -             | -      | A12   |
| PG3      | A13            | -             | -      | -     |
| PG4      | A14            | -             | -      | BA0   |
| PG5      | A15            | -             | -      | BA1   |
| PD11     | A16            | A16           | CLE    | -     |
| PD12     | A17            | A17           | ALE    | -     |
| PD13     | A18            | A18           | -      | -     |
| PE3      | A19            | A19           | -      | -     |
| PE4      | A20            | A20           | -      | -     |
| PE5      | A21            | A21           | -      | -     |
| PE6      | A22            | A22           | -      | -     |
| PE2      | A23            | A23           | -      | -     |
| PG13     | A24            | A24           | -      | -     |
| PG14     | A25            | A25           | -      | -     |
| PD14     | D0             | DA0           | D0     | D0    |
| PD15     | D1             | DA1           | D1     | D1    |
| PD0      | D2             | DA2           | D2     | D2    |
| PD1      | D3             | DA3           | D3     | D3    |
| PE7      | D4             | DA4           | D4     | D4    |
| PE8      | D5             | DA5           | D5     | D5    |
| PE9      | D6             | DA6           | D6     | D6    |
| PE10     | D7             | DA7           | D7     | D7    |

Table 11. FMC pin definition (continued)

| Pin name | NOR/PSRAM/SRAM | NOR/PSRAM Mux | NAND16 | SDRAM |
|----------|----------------|---------------|--------|-------|
| PE11     | D8             | DA8           | D8     | D8    |
| PE12     | D9             | DA9           | D9     | D9    |
| PE13     | D10            | DA10          | D10    | D10   |
| PE14     | D11            | DA11          | D11    | D11   |
| PE15     | D12            | DA12          | D12    | D12   |
| PD8      | D13            | DA13          | D13    | D13   |
| PD9      | D14            | DA14          | D14    | D14   |
| PD10     | D15            | DA15          | D15    | D15   |
| PH8      | D16            | -             | -      | D16   |
| PH9      | D17            | -             | -      | D17   |
| PH10     | D18            | -             | -      | D18   |
| PH11     | D19            | -             | -      | D19   |
| PH12     | D20            | -             | -      | D20   |
| PH13     | D21            | -             | -      | D21   |
| PH14     | D22            | -             | -      | D22   |
| PH15     | D23            | -             | -      | D23   |
| PI0      | D24            | -             | -      | D24   |
| PI1      | D25            | -             | -      | D25   |
| PI2      | D26            | -             | -      | D26   |
| PI3      | D27            | -             | -      | D27   |
| PI6      | D28            | -             | -      | D28   |
| PI7      | D29            | -             | -      | D29   |
| PI9      | D30            | -             | -      | D30   |
| PI10     | D31            | -             | -      | D31   |
| PD7      | NE1            | NE1           | -      | -     |
| PG9      | NE2            | NE2           | NCE    | -     |
| PG10     | NE3            | NE3           | -      | -     |
| PG11     | -              | -             | -      | -     |
| PG12     | NE4            | NE4           | -      | -     |
| PD3      | CLK            | CLK           | -      | -     |
| PD4      | NOE            | NOE           | NOE    | -     |
| PD5      | NWE            | NWE           | NWE    | -     |
| PD6      | NWAIT          | NWAIT         | NWAIT  | -     |
| PB7      | NADV           | NADV          | -      | -     |

Table 11. FMC pin definition (continued)

| Pin name | NOR/PSRAM/SRAM | NOR/PSRAM Mux | NAND16 | SDRAM  |
|----------|----------------|---------------|--------|--------|
| PF6      | -              | -             | -      | -      |
| PF7      | -              | -             | -      | -      |
| PF8      | -              | -             | -      | -      |
| PF9      | -              | -             | -      | -      |
| PF10     | -              | -             | -      | -      |
| PG6      | -              | -             | -      | -      |
| PG7      | -              | -             | INT    | -      |
| PE0      | NBL0           | NBL0          | -      | NBL0   |
| PE1      | NBL1           | NBL1          | -      | NBL1   |
| PI4      | NBL2           | -             | -      | NBL2   |
| PI5      | NBL3           | -             | -      | NBL3   |
| PG8      | -              | -             | -      | SDCLK  |
| PC0      | -              | -             | -      | SDNWE  |
| PF11     | -              | -             | -      | SDNRAS |
| PG15     | -              | -             | -      | SDNCAS |
| PH2      | -              | -             | -      | SDCKE0 |
| PH3      | -              | -             | -      | SDNE0  |
| PH6      | -              | -             | -      | SDNE1  |
| PH7      | -              | -             | -      | SDCKE1 |
| PH5      | -              | -             | -      | SDNWE  |
| PC2      | -              | -             | -      | SDNE0  |
| PC3      | -              | -             | -      | SDCKE0 |
| PB5      | -              | -             | -      | SDCKE1 |
| PB6      | -              | -             | -      | SDNE1  |

Table 12. STM32F756xx alternate function mapping

| Port   |      | AF0  | AF1               | AF2      | AF3                     | AF4            | AF5               | AF6              | AF7                           | AF8                           | AF9                            | AF10                 | AF11                            | AF12              | AF13        | AF14      | AF15      |
|--------|------|------|-------------------|----------|-------------------------|----------------|-------------------|------------------|-------------------------------|-------------------------------|--------------------------------|----------------------|---------------------------------|-------------------|-------------|-----------|-----------|
|        |      | SYS  | TIM1/2            | TIM3/4/5 | TIM8/9/10/11/LPTIM1/CEC | I2C1/2/3/4/CEC | SPI1/2/3/4/5/6    | SPI2/3/SPI1      | SPI2/3/USART1/2/3/UART5/SPDIF | SAI2/USART6/UART4/5/7/8/SPDIF | CAN1/2/TIM12/13/14/QUADSPI/LCD | SAI2/QUADSPI/OTG1_FS | ETH/OTG1_FS                     | FMC/SDMMC/OTG2_FS | DCMI        | LCD       | SYS       |
| Port A | PA0  |      | TIM2_CH1/TIM2_ETR | TIM5_CH1 | TIM8_ETR                |                |                   |                  | USART2_CTS                    | UART4_TX                      |                                | SAI2_SDB             | ETH_MII_CRS                     |                   |             |           | EVEN TOUT |
|        | PA1  |      | TIM2_CH2          | TIM5_CH2 |                         |                |                   |                  | USART2_RTS                    | UART4_RX                      | QUADSPI_BK1_IO3                | SAI2_MCK_B           | ETH_MII_RX_CLK/ETH_RMII_REF_CLK |                   |             | LCD_R2    | EVEN TOUT |
|        | PA2  |      | TIM2_CH3          | TIM5_CH3 | TIM9_CH1                |                |                   |                  | USART2_TX                     | SAI2_SCK_B                    |                                |                      | ETH_MDI_O                       |                   |             | LCD_R1    | EVEN TOUT |
|        | PA3  |      | TIM2_CH4          | TIM5_CH4 | TIM9_CH2                |                |                   |                  | USART2_RX                     |                               |                                | OTG_HS_ULPI_D0       | ETH_MII_COL                     |                   |             | LCD_B5    | EVEN TOUT |
|        | PA4  |      |                   |          |                         |                | SPI1_NSS/I2S1_WS  | SPI3_NSS/I2S3_WS | USART2_CK                     |                               |                                |                      |                                 | OTG_HS_SOF        | DCMI_HSYNC  | LCD_VSYNC | EVEN TOUT |
|        | PA5  |      | TIM2_CH1/TIM2_ETR |          | TIM8_CH1N               |                | SPI1_SCK/I2S1_CK  |                  |                               |                               |                                | OTG_HS_ULPI_CK       |                                 |                   |             | LCD_R4    | EVEN TOUT |
|        | PA6  |      | TIM1_BKIN         | TIM3_CH1 | TIM8_BK1N               |                | SPI1_MISO         |                  |                               |                               | TIM13_CH1                      |                      |                                 |                   | DCMI_PIXCLK | LCD_G2    | EVEN TOUT |
|        | PA7  |      | TIM1_CH1N         | TIM3_CH2 | TIM8_CH1N               |                | SPI1_MOSI/I2S1_SD |                  |                               |                               | TIM14_CH1                      |                      | ETH_MII_RX_DV/ETH_RMII_CRS_DV   | FMC_SD_NWE        |             |           | EVEN TOUT |
|        | PA8  | MCO1 | TIM1_CH1          |          | TIM8_BK1N2              | I2C3_SCL       |                   |                  | USART1_CK                     |                               |                                | OTG_FS_SOF           |                                 |                   |             | LCD_R6    | EVEN TOUT |
|        | PA9  |      | TIM1_CH2          |          |                         | I2C3_SMBA      | SPI2_SCK/I2S2_CK  |                  | USART1_TX                     |                               |                                |                      |                                 |                   | DCMI_D0     |           | EVEN TOUT |
|        | PA10 |      | TIM1_CH3          |          |                         |                |                   |                  | USART1_RX                     |                               |                                | OTG_FS_ID            |                                 |                   | DCMI_D1     |           | EVEN TOUT |
|        | PA11 |      | TIM1_CH4          |          |                         |                |                   |                  | USART1_CTS                    |                               | CAN1_RX                        | OTG_FS_DM            |                                 |                   |             | LCD_R4    | EVEN TOUT |
|        | PA12 |      | TIM1_ETR          |          |                         |                |                   |                  | USART1_RTS                    | SAI2_FS_B                     | CAN1_TX                        | OTG_FS_DP            |                                 |                   |             | LCD_R5    | EVEN TOUT |



Table 12. STM32F756xx alternate function mapping (continued)

| Port   |      | AF0                   | AF1                       | AF2          | AF3                             | AF4                | AF5                       | AF6                       | AF7                                       | AF8                                       | AF9                                        | AF10                                     | AF11             | AF12                      | AF13           | AF14   | AF15         |
|--------|------|-----------------------|---------------------------|--------------|---------------------------------|--------------------|---------------------------|---------------------------|-------------------------------------------|-------------------------------------------|--------------------------------------------|------------------------------------------|------------------|---------------------------|----------------|--------|--------------|
|        |      | SYS                   | TIM1/2                    | TIM3/4/5     | TIM8/9/10/<br>11/LPTIM<br>1/CEC | I2C1/2/3/<br>4/CEC | SPI1/2/3/<br>4/5/6        | SPI2/3/S<br>AI1           | SPI2/3/U<br>SART1/2/<br>3/UART5/<br>SPDIF | SAI2/US<br>ART6/UA<br>RT4/5/7/8<br>/SPDIF | CAN1/2/T<br>IM12/13/<br>14/QUAD<br>SPI/LCD | SAI2/QU<br>ADSPI/O<br>TG2_HS/<br>OTG1_FS | ETH/OTG<br>1_FS  | FMC/SD<br>MMC/OT<br>G2_FS | DCMI           | LCD    | SYS          |
| Port A | PA13 | JTMS-<br>SWDIO        |                           |              |                                 |                    |                           |                           |                                           |                                           |                                            |                                          |                  |                           |                |        | EVEN<br>TOUT |
|        | PA14 | JTCK-<br>SWCLK        |                           |              |                                 |                    |                           |                           |                                           |                                           |                                            |                                          |                  |                           |                |        | EVEN<br>TOUT |
|        | PA15 | JTDI                  | TIM2_C<br>H1/TIM2<br>_ETR |              |                                 | HDMI-<br>CEC       | SPI1_NS<br>S/I2S1_<br>WS  | SPI3_NS<br>S/I2S3_<br>WS  |                                           | UART4_<br>RTS                             |                                            |                                          |                  |                           |                |        | EVEN<br>TOUT |
| Port B | PB0  |                       | TIM1_C<br>H2N             | TIM3_C<br>H3 | TIM8_CH<br>2N                   |                    |                           |                           |                                           | UART4_<br>CTS                             | LCD_R3                                     | OTG_HS_<br>ULPI_D1                       | ETH_MII_<br>RXD2 |                           |                |        | EVEN<br>TOUT |
|        | PB1  |                       | TIM1_C<br>H3N             | TIM3_C<br>H4 | TIM8_CH<br>3N                   |                    |                           |                           |                                           |                                           | LCD_R6                                     | OTG_HS_<br>ULPI_D2                       | ETH_MII_<br>RXD3 |                           |                |        | EVEN<br>TOUT |
|        | PB2  |                       |                           |              |                                 |                    |                           | SAI1_SD<br>_A             | SPI3_MO<br>S/I2S3_<br>SD                  |                                           | QUADSP<br>I_CLK                            |                                          |                  |                           |                |        | EVEN<br>TOUT |
|        | PB3  | JTDO/T<br>RACES<br>WO | TIM2_C<br>H2              |              |                                 |                    | SPI1_SC<br>K/I2S1_<br>CK  | SPI3_SC<br>K/I2S3_<br>CK  |                                           |                                           |                                            |                                          |                  |                           |                |        | EVEN<br>TOUT |
|        | PB4  | NJTRST                |                           | TIM3_C<br>H1 |                                 |                    | SPI1_MI<br>SO             | SPI3_MI<br>SO             | SPI2_NS<br>S/I2S2_<br>WS                  |                                           |                                            |                                          |                  |                           |                |        | EVEN<br>TOUT |
|        | PB5  |                       |                           | TIM3_C<br>H2 |                                 | I2C1_SM<br>BA      | SPI1_M<br>OSI/I2S1_<br>SD | SPI3_M<br>OSI/I2S3_<br>SD |                                           |                                           | CAN2_R<br>X                                | OTG_HS_<br>ULPI_D7                       | ETH_PPS<br>_OUT  | FMC_SD<br>CKE1            | DCMI_D<br>10   |        | EVEN<br>TOUT |
|        | PB6  |                       |                           | TIM4_C<br>H1 | HDMI-<br>CEC                    | I2C1_SC<br>L       |                           |                           | USART1<br>_TX                             |                                           | CAN2_T<br>X                                | QUADSPI<br>_BK1_NC<br>S                  |                  | FMC_SD<br>NE1             | DCMI_D<br>5    |        | EVEN<br>TOUT |
|        | PB7  |                       |                           | TIM4_C<br>H2 |                                 | I2C1_SD<br>A       |                           |                           | USART1<br>_RX                             |                                           |                                            |                                          |                  | FMC_NL                    | DCMI_V<br>SYNC |        | EVEN<br>TOUT |
|        | PB8  |                       |                           | TIM4_C<br>H3 | TIM10_C<br>H1                   | I2C1_SC<br>L       |                           |                           |                                           |                                           | CAN1_R<br>X                                |                                          | ETH_MII_<br>TXD3 | SDMMC<br>_D4              | DCMI_D<br>6    | LCD_B6 | EVEN<br>TOUT |
|        | PB9  |                       |                           | TIM4_C<br>H4 | TIM11_CH<br>1                   | I2C1_SD<br>A       | SPI2_NS<br>S/I2S2_<br>WS  |                           |                                           |                                           | CAN1_T<br>X                                |                                          |                  | SDMMC<br>_D5              | DCMI_D<br>7    | LCD_B7 | EVEN<br>TOUT |

Table 12. STM32F756xx alternate function mapping (continued)

| Port   |      | AF0           | AF1           | AF2      | AF3                             | AF4                | AF5                       | AF6             | AF7                                       | AF8                                       | AF9                                        | AF10                                     | AF11                                     | AF12                      | AF13 | AF14   | AF15         |
|--------|------|---------------|---------------|----------|---------------------------------|--------------------|---------------------------|-----------------|-------------------------------------------|-------------------------------------------|--------------------------------------------|------------------------------------------|------------------------------------------|---------------------------|------|--------|--------------|
|        |      | SYS           | TIM1/2        | TIM3/4/5 | TIM8/9/10/<br>11/LPTIM<br>1/CEC | I2C1/2/3/<br>4/CEC | SPI1/2/3/<br>4/5/6        | SPI2/3/S<br>AI1 | SPI2/3/U<br>SART1/2/<br>3/UART5/<br>SPDIF | SAI2/US<br>ART6/UA<br>RT4/5/7/8<br>/SPDIF | CAN1/2/T<br>IM12/13/<br>14/QUAD<br>SPI/LCD | SAI2/QU<br>ADSPI/O<br>TG2_HS/<br>OTG1_FS | ETH/OTG<br>1_FS                          | FMC/SD<br>MMC/OT<br>G2_FS | DCMI | LCD    | SYS          |
| Port B | PB10 |               | TIM2_C<br>H3  |          |                                 | I2C2_SC<br>L       | SPI2_SC<br>K/I2S2_<br>CK  |                 | USART3<br>_TX                             |                                           |                                            | OTG_HS_<br>ULPI_D3                       | ETH_MII_<br>RX_ER                        |                           |      | LCD_G4 | EVEN<br>TOUT |
|        | PB11 |               | TIM2_C<br>H4  |          |                                 | I2C2_SD<br>A       |                           |                 | USART3<br>_RX                             |                                           |                                            | OTG_HS_<br>ULPI_D4                       | ETH_MII_<br>TX_EN/E<br>TH_RMII_<br>TX_EN |                           |      | LCD_G5 | EVEN<br>TOUT |
|        | PB12 |               | TIM1_B<br>KIN |          |                                 | I2C2_SM<br>BA      | SPI2_NS<br>S/I2S2_<br>WS  |                 | USART3<br>_CK                             |                                           | CAN2_R<br>X                                | OTG_HS_<br>ULPI_D5                       | ETH_MII_<br>TXD0/ET<br>H_RMII_T<br>XD0   | OTG_HS<br>_ID             |      |        | EVEN<br>TOUT |
|        | PB13 |               | TIM1_C<br>H1N |          |                                 |                    | SPI2_SC<br>K/I2S2_<br>CK  |                 | USART3<br>_CTS                            |                                           | CAN2_T<br>X                                | OTG_HS_<br>ULPI_D6                       | ETH_MII_<br>TXD1/ET<br>H_RMII_T<br>XD1   |                           |      |        | EVEN<br>TOUT |
|        | PB14 |               | TIM1_C<br>H2N |          | TIM8_CH<br>2N                   |                    | SPI2_MI<br>SO             |                 | USART3<br>_RTS                            |                                           | TIM12_C<br>H1                              |                                          |                                          | OTG_HS<br>_DM             |      |        | EVEN<br>TOUT |
|        | PB15 | RTC_RE<br>FIN | TIM1_C<br>H3N |          | TIM8_CH<br>3N                   |                    | SPI2_M<br>OSI/I2S2<br>_SD |                 |                                           |                                           | TIM12_C<br>H2                              |                                          |                                          | OTG_HS<br>_DP             |      |        | EVEN<br>TOUT |
| Port C | PC0  |               |               |          |                                 |                    |                           |                 |                                           | SAI2_FS<br>_B                             |                                            | OTG_HS_<br>ULPI_ST<br>P                  |                                          | FMC_SD<br>NWE             |      | LCD_R5 | EVEN<br>TOUT |
|        | PC1  | TRACED<br>0   |               |          |                                 |                    | SPI2_M<br>OSI/I2S2<br>_SD | SAI1_SD<br>_A   |                                           |                                           |                                            |                                          | ETH_MD<br>C                              |                           |      |        | EVEN<br>TOUT |
|        | PC2  |               |               |          |                                 |                    | SPI2_MI<br>SO             |                 |                                           |                                           |                                            | OTG_HS_<br>ULPI_DIR                      | ETH_MII_<br>TXD2                         | FMC_SD<br>NE0             |      |        | EVEN<br>TOUT |
|        | PC3  |               |               |          |                                 |                    | SPI2_M<br>OSI/I2S2<br>_SD |                 |                                           |                                           |                                            | OTG_HS_<br>ULPI_NX<br>T                  | ETH_MII_<br>TX_CLK                       | FMC_SD<br>CKE0            |      |        | EVEN<br>TOUT |
|        | PC4  |               |               |          |                                 |                    | I2S1_M<br>CK              |                 |                                           | SPDIF_R<br>X2                             |                                            |                                          | ETH_MII_<br>RXD0/ET<br>H_RMII_<br>RXD0   | FMC_SD<br>NE0             |      |        | EVEN<br>TOUT |



Table 12. STM32F756xx alternate function mapping (continued)

| Port   |      | AF0         | AF1    | AF2          | AF3                             | AF4                | AF5                | AF6                      | AF7                                       | AF8                                       | AF9                                        | AF10                                     | AF11                                   | AF12                      | AF13         | AF14          | AF15         |
|--------|------|-------------|--------|--------------|---------------------------------|--------------------|--------------------|--------------------------|-------------------------------------------|-------------------------------------------|--------------------------------------------|------------------------------------------|----------------------------------------|---------------------------|--------------|---------------|--------------|
|        |      | SYS         | TIM1/2 | TIM3/4/5     | TIM8/9/10/<br>11/LPTIM<br>1/CEC | I2C1/2/3/<br>4/CEC | SPI1/2/3/<br>4/5/6 | SPI2/3/S<br>AI1          | SPI2/3/U<br>SART1/2/<br>3/UART5/<br>SPDIF | SAI2/US<br>ART6/UA<br>RT4/5/7/8<br>/SPDIF | CAN1/2/T<br>IM12/13/<br>14/QUAD<br>SPI/LCD | SAI2/QU<br>ADSPI/O<br>TG2_HS/<br>OTG1_FS | ETH/OTG<br>1_FS                        | FMC/SD<br>MMC/OT<br>G2_FS | DCMI         | LCD           | SYS          |
| Port C | PC5  |             |        |              |                                 |                    |                    |                          |                                           | SPDIF_R<br>X3                             |                                            |                                          | ETH_MII_<br>RXD1/ET<br>H_RMII_<br>RXD1 | FMC_SD<br>CKE0            |              |               | EVEN<br>TOUT |
|        | PC6  |             |        | TIM3_C<br>H1 | TIM8_CH<br>1                    |                    | I2S2_M<br>CK       |                          |                                           | USART6<br>_TX                             |                                            |                                          |                                        | SDMMC<br>_D6              | DCMI_D<br>0  | LCD_HS<br>YNC | EVEN<br>TOUT |
|        | PC7  |             |        | TIM3_C<br>H2 | TIM8_<br>CH2                    |                    |                    | I2S3_M<br>CK             |                                           | USART6<br>_RX                             |                                            |                                          |                                        | SDMMC<br>_D7              | DCMI_D<br>1  | LCD_G6        | EVEN<br>TOUT |
|        | PC8  | TRACED<br>1 |        | TIM3_C<br>H3 | TIM8_<br>CH3                    |                    |                    |                          | UART5_<br>RTS                             | USART6<br>_CK                             |                                            |                                          |                                        | SDMMC<br>_D0              | DCMI_D<br>2  |               | EVEN<br>TOUT |
|        | PC9  | MCO2        |        | TIM3_C<br>H4 | TIM8_<br>CH4                    | I2C3_SD<br>A       | I2S_CK1<br>N       |                          | UART5_<br>CTS                             |                                           | QUADSP<br>I_BK1_IO<br>0                    |                                          |                                        | SDMMC<br>_D1              | DCMI_D<br>3  |               | EVEN<br>TOUT |
|        | PC10 |             |        |              |                                 |                    |                    | SPI3_SC<br>K/I2S3_<br>CK | USART3<br>_TX                             | UART4_T<br>X                              | QUADSP<br>I_BK1_IO<br>1                    |                                          |                                        | SDMMC<br>_D2              | DCMI_D<br>8  | LCD_R2        | EVEN<br>TOUT |
|        | PC11 |             |        |              |                                 |                    |                    | SPI3_MI<br>S0            | USART3<br>_RX                             | UART4_<br>RX                              | QUADSP<br>I_BK2_N<br>CS                    |                                          |                                        | SDMMC<br>_D3              | DCMI_D<br>4  |               | EVEN<br>TOUT |
|        | PC12 | TRACED<br>3 |        |              |                                 |                    |                    | SPI3_M<br>OS/I2S3<br>_SD | USART3<br>_CK                             | UART5_T<br>X                              |                                            |                                          |                                        | SDMMC<br>_CK              | DCMI_D<br>9  |               | EVEN<br>TOUT |
|        | PC13 |             |        |              |                                 |                    |                    |                          |                                           |                                           |                                            |                                          |                                        |                           |              |               | EVEN<br>TOUT |
|        | PC14 |             |        |              |                                 |                    |                    |                          |                                           |                                           |                                            |                                          |                                        |                           |              |               | EVEN<br>TOUT |
|        | PC15 |             |        |              |                                 |                    |                    |                          |                                           |                                           |                                            |                                          |                                        |                           |              |               | EVEN<br>TOUT |
| Port D | PD0  |             |        |              |                                 |                    |                    |                          |                                           |                                           | CAN1_R<br>X                                |                                          |                                        | FMC_D2                    |              |               | EVEN<br>TOUT |
|        | PD1  |             |        |              |                                 |                    |                    |                          |                                           |                                           | CAN1_T<br>X                                |                                          |                                        | FMC_D3                    |              |               | EVEN<br>TOUT |
|        | PD2  | TRACED<br>2 |        | TIM3_ET<br>R |                                 |                    |                    |                          |                                           | UART5_<br>RX                              |                                            |                                          |                                        | SDMMC<br>_CMD             | DCMI_D<br>11 |               | EVEN<br>TOUT |



Table 12. STM32F756xx alternate function mapping (continued)

| Port   |      | AF0 | AF1    | AF2          | AF3                             | AF4                | AF5                       | AF6             | AF7                                       | AF8                                       | AF9                                        | AF10                                     | AF11            | AF12                      | AF13         | AF14   | AF15         |
|--------|------|-----|--------|--------------|---------------------------------|--------------------|---------------------------|-----------------|-------------------------------------------|-------------------------------------------|--------------------------------------------|------------------------------------------|-----------------|---------------------------|--------------|--------|--------------|
|        |      | SYS | TIM1/2 | TIM3/4/5     | TIM8/9/10/<br>11/LPTIM<br>1/CEC | I2C1/2/3/<br>4/CEC | SPI1/2/3/<br>4/5/6        | SPI2/3/S<br>AI1 | SPI2/3/U<br>SART1/2/<br>3/UART5/<br>SPDIF | SAI2/US<br>ART6/UA<br>RT4/5/7/8<br>/SPDIF | CAN1/2/T<br>IM12/13/<br>14/QUAD<br>SPI/LCD | SAI2/QU<br>ADSPI/O<br>TG2_HS/<br>OTG1_FS | ETH/OTG<br>1_FS | FMC/SD<br>MMC/OT<br>G2_FS | DCMI         | LCD    | SYS          |
| Port D | PD3  |     |        |              |                                 |                    | SPI2_SC<br>K/I2S2_<br>CK  |                 | USART2<br>_CTS                            |                                           |                                            |                                          |                 | FMC_CL<br>K               | DCMI_D<br>5  | LCD_G7 | EVEN<br>TOUT |
|        | PD4  |     |        |              |                                 |                    |                           |                 | USART2<br>_RTS                            |                                           |                                            |                                          |                 | FMC_N<br>OE               |              |        | EVEN<br>TOUT |
|        | PD5  |     |        |              |                                 |                    |                           |                 | USART2<br>_TX                             |                                           |                                            |                                          |                 | FMC_N<br>WE               |              |        | EVEN<br>TOUT |
|        | PD6  |     |        |              |                                 |                    | SPI3_M<br>OSI/I2S3<br>_SD | SAI1_SD<br>_A   | USART2<br>_RX                             |                                           |                                            |                                          |                 | FMC_N<br>WAIT             | DCMI_D<br>10 | LCD_B2 | EVEN<br>TOUT |
|        | PD7  |     |        |              |                                 |                    |                           |                 | USART2<br>_CK                             | SPDIF_R<br>X0                             |                                            |                                          |                 | FMC_NE<br>1               |              |        | EVEN<br>TOUT |
|        | PD8  |     |        |              |                                 |                    |                           |                 | USART3<br>_TX                             | SPDIF_R<br>X1                             |                                            |                                          |                 | FMC_D1<br>3               |              |        | EVEN<br>TOUT |
|        | PD9  |     |        |              |                                 |                    |                           |                 | USART3<br>_RX                             |                                           |                                            |                                          |                 | FMC_D1<br>4               |              |        | EVEN<br>TOUT |
|        | PD10 |     |        |              |                                 |                    |                           |                 | USART3<br>_CK                             |                                           |                                            |                                          |                 | FMC_D1<br>5               |              | LCD_B3 | EVEN<br>TOUT |
|        | PD11 |     |        |              |                                 | I2C4_SM<br>BA      |                           |                 | USART3<br>_CTS                            |                                           | QUADSP<br>I_BK1_IO<br>0                    | SAI2_SD_<br>A                            |                 | FMC_A1<br>6/FMC_<br>CLE   |              |        | EVEN<br>TOUT |
|        | PD12 |     |        | TIM4_C<br>H1 | LPTIM1_I<br>N1                  | I2C4_SC<br>L       |                           |                 | USART3<br>_RTS                            |                                           | QUADSP<br>I_BK1_IO<br>1                    | SAI2_FS_<br>A                            |                 | FMC_A1<br>7/FMC_<br>ALE   |              |        | EVEN<br>TOUT |
|        | PD13 |     |        | TIM4_C<br>H2 | LPTIM1_<br>OUT                  | I2C4_SD<br>A       |                           |                 |                                           |                                           | QUADSP<br>I_BK1_IO<br>3                    | SAI2_SC<br>K_A                           |                 | FMC_A1<br>8               |              |        | EVEN<br>TOUT |
|        | PD14 |     |        | TIM4_C<br>H3 |                                 |                    |                           |                 |                                           | UART8_<br>CTS                             |                                            |                                          |                 | FMC_D0                    |              |        | EVEN<br>TOUT |
|        | PD15 |     |        | TIM4_C<br>H4 |                                 |                    |                           |                 |                                           | UART8_<br>RTS                             |                                            |                                          |                 | FMC_D1                    |              |        | EVEN<br>TOUT |
| Port E | PE0  |     |        | TIM4_ET<br>R | LPTIM1_E<br>TR                  |                    |                           |                 |                                           | UART8_<br>Rx                              |                                            | SAI2_MC<br>K_A                           |                 | FMC_NB<br>L0              | DCMI_D<br>2  |        | EVEN<br>TOUT |



Table 12. STM32F756xx alternate function mapping (continued)

| Port   |      | AF0      | AF1        | AF2      | AF3                     | AF4            | AF5            | AF6         | AF7                          | AF8                           | AF9                            | AF10                         | AF11         | AF12              | AF13    | AF14    | AF15      |
|--------|------|----------|------------|----------|-------------------------|----------------|----------------|-------------|------------------------------|-------------------------------|--------------------------------|------------------------------|--------------|-------------------|---------|---------|-----------|
|        |      | SYS      | TIM1/2     | TIM3/4/5 | TIM8/9/10/11/LPTIM1/CEC | I2C1/2/3/4/CEC | SPI1/2/3/4/5/6 | SPI2/3/SAI1 | SPI2/3/UART1/2/3/UART5/SPDIF | SAI2/USART6/UART4/5/7/8/SPDIF | CAN1/2/TIM12/13/14/QUADSPI/LCD | SAI2/QUADSPI/OTG1_HS/OTG1_FS | ETH/OTG1_FS  | FMC/SDMMC/OTG2_FS | DCMI    | LCD     | SYS       |
| Port E | PE1  |          |            |          | LPTIM1_I_N2             |                |                |             |                              | UART8_Tx                      |                                |                              |              | FMC_NBL1          | DCMI_D3 |         | EVEN TOUT |
|        | PE2  | TRACECLK |            |          |                         |                | SPI4_SCK       | SAI1_MCLK_A |                              |                               | QUADSPI_BK1_IO2                |                              | ETH_MII_TXD3 | FMC_A23           |         |         | EVEN TOUT |
|        | PE3  | TRACED0  |            |          |                         |                |                | SAI1_SDB    |                              |                               |                                |                              |              | FMC_A19           |         |         | EVEN TOUT |
|        | PE4  | TRACED1  |            |          |                         |                | SPI4_NSS       | SAI1_FSA    |                              |                               |                                |                              |              | FMC_A20           | DCMI_D4 | LCD_B0  | EVEN TOUT |
|        | PE5  | TRACED2  |            |          | TIM9_CH1                |                | SPI4_MISO      | SAI1_SCK_A  |                              |                               |                                |                              |              | FMC_A21           | DCMI_D6 | LCD_G0  | EVEN TOUT |
|        | PE6  | TRACED3  | TIM1_BKIN2 |          | TIM9_CH2                |                | SPI4_MOSI      | SAI1_SDA    |                              |                               |                                | SAI2_MCK_B                   |              | FMC_A22           | DCMI_D7 | LCD_G1  | EVEN TOUT |
|        | PE7  |          | TIM1_ETR   |          |                         |                |                |             |                              | UART7_Rx                      |                                | QUADSPI_BK2_IO0              |              | FMC_D4            |         |         | EVEN TOUT |
|        | PE8  |          | TIM1_CH1N  |          |                         |                |                |             |                              | UART7_Tx                      |                                | QUADSPI_BK2_IO1              |              | FMC_D5            |         |         | EVEN TOUT |
|        | PE9  |          | TIM1_CH1   |          |                         |                |                |             |                              | UART7_RTS                     |                                | QUADSPI_BK2_IO2              |              | FMC_D6            |         |         | EVEN TOUT |
|        | PE10 |          | TIM1_CH2N  |          |                         |                |                |             |                              | UART7_CTS                     |                                | QUADSPI_BK2_IO3              |              | FMC_D7            |         |         | EVEN TOUT |
|        | PE11 |          | TIM1_CH2   |          |                         |                | SPI4_NSS       |             |                              |                               |                                | SAI2_SDB                     |              | FMC_D8            |         | LCD_G3  | EVEN TOUT |
|        | PE12 |          | TIM1_CH3N  |          |                         |                | SPI4_SCK       |             |                              |                               |                                | SAI2_SCK_B                   |              | FMC_D9            |         | LCD_B4  | EVEN TOUT |
|        | PE13 |          | TIM1_CH3   |          |                         |                | SPI4_MISO      |             |                              |                               |                                | SAI2_FSB                     |              | FMC_D10           |         | LCD_DE  | EVEN TOUT |
|        | PE14 |          | TIM1_CH4   |          |                         |                | SPI4_MOSI      |             |                              |                               |                                | SAI2_MCK_B                   |              | FMC_D11           |         | LCD_CLK | EVEN TOUT |
|        | PE15 |          | TIM1_BKIN  |          |                         |                |                |             |                              |                               |                                |                              |              | FMC_D12           |         | LCD_R7  | EVEN TOUT |

Table 12. STM32F756xx alternate function mapping (continued)

| Port   |      | AF0 | AF1    | AF2      | AF3                             | AF4                | AF5                | AF6             | AF7                                       | AF8                                       | AF9                                        | AF10                                     | AF11            | AF12                      | AF13         | AF14   | AF15         |
|--------|------|-----|--------|----------|---------------------------------|--------------------|--------------------|-----------------|-------------------------------------------|-------------------------------------------|--------------------------------------------|------------------------------------------|-----------------|---------------------------|--------------|--------|--------------|
|        |      | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/<br>11/LPTIM<br>1/CEC | I2C1/2/3/<br>4/CEC | SPI1/2/3/<br>4/5/6 | SPI2/3/S<br>AI1 | SPI2/3/U<br>SART1/2/<br>3/UART5/<br>SPDIF | SAI2/US<br>ART6/UA<br>RT4/5/7/8<br>/SPDIF | CAN1/2/T<br>IM12/13/<br>14/QUAD<br>SPI/LCD | SAI2/QU<br>ADSPI/O<br>TG2_HS/<br>OTG1_FS | ETH/OTG<br>1_FS | FMC/SD<br>MMC/OT<br>G2_FS | DCMI         | LCD    | SYS          |
| Port F | PF0  |     |        |          |                                 | I2C2_SD<br>A       |                    |                 |                                           |                                           |                                            |                                          |                 | FMC_A0                    |              |        | EVEN<br>TOUT |
|        | PF1  |     |        |          |                                 | I2C2_SC<br>L       |                    |                 |                                           |                                           |                                            |                                          |                 | FMC_A1                    |              |        | EVEN<br>TOUT |
|        | PF2  |     |        |          |                                 | I2C2_SM<br>BA      |                    |                 |                                           |                                           |                                            |                                          |                 | FMC_A2                    |              |        | EVEN<br>TOUT |
|        | PF3  |     |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                          |                 | FMC_A3                    |              |        | EVEN<br>TOUT |
|        | PF4  |     |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                          |                 | FMC_A4                    |              |        | EVEN<br>TOUT |
|        | PF5  |     |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                          |                 | FMC_A5                    |              |        | EVEN<br>TOUT |
|        | PF6  |     |        |          | TIM10_C<br>H1                   |                    | SPI5_NS<br>S       | SAI1_SD<br>_B   |                                           | UART7_<br>Rx                              | QUADSP<br>I_BK1_IO<br>3                    |                                          |                 |                           |              |        | EVEN<br>TOUT |
|        | PF7  |     |        |          | TIM11_CH<br>1                   |                    | SPI5_SC<br>K       | SAI1_M<br>CLK_B |                                           | UART7_T<br>x                              | QUADSP<br>I_BK1_IO<br>2                    |                                          |                 |                           |              |        | EVEN<br>TOUT |
|        | PF8  |     |        |          |                                 |                    | SPI5_MI<br>SO      | SAI1_SC<br>K_B  |                                           | UART7_<br>RTS                             | TIM13_C<br>H1                              | QUADSPI<br>_BK1_IO0                      |                 |                           |              |        | EVEN<br>TOUT |
|        | PF9  |     |        |          |                                 |                    | SPI5_M<br>OSI      | SAI1_FS<br>_B   |                                           | UART7_<br>CTS                             | TIM14_C<br>H1                              | QUADSPI<br>_BK1_IO1                      |                 |                           |              |        | EVEN<br>TOUT |
|        | PF10 |     |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                          |                 |                           | DCMI_D<br>11 | LCD_DE | EVEN<br>TOUT |
|        | PF11 |     |        |          |                                 |                    | SPI5_M<br>OSI      |                 |                                           |                                           |                                            | SAI2_SD_<br>B                            |                 | FMC_SD<br>NRAS            | DCMI_D<br>12 |        | EVEN<br>TOUT |
|        | PF12 |     |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                          |                 | FMC_A6                    |              |        | EVEN<br>TOUT |
|        | PF13 |     |        |          |                                 | I2C4_SM<br>BA      |                    |                 |                                           |                                           |                                            |                                          |                 | FMC_A7                    |              |        | EVEN<br>TOUT |
|        | PF14 |     |        |          |                                 | I2C4_SC<br>L       |                    |                 |                                           |                                           |                                            |                                          |                 | FMC_A8                    |              |        | EVEN<br>TOUT |
|        | PF15 |     |        |          |                                 | I2C4_SD<br>A       |                    |                 |                                           |                                           |                                            |                                          |                 | FMC_A9                    |              |        | EVEN<br>TOUT |



Table 12. STM32F756xx alternate function mapping (continued)

| Port   |      | AF0         | AF1    | AF2      | AF3                             | AF4                | AF5                | AF6             | AF7                                       | AF8                                       | AF9                                        | AF10                                     | AF11                                     | AF12                      | AF13           | AF14        | AF15         |
|--------|------|-------------|--------|----------|---------------------------------|--------------------|--------------------|-----------------|-------------------------------------------|-------------------------------------------|--------------------------------------------|------------------------------------------|------------------------------------------|---------------------------|----------------|-------------|--------------|
|        |      | SYS         | TIM1/2 | TIM3/4/5 | TIM8/9/10/<br>11/LPTIM<br>1/CEC | I2C1/2/3/<br>4/CEC | SPI1/2/3/<br>4/5/6 | SPI2/3/S<br>AI1 | SPI2/3/U<br>SART1/2/<br>3/UART5/<br>SPDIF | SAI2/US<br>ART6/UA<br>RT4/5/7/8<br>/SPDIF | CAN1/2/T<br>IM12/13/<br>14/QUAD<br>SPI/LCD | SAI2/QU<br>ADSPI/O<br>TG2_HS/<br>OTG1_FS | ETH/OTG<br>1_FS                          | FMC/SD<br>MMC/OT<br>G2_FS | DCMI           | LCD         | SYS          |
| Port G | PG0  |             |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                          |                                          | FMC_A1<br>0               |                |             | EVEN<br>TOUT |
|        | PG1  |             |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                          |                                          | FMC_A1<br>1               |                |             | EVEN<br>TOUT |
|        | PG2  |             |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                          |                                          | FMC_A1<br>2               |                |             | EVEN<br>TOUT |
|        | PG3  |             |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                          |                                          | FMC_A1<br>3               |                |             | EVEN<br>TOUT |
|        | PG4  |             |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                          |                                          | FMC_A1<br>4/FMC_<br>BA0   |                |             | EVEN<br>TOUT |
|        | PG5  |             |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                          |                                          | FMC_A1<br>5/FMC_<br>BA1   |                |             | EVEN<br>TOUT |
|        | PG6  |             |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                          |                                          |                           | DCMI_D<br>12   | LCD_R7      | EVEN<br>TOUT |
|        | PG7  |             |        |          |                                 |                    |                    |                 |                                           | USART6<br>_CK                             |                                            |                                          |                                          | FMC_IN<br>T               | DCMI_D<br>13   | LCD_CL<br>K | EVEN<br>TOUT |
|        | PG8  |             |        |          |                                 |                    | SPI6_NS<br>S       |                 | SPDIF_R<br>X2                             | USART6<br>_RTS                            |                                            |                                          | ETH_PPS<br>_OUT                          | FMC_SD<br>CLK             |                |             | EVEN<br>TOUT |
|        | PG9  |             |        |          |                                 |                    |                    |                 | SPDIF_R<br>X3                             | USART6<br>_RX                             | QUADSP<br>I_BK2_IO<br>2                    | SAI2_FS_<br>B                            |                                          | FMC_NE<br>2/FMC_<br>NCE   | DCMI_V<br>SYNC |             | EVEN<br>TOUT |
|        | PG10 |             |        |          |                                 |                    |                    |                 |                                           |                                           | LCD_G3                                     | SAI2_SD_<br>B                            |                                          | FMC_NE<br>3               | DCMI_D<br>2    | LCD_B2      | EVEN<br>TOUT |
|        | PG11 |             |        |          |                                 |                    |                    |                 | SPDIF_R<br>X0                             |                                           |                                            |                                          | ETH_MII_<br>TX_EN/E<br>TH_RMII_<br>TX_EN |                           | DCMI_D<br>3    | LCD_B3      | EVEN<br>TOUT |
|        | PG12 |             |        |          | LPTIM1_I<br>N1                  |                    | SPI6_MI<br>SO      |                 | SPDIF_R<br>X1                             | USART6<br>_RTS                            | LCD_B4                                     |                                          |                                          | FMC_NE<br>4               |                | LCD_B1      | EVEN<br>TOUT |
|        | PG13 | TRACED<br>0 |        |          | LPTIM1_<br>OUT                  |                    | SPI6_SC<br>K       |                 |                                           | USART6<br>_CTS                            |                                            |                                          | ETH_MII_<br>TXD0/ET<br>H_RMII_T<br>XD0   | FMC_A2<br>4               |                | LCD_R0      | EVEN<br>TOUT |

Table 12. STM32F756xx alternate function mapping (continued)

| Port   |      | AF0     | AF1    | AF2      | AF3                     | AF4            | AF5            | AF6         | AF7                          | AF8                           | AF9                            | AF10                 | AF11                       | AF12              | AF13       | AF14   | AF15      |
|--------|------|---------|--------|----------|-------------------------|----------------|----------------|-------------|------------------------------|-------------------------------|--------------------------------|----------------------|----------------------------|-------------------|------------|--------|-----------|
|        |      | SYS     | TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1/CEC | I2C1/2/3/4/CEC | SPI1/2/3/4/5/6 | SPI2/3/SAI1 | SPI2/3/UART1/2/3/UART5/SPDIF | SAI2/USART6/UART4/5/7/8/SPDIF | CAN1/2/TIM12/13/14/QUADSPI/LCD | SAI2/QUADSPI/OTG1_FS | ETH/OTG1_FS                | FMC/SDMMC/OTG2_FS | DCMI       | LCD    | SYS       |
| Port G | PG14 | TRACED1 |        |          | LPTIM1_ETR              |                | SPI6_MOSI      |             |                              | USART6_TX                     | QUADSPI_BK2_IO3                |                      | ETH_MII_TXD1/ETH_RMII_TXD1 | FMC_A25           |            | LCD_B0 | EVEN TOUT |
|        | PG15 |         |        |          |                         |                |                |             |                              | USART6_CTS                    |                                |                      |                            | FMC_SDNCAS        | DCMI_D13   |        | EVEN TOUT |
| Port H | PH0  |         |        |          |                         |                |                |             |                              |                               |                                |                      |                            |                   |            |        | EVEN TOUT |
|        | PH1  |         |        |          |                         |                |                |             |                              |                               |                                |                      |                            |                   |            |        | EVEN TOUT |
|        | PH2  |         |        |          | LPTIM1_IN2              |                |                |             |                              |                               | QUADSPI_BK2_IO0                | SAI2_SCK_B           | ETH_MII_CRS                | FMC_SDCKE0        |            | LCD_R0 | EVEN TOUT |
|        | PH3  |         |        |          |                         |                |                |             |                              |                               | QUADSPI_BK2_IO1                | SAI2_MCK_B           | ETH_MII_COL                | FMC_SDNE0         |            | LCD_R1 | EVEN TOUT |
|        | PH4  |         |        |          |                         | I2C2_SCL       |                |             |                              |                               |                                | OTG_HS_ULPI_NXT      |                            |                   |            |        | EVEN TOUT |
|        | PH5  |         |        |          |                         | I2C2_SDA       | SPI5_NSS       |             |                              |                               |                                |                      |                            | FMC_SDNWE         |            |        | EVEN TOUT |
|        | PH6  |         |        |          |                         | I2C2_SMB_A     | SPI5_SCK       |             |                              |                               | TIM12_CH1                      |                      | ETH_MII_RXD2               | FMC_SDNE1         | DCMI_D8    |        | EVEN TOUT |
|        | PH7  |         |        |          |                         | I2C3_SCL       | SPI5_MISO      |             |                              |                               |                                |                      | ETH_MII_RXD3               | FMC_SDCKE1        | DCMI_D9    |        | EVEN TOUT |
|        | PH8  |         |        |          |                         | I2C3_SDA       |                |             |                              |                               |                                |                      |                            | FMC_D16           | DCMI_HSYNC | LCD_R2 | EVEN TOUT |
|        | PH9  |         |        |          |                         | I2C3_SMB_A     |                |             |                              |                               | TIM12_CH2                      |                      |                            | FMC_D17           | DCMI_D0    | LCD_R3 | EVEN TOUT |
|        | PH10 |         |        | TIM5_CH1 |                         | I2C4_SMB_A     |                |             |                              |                               |                                |                      |                            | FMC_D18           | DCMI_D1    | LCD_R4 | EVEN TOUT |
|        | PH11 |         |        | TIM5_CH2 |                         | I2C4_SCL       |                |             |                              |                               |                                |                      |                            | FMC_D19           | DCMI_D2    | LCD_R5 | EVEN TOUT |
|        | PH12 |         |        | TIM5_CH3 |                         | I2C4_SDA       |                |             |                              |                               |                                |                      |                            | FMC_D20           | DCMI_D3    | LCD_R6 | EVEN TOUT |



Table 12. STM32F756xx alternate function mapping (continued)

| Port   |      | AF0 | AF1    | AF2          | AF3                             | AF4                | AF5                       | AF6             | AF7                                       | AF8                                       | AF9                                        | AF10                                     | AF11              | AF12                      | AF13           | AF14          | AF15         |
|--------|------|-----|--------|--------------|---------------------------------|--------------------|---------------------------|-----------------|-------------------------------------------|-------------------------------------------|--------------------------------------------|------------------------------------------|-------------------|---------------------------|----------------|---------------|--------------|
|        |      | SYS | TIM1/2 | TIM3/4/5     | TIM8/9/10/<br>11/LPTIM<br>1/CEC | I2C1/2/3/<br>4/CEC | SPI1/2/3/<br>4/5/6        | SPI2/3/S<br>AI1 | SPI2/3/U<br>SART1/2/<br>3/UART5/<br>SPDIF | SAI2/US<br>ART6/UA<br>RT4/5/7/8<br>/SPDIF | CAN1/2/T<br>IM12/13/<br>14/QUAD<br>SPI/LCD | SAI2/QU<br>ADSPI/O<br>TG2_HS/<br>OTG1_FS | ETH/OTG<br>1_FS   | FMC/SD<br>MMC/OT<br>G2_FS | DCMI           | LCD           | SYS          |
| Port H | PH13 |     |        |              | TIM8_CH<br>1N                   |                    |                           |                 |                                           |                                           | CAN1_T<br>X                                |                                          |                   | FMC_D2<br>1               |                | LCD_G2        | EVEN<br>TOUT |
|        | PH14 |     |        |              | TIM8_CH<br>2N                   |                    |                           |                 |                                           |                                           |                                            |                                          |                   | FMC_D2<br>2               | DCMI_D<br>4    | LCD_G3        | EVEN<br>TOUT |
|        | PH15 |     |        |              | TIM8_CH<br>3N                   |                    |                           |                 |                                           |                                           |                                            |                                          |                   | FMC_D2<br>3               | DCMI_D<br>11   | LCD_G4        | EVEN<br>TOUT |
| Port I | PI0  |     |        | TIM5_C<br>H4 |                                 |                    | SPI2_NS<br>S/I2S2_<br>WS  |                 |                                           |                                           |                                            |                                          |                   | FMC_D2<br>4               | DCMI_D<br>13   | LCD_G5        | EVEN<br>TOUT |
|        | PI1  |     |        |              | TIM8_BKI<br>N2                  |                    | SPI2_SC<br>K/I2S2_<br>CK  |                 |                                           |                                           |                                            |                                          |                   | FMC_D2<br>5               | DCMI_D<br>8    | LCD_G6        | EVEN<br>TOUT |
|        | PI2  |     |        |              | TIM8_CH<br>4                    |                    | SPI2_MI<br>SO             |                 |                                           |                                           |                                            |                                          |                   | FMC_D2<br>6               | DCMI_D<br>9    | LCD_G7        | EVEN<br>TOUT |
|        | PI3  |     |        |              | TIM8_ET<br>R                    |                    | SPI2_M<br>OSI/I2S2<br>_SD |                 |                                           |                                           |                                            |                                          |                   | FMC_D2<br>7               | DCMI_D<br>10   |               | EVEN<br>TOUT |
|        | PI4  |     |        |              | TIM8_BKI<br>N                   |                    |                           |                 |                                           |                                           |                                            | SAI2_MC<br>K_A                           |                   | FMC_NB<br>L2              | DCMI_D<br>5    | LCD_B4        | EVEN<br>TOUT |
|        | PI5  |     |        |              | TIM8_CH<br>1                    |                    |                           |                 |                                           |                                           |                                            | SAI2_SC<br>K_A                           |                   | FMC_NB<br>L3              | DCMI_V<br>SYNC | LCD_B5        | EVEN<br>TOUT |
|        | PI6  |     |        |              | TIM8_CH<br>2                    |                    |                           |                 |                                           |                                           |                                            | SAI2_SD_<br>A                            |                   | FMC_D2<br>8               | DCMI_D<br>6    | LCD_B6        | EVEN<br>TOUT |
|        | PI7  |     |        |              | TIM8_CH<br>3                    |                    |                           |                 |                                           |                                           |                                            | SAI2_FS_<br>A                            |                   | FMC_D2<br>9               | DCMI_D<br>7    | LCD_B7        | EVEN<br>TOUT |
|        | PI8  |     |        |              |                                 |                    |                           |                 |                                           |                                           |                                            |                                          |                   |                           |                |               | EVEN<br>TOUT |
|        | PI9  |     |        |              |                                 |                    |                           |                 |                                           |                                           | CAN1_R<br>X                                |                                          |                   | FMC_D3<br>0               |                | LCD_VS<br>YNC | EVEN<br>TOUT |
|        | PI10 |     |        |              |                                 |                    |                           |                 |                                           |                                           |                                            |                                          | ETH_MII_<br>RX_ER | FMC_D3<br>1               |                | LCD_HS<br>YNC | EVEN<br>TOUT |
|        | PI11 |     |        |              |                                 |                    |                           |                 |                                           |                                           |                                            | OTG_HS_<br>ULPI_DIR                      |                   |                           |                |               | EVEN<br>TOUT |

Table 12. STM32F756xx alternate function mapping (continued)

| Port   |      | AF0 | AF1    | AF2      | AF3                             | AF4                | AF5                | AF6             | AF7                                       | AF8                                       | AF9                                        | AF10                                     | AF11            | AF12                      | AF13 | AF14          | AF15         |
|--------|------|-----|--------|----------|---------------------------------|--------------------|--------------------|-----------------|-------------------------------------------|-------------------------------------------|--------------------------------------------|------------------------------------------|-----------------|---------------------------|------|---------------|--------------|
|        |      | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/<br>11/LPTIM<br>1/CEC | I2C1/2/3/<br>4/CEC | SPI1/2/3/<br>4/5/6 | SPI2/3/S<br>AI1 | SPI2/3/U<br>SART1/2/<br>3/UART5/<br>SPDIF | SAI2/US<br>ART6/UA<br>RT4/5/7/8<br>/SPDIF | CAN1/2/T<br>IM12/13/<br>14/QUAD<br>SPI/LCD | SAI2/QU<br>ADSPI/O<br>TG2_HS/<br>OTG1_FS | ETH/OTG<br>1_FS | FMC/SD<br>MMC/OT<br>G2_FS | DCMI | LCD           | SYS          |
| Port I | PI12 |     |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                          |                 |                           |      | LCD_HS<br>YNC | EVEN<br>TOUT |
|        | PI13 |     |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                          |                 |                           |      | LCD_VS<br>YNC | EVEN<br>TOUT |
|        | PI14 |     |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                          |                 |                           |      | LCD_CL<br>K   | EVEN<br>TOUT |
|        | PI15 |     |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                          |                 |                           |      | LCD_R0        | EVEN<br>TOUT |
| Port J | PJ0  |     |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                          |                 |                           |      | LCD_R1        | EVEN<br>TOUT |
|        | PJ1  |     |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                          |                 |                           |      | LCD_R2        | EVEN<br>TOUT |
|        | PJ2  |     |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                          |                 |                           |      | LCD_R3        | EVEN<br>TOUT |
|        | PJ3  |     |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                          |                 |                           |      | LCD_R4        | EVEN<br>TOUT |
|        | PJ4  |     |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                          |                 |                           |      | LCD_R5        | EVEN<br>TOUT |
|        | PJ5  |     |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                          |                 |                           |      | LCD_R6        | EVEN<br>TOUT |
|        | PJ6  |     |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                          |                 |                           |      | LCD_R7        | EVEN<br>TOUT |
|        | PJ7  |     |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                          |                 |                           |      | LCD_G0        | EVEN<br>TOUT |
|        | PJ8  |     |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                          |                 |                           |      | LCD_G1        | EVEN<br>TOUT |
|        | PJ9  |     |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                          |                 |                           |      | LCD_G2        | EVEN<br>TOUT |
|        | PJ10 |     |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                          |                 |                           |      | LCD_G3        | EVEN<br>TOUT |
|        | PJ11 |     |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                          |                 |                           |      | LCD_G4        | EVEN<br>TOUT |



Table 12. STM32F756xx alternate function mapping (continued)

| Port   |      | AF0 | AF1    | AF2      | AF3                             | AF4                | AF5                | AF6             | AF7                                       | AF8                                       | AF9                                        | AF10                                    | AF11            | AF12                      | AF13 | AF14   | AF15         |
|--------|------|-----|--------|----------|---------------------------------|--------------------|--------------------|-----------------|-------------------------------------------|-------------------------------------------|--------------------------------------------|-----------------------------------------|-----------------|---------------------------|------|--------|--------------|
|        |      | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/<br>11/LPTIM<br>1/CEC | I2C1/2/3/<br>4/CEC | SPI1/2/3/<br>4/5/6 | SPI2/3/S<br>AI1 | SPI2/3/U<br>SART1/2/<br>3/UART5/<br>SPDIF | SAI2/US<br>ART6/UA<br>RT4/5/7/8<br>/SPDIF | CAN1/2/T<br>IM12/13/<br>14/QUAD<br>SPI/LCD | SAI2/QU<br>ADSPI/O<br>TG_HS/<br>OTG1_FS | ETH/OTG<br>1_FS | FMC/SD<br>MMC/OT<br>G2_FS | DCMI | LCD    | SYS          |
| Port J | PJ12 |     |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                         |                 |                           |      | LCD_B0 | EVEN<br>TOUT |
|        | PJ13 |     |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                         |                 |                           |      | LCD_B1 | EVEN<br>TOUT |
|        | PJ14 |     |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                         |                 |                           |      | LCD_B2 | EVEN<br>TOUT |
|        | PJ15 |     |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                         |                 |                           |      | LCD_B3 | EVEN<br>TOUT |
| Port K | PK0  |     |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                         |                 |                           |      | LCD_G5 | EVEN<br>TOUT |
|        | PK1  |     |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                         |                 |                           |      | LCD_G6 | EVEN<br>TOUT |
|        | PK2  |     |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                         |                 |                           |      | LCD_G7 | EVEN<br>TOUT |
|        | PK3  |     |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                         |                 |                           |      | LCD_B4 | EVEN<br>TOUT |
|        | PK4  |     |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                         |                 |                           |      | LCD_B5 | EVEN<br>TOUT |
|        | PK5  |     |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                         |                 |                           |      | LCD_B6 | EVEN<br>TOUT |
|        | PK6  |     |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                         |                 |                           |      | LCD_B7 | EVEN<br>TOUT |
|        | PK7  |     |        |          |                                 |                    |                    |                 |                                           |                                           |                                            |                                         |                 |                           |      | LCD_DE | EVEN<br>TOUT |



4 Memory mapping

The memory map is shown in *Figure 16*.

Figure 16. Memory map

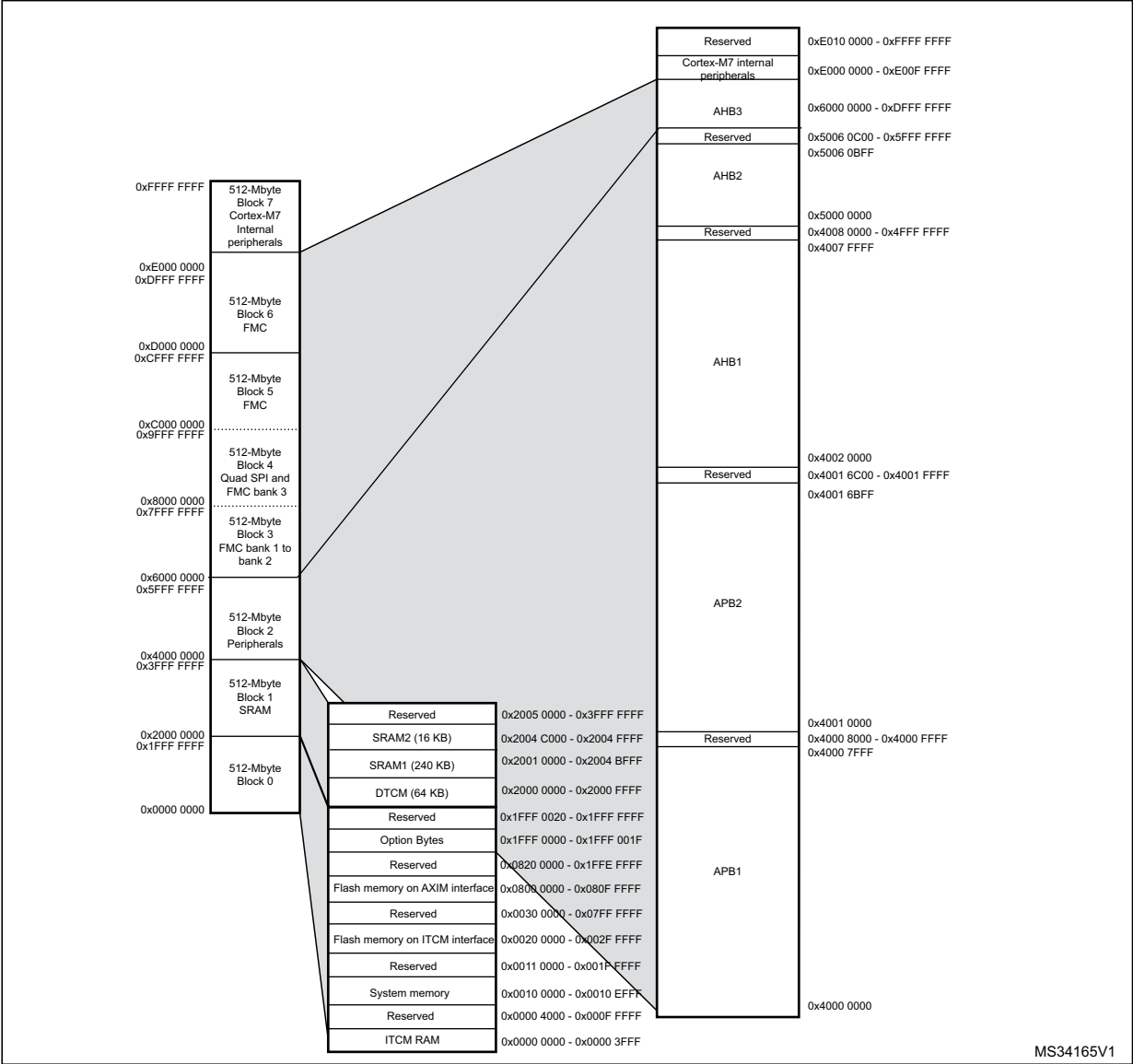


Table 13. STM32F756xx register boundary addresses

| Bus       | Boundary address          | Peripheral                     |
|-----------|---------------------------|--------------------------------|
|           | 0xE00F FFFF - 0xFFFF FFFF | Reserved                       |
| Cortex-M7 | 0xE000 0000 - 0xE00F FFFF | Cortex-M7 internal peripherals |
| AHB3      | 0xD000 0000 - 0xDFFF FFFF | FMC bank 6                     |
|           | 0xC000 0000 - 0xCFFF FFFF | FMC bank 5                     |
|           | 0xA000 2000 - 0xBFFF FFFF | Reserved                       |
|           | 0xA000 1000 - 0xA000 1FFF | Quad SPI control register      |
|           | 0xA000 0000 - 0xA000 0FFF | FMC control register           |
|           | 0x9000 0000 - 0x9FFF FFFF | Quad SPI                       |
|           | 0x8000 0000 - 0x8FFF FFFF | FMC bank 3                     |
|           | 0x7000 0000 - 0x7FFF FFFF | FMC bank 2                     |
|           | 0x6000 0000 - 0x6FFF FFFF | FMC bank 1                     |
|           | 0x5006 0C00 - 0x5FFF FFFF | Reserved                       |
| AHB2      | 0x5006 0800 - 0x5006 0BFF | RNG                            |
|           | 0x5006 0400 - 0x5006 07FF | HASH                           |
|           | 0x5006 0000 - 0x5006 03FF | CRYP                           |
|           | 0x5005 0400 - 0x5006 07FF | Reserved                       |
|           | 0x5005 0000 - 0x5005 03FF | DCMI                           |
|           | 0x5004 0000 - 0x5004 FFFF | Reserved                       |
|           | 0x5000 0000 - 0x5003 FFFF | USB OTG FS                     |

Table 13. STM32F756xx register boundary addresses (continued)

| Bus  | Boundary address          | Peripheral               |
|------|---------------------------|--------------------------|
|      | 0x4008 0000- 0x4FFF FFFF  | Reserved                 |
| AHB1 | 0x4004 0000 - 0x4007 FFFF | USB OTG HS               |
|      | 0x4002 BC00- 0x4003 FFFF  | Reserved                 |
|      | 0x4002 B000 - 0x4002 BBFF | Chrom-ART (DMA2D)        |
|      | 0x4002 9400 - 0x4002 AFFF | Reserved                 |
|      | 0x4002 9000 - 0x4002 93FF | ETHERNET MAC             |
|      | 0x4002 8C00 - 0x4002 8FFF |                          |
|      | 0x4002 8800 - 0x4002 8BFF |                          |
|      | 0x4002 8400 - 0x4002 87FF |                          |
|      | 0x4002 8000 - 0x4002 83FF |                          |
|      | 0x4002 6800 - 0x4002 7FFF | Reserved                 |
|      | 0x4002 6400 - 0x4002 67FF | DMA2                     |
|      | 0x4002 6000 - 0x4002 63FF | DMA1                     |
|      | 0x4002 5000 - 0x4002 5FFF | Reserved                 |
|      | 0x4002 4000 - 0x4002 4FFF | BKPSRAM                  |
|      | 0x4002 3C00 - 0x4002 3FFF | Flash interface register |
|      | 0x4002 3800 - 0x4002 3BFF | RCC                      |
|      | 0x4002 3400 - 0x4002 37FF | Reserved                 |
|      | 0x4002 3000 - 0x4002 33FF | CRC                      |
|      | 0x4002 2C00 - 0x4002 2FFF | Reserved                 |
|      | 0x4002 2800 - 0x4002 2BFF | GPIOK                    |
|      | 0x4002 2400 - 0x4002 27FF | GPIOJ                    |
|      | 0x4002 2000 - 0x4002 23FF | GPIOI                    |
|      | 0x4002 1C00 - 0x4002 1FFF | GPIOH                    |
|      | 0x4002 1800 - 0x4002 1BFF | GPIOG                    |
|      | 0x4002 1400 - 0x4002 17FF | GPIOF                    |
|      | 0x4002 1000 - 0x4002 13FF | GPIOE                    |
|      | 0x4002 0C00 - 0x4002 0FFF | GPIOD                    |
|      | 0x4002 0800 - 0x4002 0BFF | GPIOC                    |
|      | 0x4002 0400 - 0x4002 07FF | GPIOB                    |
|      | 0x4002 0000 - 0x4002 03FF | GPIOA                    |

Table 13. STM32F756xx register boundary addresses (continued)

| Bus  | Boundary address          | Peripheral         |
|------|---------------------------|--------------------|
|      | 0x4001 6C00 - 0x4001 FFFF | Reserved           |
| APB2 | 0x4001 6800 - 0x4001 6BFF | LCD-TFT            |
|      | 0x4001 6000 - 0x4001 67FF | Reserved           |
|      | 0x4001 5C00 - 0x4001 5FFF | SAI2               |
|      | 0x4001 5800 - 0x4001 5BFF | SAI1               |
|      | 0x4001 5400 - 0x4001 57FF | SPI6               |
|      | 0x4001 5000 - 0x4001 53FF | SPI5               |
|      | 0x4001 4C00 - 0x4001 4FFF | Reserved           |
|      | 0x4001 4800 - 0x4001 4BFF | TIM11              |
|      | 0x4001 4400 - 0x4001 47FF | TIM10              |
|      | 0x4001 4000 - 0x4001 43FF | TIM9               |
|      | 0x4001 3C00 - 0x4001 3FFF | EXTI               |
|      | 0x4001 3800 - 0x4001 3BFF | SYSCFG             |
|      | 0x4001 3400 - 0x4001 37FF | SPI4               |
|      | 0x4001 3000 - 0x4001 33FF | SPI1/I2S1          |
|      | 0x4001 2C00 - 0x4001 2FFF | SDMMC              |
|      | 0x4001 2400 - 0x4001 2BFF | Reserved           |
|      | 0x4001 2000 - 0x4001 23FF | ADC1 - ADC2 - ADC3 |
|      | 0x4001 1800 - 0x4001 1FFF | Reserved           |
|      | 0x4001 1400 - 0x4001 17FF | USART6             |
|      | 0x4001 1000 - 0x4001 13FF | USART1             |
|      | 0x4001 0800 - 0x4001 0FFF | Reserved           |
|      | 0x4001 0400 - 0x4001 07FF | TIM8               |
|      | 0x4001 0000 - 0x4001 03FF | TIM1               |

Table 13. STM32F756xx register boundary addresses (continued)

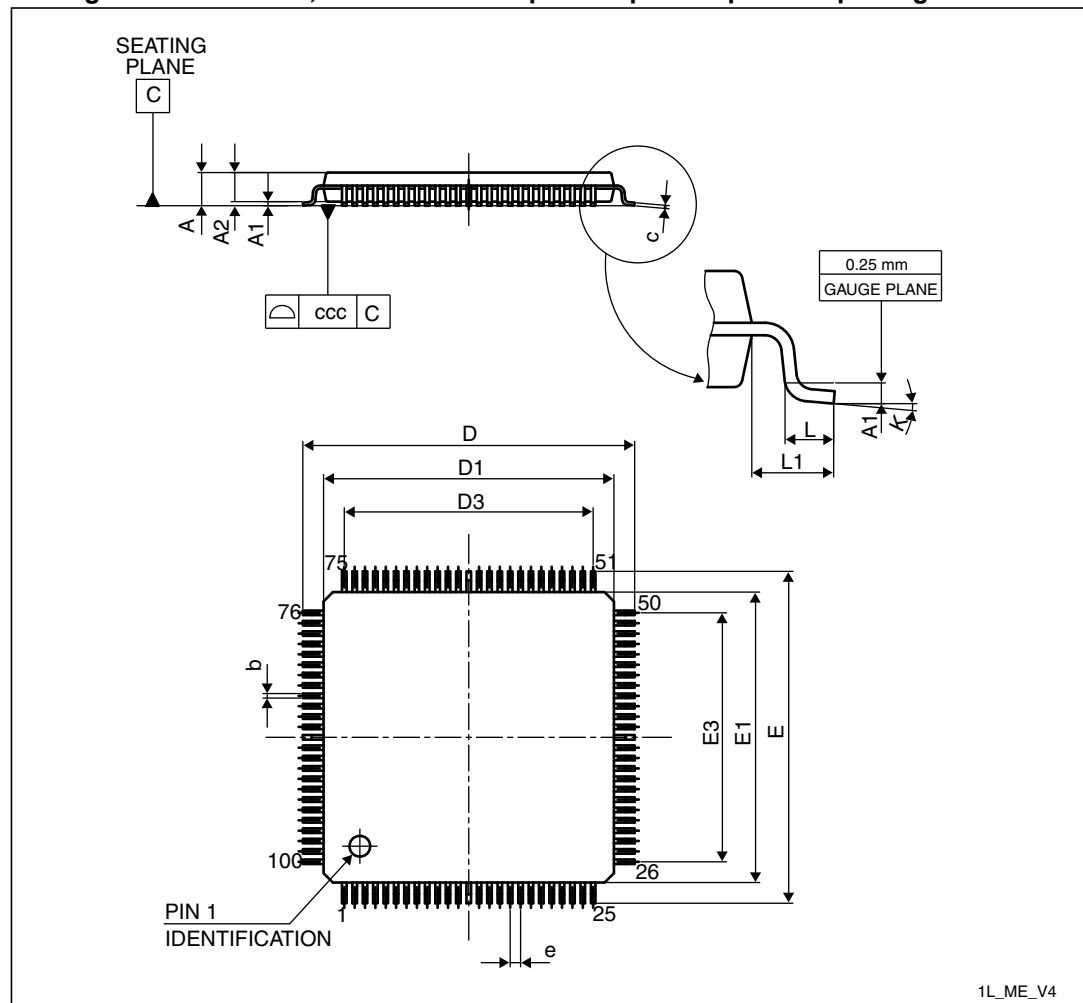
| Bus  | Boundary address          | Peripheral          |
|------|---------------------------|---------------------|
|      | 0x4000 8000 - 0x4000 FFFF | Reserved            |
| APB1 | 0x4000 7C00 - 0x4000 7FFF | UART8               |
|      | 0x4000 7800 - 0x4000 7BFF | UART7               |
|      | 0x4000 7400 - 0x4000 77FF | DAC                 |
|      | 0x4000 7000 - 0x4000 73FF | PWR                 |
|      | 0x4000 6C00 - 0x4000 6FFF | HDMI-CEC            |
|      | 0x4000 6800 - 0x4000 6BFF | CAN2                |
|      | 0x4000 6400 - 0x4000 67FF | CAN1                |
|      | 0x4000 6000 - 0x4000 63FF | I2C4                |
|      | 0x4000 5C00 - 0x4000 5FFF | I2C3                |
|      | 0x4000 5800 - 0x4000 5BFF | I2C2                |
|      | 0x4000 5400 - 0x4000 57FF | I2C1                |
|      | 0x4000 5000 - 0x4000 53FF | UART5               |
|      | 0x4000 4C00 - 0x4000 4FFF | UART4               |
|      | 0x4000 4800 - 0x4000 4BFF | USART3              |
|      | 0x4000 4400 - 0x4000 47FF | USART2              |
|      | 0x4000 4000 - 0x4000 43FF | SPDIF-RX            |
|      | 0x4000 3C00 - 0x4000 3FFF | SPI3 / I2S3         |
|      | 0x4000 3800 - 0x4000 3BFF | SPI2 / I2S2         |
|      | 0x4000 3400 - 0x4000 37FF | Reserved            |
|      | 0x4000 3000 - 0x4000 33FF | IWDG                |
|      | 0x4000 2C00 - 0x4000 2FFF | WWDG                |
|      | 0x4000 2800 - 0x4000 2BFF | RTC & BKP Registers |
|      | 0x4000 2400 - 0x4000 27FF | LPTIM1              |
|      | 0x4000 2000 - 0x4000 23FF | TIM14               |
|      | 0x4000 1C00 - 0x4000 1FFF | TIM13               |
|      | 0x4000 1800 - 0x4000 1BFF | TIM12               |
|      | 0x4000 1400 - 0x4000 17FF | TIM7                |
|      | 0x4000 1000 - 0x4000 13FF | TIM6                |
|      | 0x4000 0C00 - 0x4000 0FFF | TIM5                |
|      | 0x4000 0800 - 0x4000 0BFF | TIM4                |
|      | 0x4000 0400 - 0x4000 07FF | TIM3                |
|      | 0x4000 0000 - 0x4000 03FF | TIM2                |

## 5 Package characteristics

### 5.1 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

Figure 17. LQFP100, 14 x 14 mm 100-pin low-profile quad flat package outline



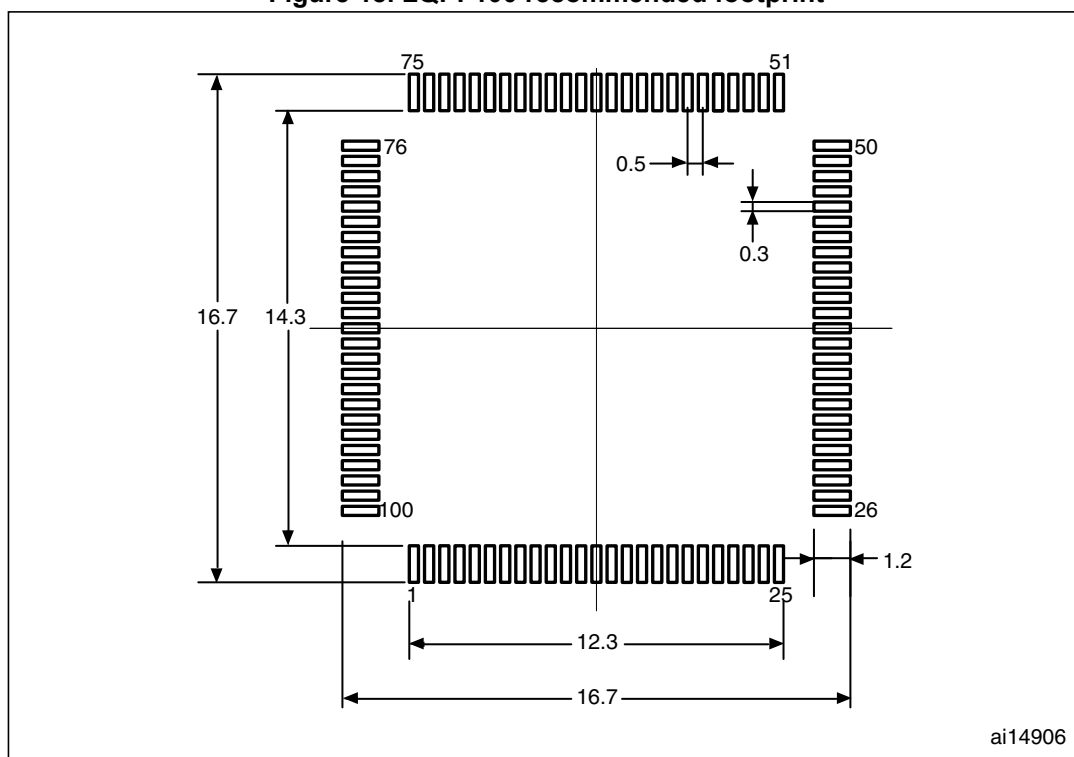
1. Drawing is not to scale.

Table 14. LQPF100, 14 x 14 mm 100-pin low-profile quad flat package mechanical data

| Symbol | millimeters |        |        | inches <sup>(1)</sup> |        |        |
|--------|-------------|--------|--------|-----------------------|--------|--------|
|        | Min         | Typ    | Max    | Min                   | Typ    | Max    |
| A      | -           | -      | 1.600  | -                     | -      | 0.0630 |
| A1     | 0.050       | -      | 0.150  | 0.0020                | -      | 0.0059 |
| A2     | 1.350       | 1.400  | 1.450  | 0.0531                | 0.0551 | 0.0571 |
| b      | 0.170       | 0.220  | 0.270  | 0.0067                | 0.0087 | 0.0106 |
| c      | 0.090       | -      | 0.200  | 0.0035                | -      | 0.0079 |
| D      | 15.800      | 16.000 | 16.200 | 0.6220                | 0.6299 | 0.6378 |
| D1     | 13.800      | 14.000 | 14.200 | 0.5433                | 0.5512 | 0.5591 |
| D3     | -           | 12.000 | -      | -                     | 0.4724 | -      |
| E      | 15.800      | 16.000 | 16.200 | 0.6220                | 0.6299 | 0.6378 |
| E1     | 13.800      | 14.000 | 14.200 | 0.5433                | 0.5512 | 0.5591 |
| E3     | -           | 12.000 | -      | -                     | 0.4724 | -      |
| e      | -           | 0.500  | -      | -                     | 0.0197 | -      |
| L      | 0.450       | 0.600  | 0.750  | 0.0177                | 0.0236 | 0.0295 |
| L1     | -           | 1.000  | -      | -                     | 0.0394 | -      |
| k      | 0°          | 3.5°   | 7°     | 0°                    | 3.5°   | 7°     |
| ccc    | -           | -      | 0.080  | -                     | -      | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 18. LQPF100 recommended footprint



1. Dimensions are expressed in millimeters.



## Device marking

Figure 19. LQFP100 marking (package top view)

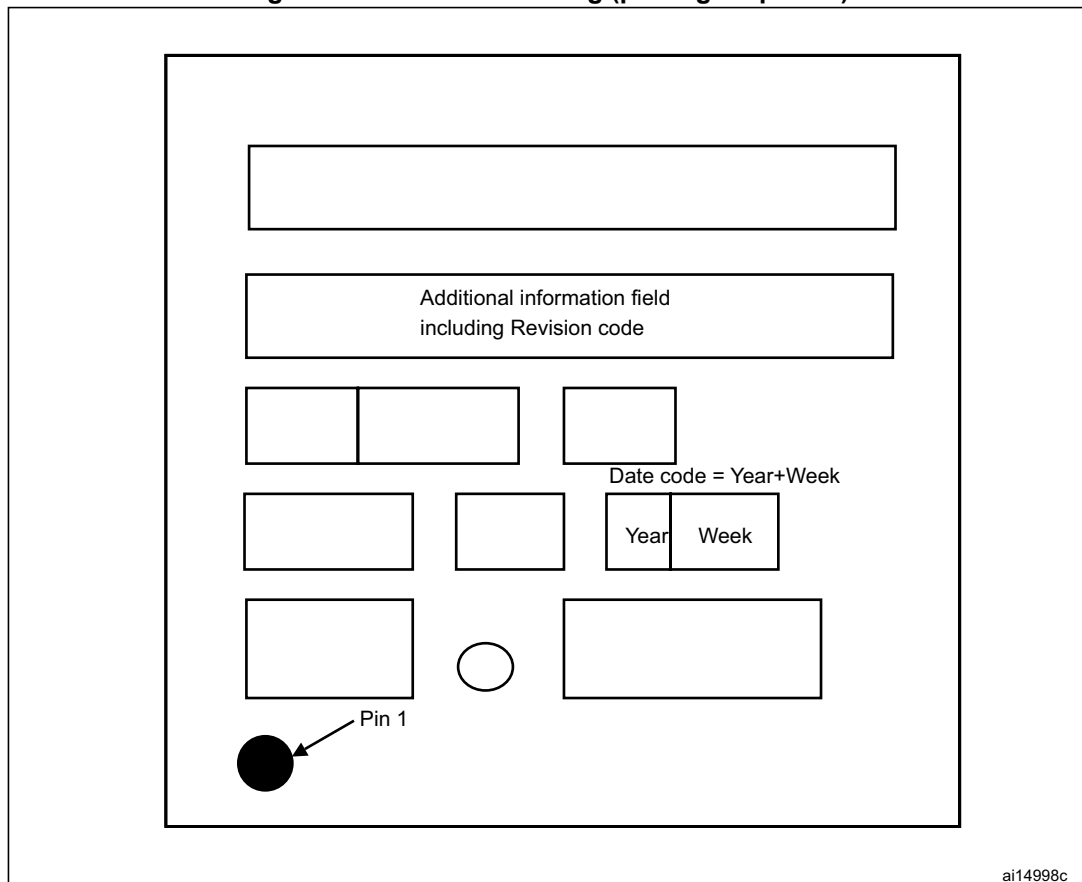
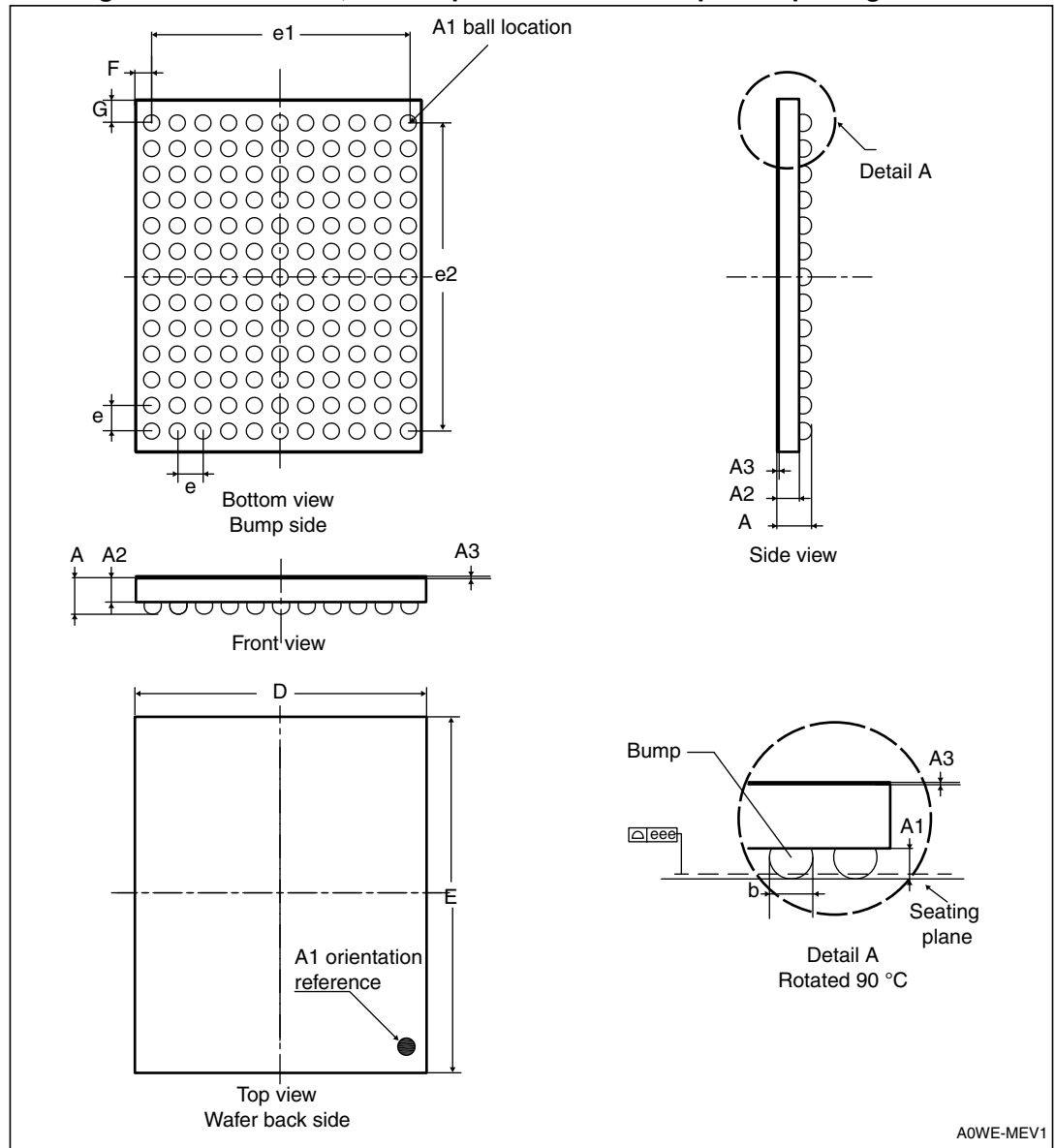


Figure 20. WLCSP143, 0.4 mm pitch wafer level chip scale package outline



1. Drawing is not to scale.

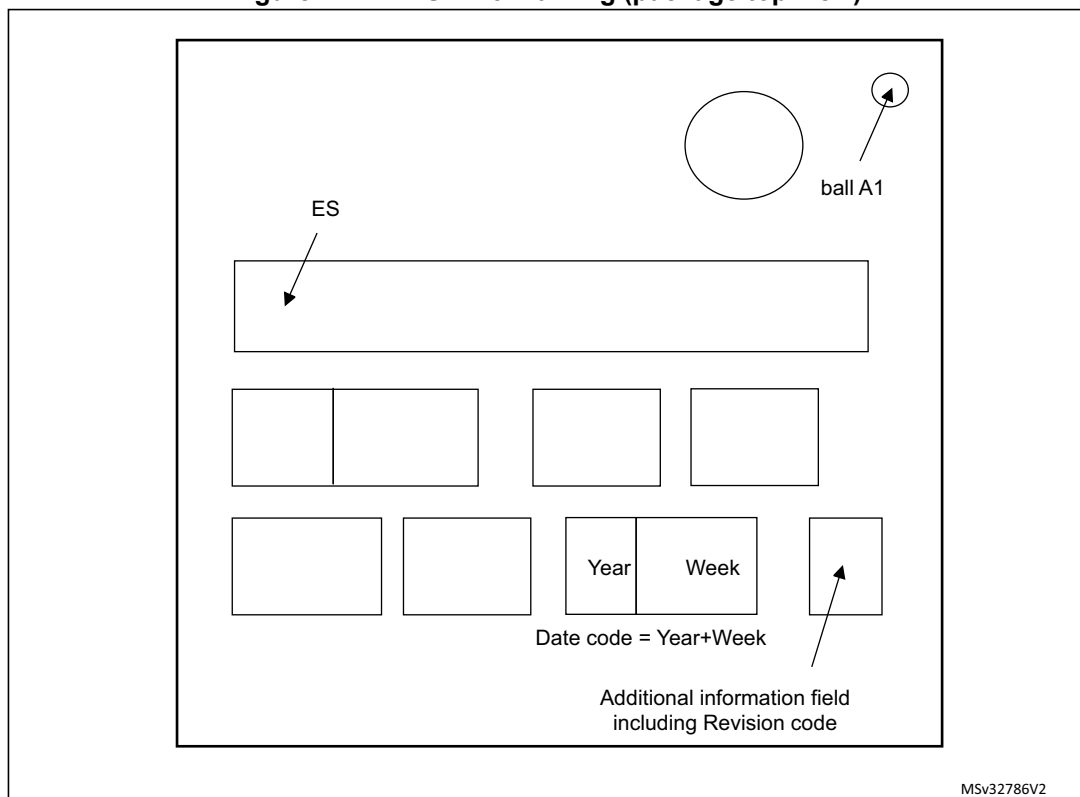
Table 15. WLCSP143, 0.4 mm pitch wafer level chip scale package mechanical data

| Symbol | millimeters |        |       | inches <sup>(1)</sup> |        |        |
|--------|-------------|--------|-------|-----------------------|--------|--------|
|        | Min         | Typ    | Max   | Min                   | Typ    | Max    |
| A      | 0.525       | 0.555  | 0.585 | 0.0207                | 0.0219 | 0.0230 |
| A1     | -           | 0.175  | -     | -                     | 0.0069 | -      |
| A2     | -           | 0.380  | -     | -                     | 0.0150 | -      |
| A3     | 0.220       | 0.025  | 0.280 | 0.0087                | 0.0010 | 0.0110 |
| b      | -           | 0.250° | -     | -                     | 0.250° | -      |
| D      | 4.486       | 4.521  | 4.556 | 0.1766                | 0.1780 | 0.1794 |
| E      | 5.512       | 5.547  | 5.582 | 0.2170                | 0.2184 | 0.2198 |
| e      | -           | 0.400  | -     | -                     | 0.0157 | -      |
| e1     | -           | 4.000  | -     | -                     | 0.1575 | -      |
| e2     | -           | 4.800  | -     | -                     | 0.1890 | -      |
| F      | -           | 0.261  | -     | -                     | 0.0103 | -      |
| G      | -           | 0.374  | -     | -                     | 0.0147 | -      |
| eee    | -           | 0.050  | -     | -                     | 0.0020 | -      |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

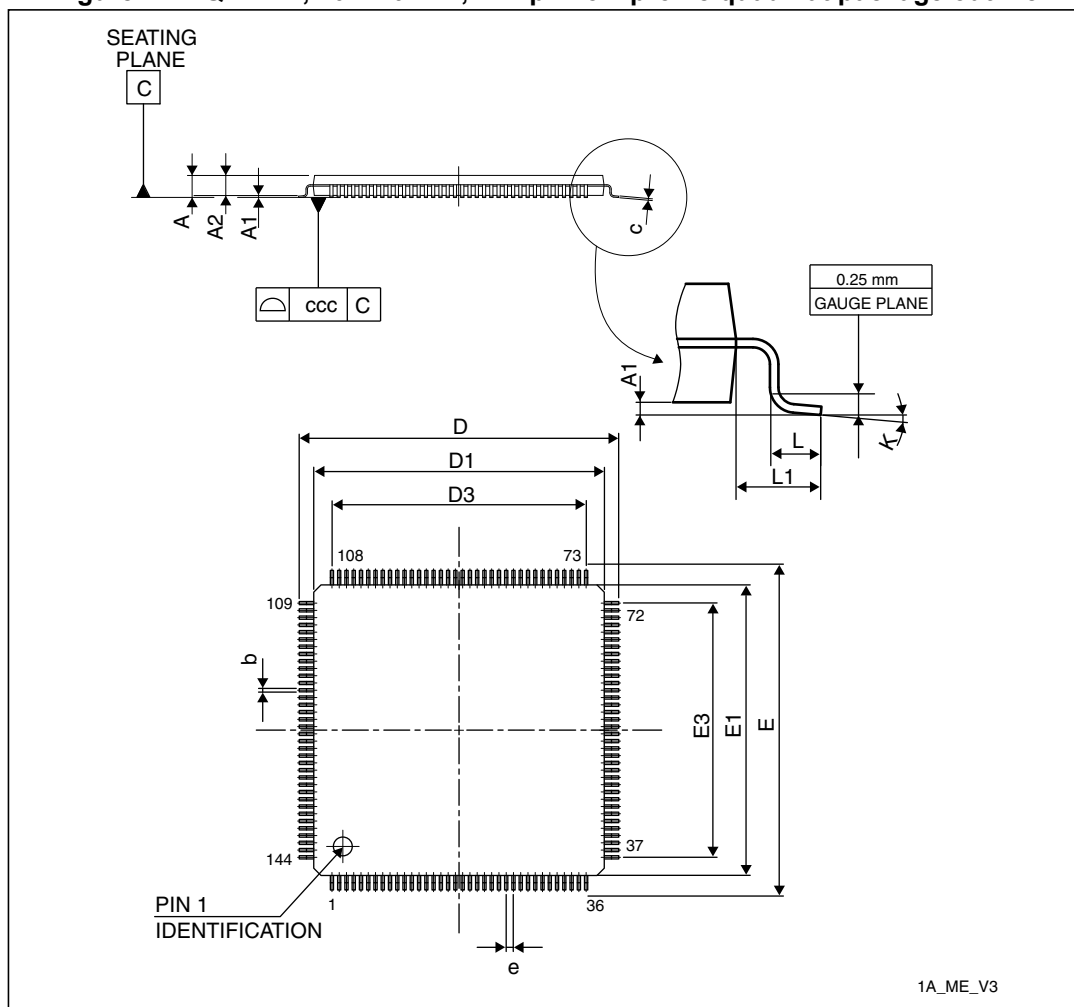
## Device marking

Figure 21. WLCSP143 marking (package top view)



1. Samples marked "ES" are to be considered as "Engineering Samples": i.e. they are intended to be sent to customer for electrical compatibility evaluation and may be used to start customer qualification where specifically authorized by ST in writing. In no event ST will be liable for any customer usage in production. Only if ST has authorized in writing the customer qualification Engineering Samples can be used for reliability qualification trials

Figure 22. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 16. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package mechanical data

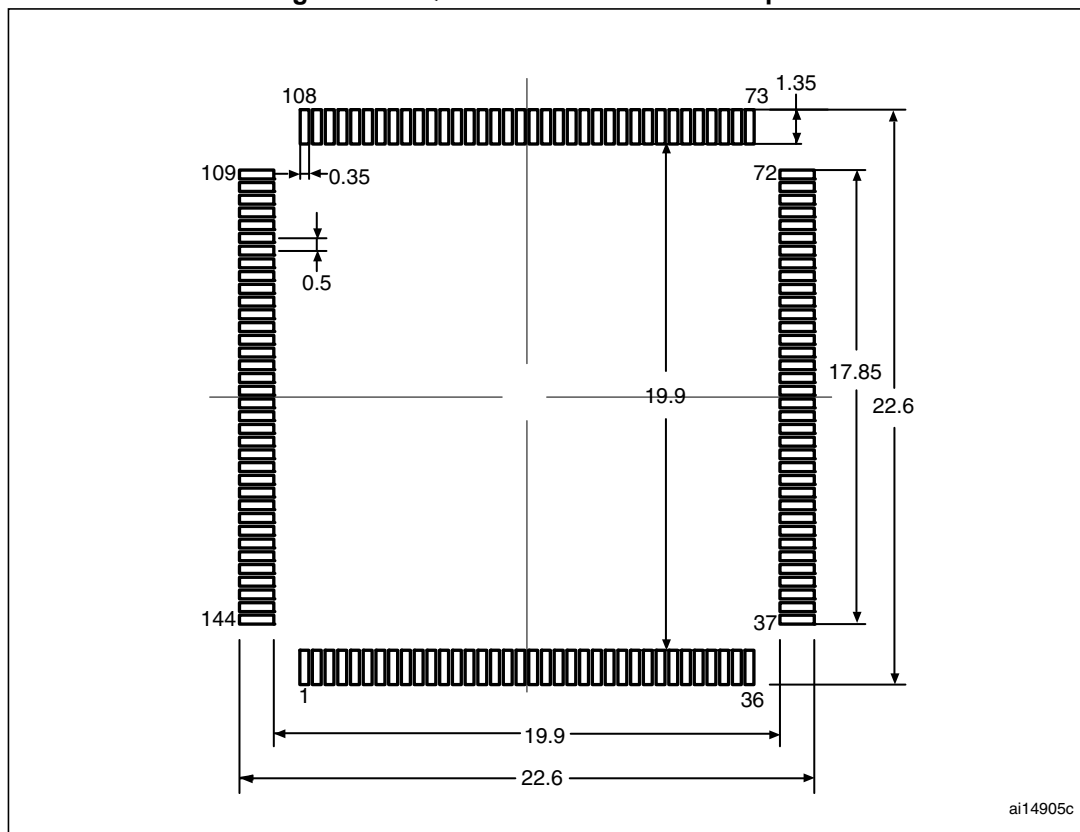
| Symbol | millimeters |        |        | inches <sup>(1)</sup> |        |        |
|--------|-------------|--------|--------|-----------------------|--------|--------|
|        | Min         | Typ    | Max    | Min                   | Typ    | Max    |
| A      | -           | -      | 1.600  | -                     | -      | 0.0630 |
| A1     | 0.050       | -      | 0.150  | 0.0020                | -      | 0.0059 |
| A2     | 1.350       | 1.400  | 1.450  | 0.0531                | 0.0551 | 0.0571 |
| b      | 0.170       | 0.220  | 0.270  | 0.0067                | 0.0087 | 0.0106 |
| c      | 0.090       | -      | 0.200  | 0.0035                | -      | 0.0079 |
| D      | 21.800      | 22.000 | 22.200 | 0.8583                | 0.8661 | 0.874  |
| D1     | 19.800      | 20.000 | 20.200 | 0.7795                | 0.7874 | 0.7953 |
| D3     | -           | 17.500 | -      | -                     | 0.689  | -      |

**Table 16. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package mechanical data (continued)**

| Symbol | millimeters |        |        | inches <sup>(1)</sup> |        |        |
|--------|-------------|--------|--------|-----------------------|--------|--------|
|        | Min         | Typ    | Max    | Min                   | Typ    | Max    |
| E      | 21.800      | 22.000 | 22.200 | 0.8583                | 0.8661 | 0.8740 |
| E1     | 19.800      | 20.000 | 20.200 | 0.7795                | 0.7874 | 0.7953 |
| E3     | -           | 17.500 | -      | -                     | 0.6890 | -      |
| e      | -           | 0.500  | -      | -                     | 0.0197 | -      |
| L      | 0.450       | 0.600  | 0.750  | 0.0177                | 0.0236 | 0.0295 |
| L1     | -           | 1.000  | -      | -                     | 0.0394 | -      |
| k      | 0°          | 3.5°   | 7°     | 0°                    | 3.5°   | 7°     |
| ccc    | -           | -      | 0.080  | -                     | -      | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

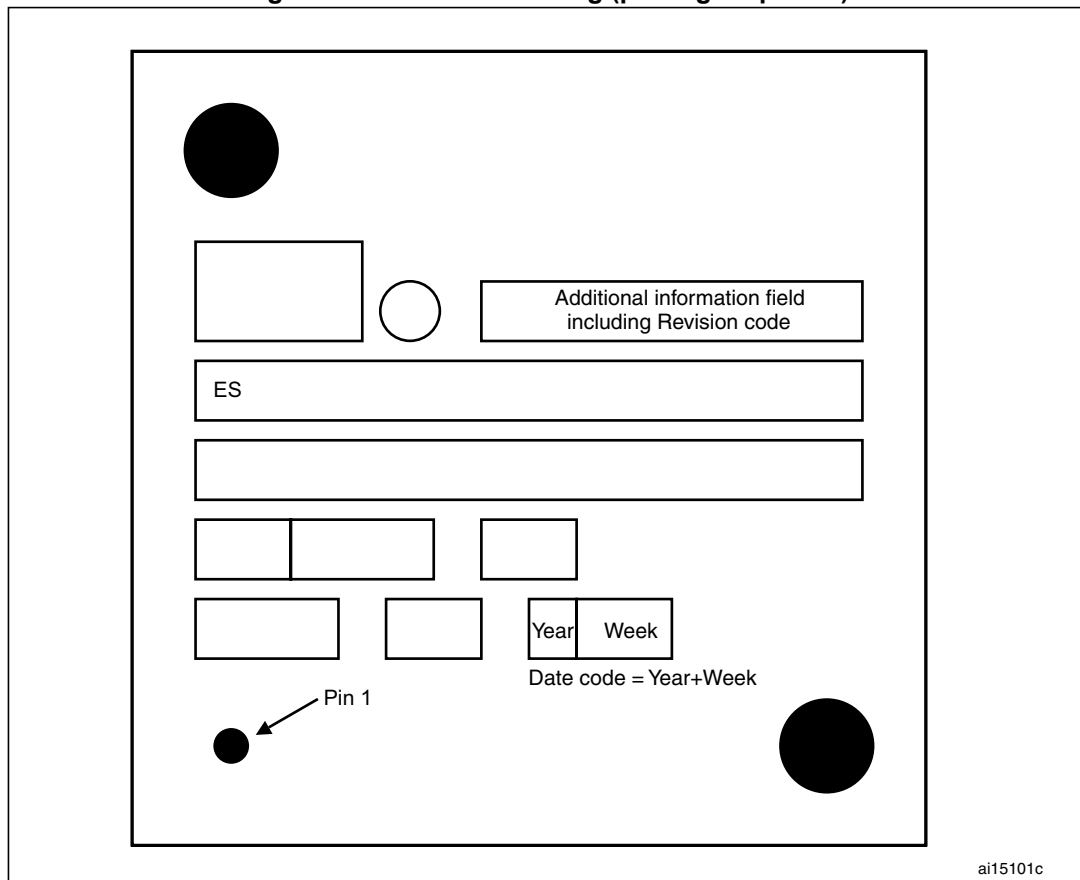
**Figure 23. LQFP144 recommended footprint**



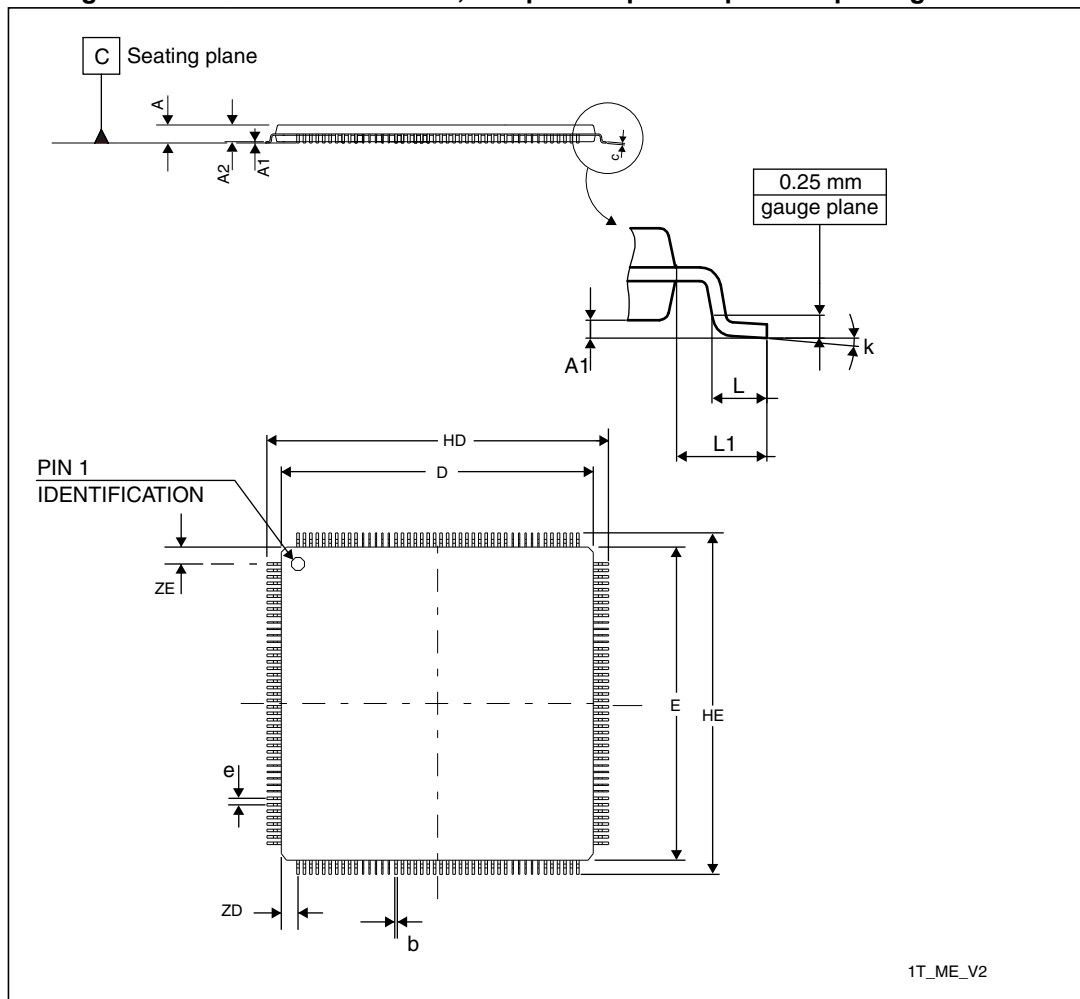
1. Dimensions are expressed in millimeters.

## Device marking

Figure 24. LQFP144 marking (package top view)



1. Samples marked "ES" are to be considered as "Engineering Samples": i.e. they are intended to be sent to customer for electrical compatibility evaluation and may be used to start customer qualification where specifically authorized by ST in writing. In no event ST will be liable for any customer usage in production. Only if ST has authorized in writing the customer qualification Engineering Samples can be used for reliability qualification trials.

**Figure 25. LQFP176 24 x 24 mm, 176-pin low-profile quad flat package outline**

1. Drawing is not to scale.

**Table 17. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package mechanical data**

| Symbol | millimeters |       |        | inches <sup>(1)</sup> |        |        |
|--------|-------------|-------|--------|-----------------------|--------|--------|
|        | Min         | Typ   | Max    | Min                   | Typ    | Max    |
| A      | -           | -     | 1.600  | -                     | -      | 0.0630 |
| A1     | 0.050       | -     | 0.150  | 0.0020                | -      | 0.0059 |
| A2     | 1.350       | -     | 1.450  | 0.0531                | -      | 0.0060 |
| b      | 0.170       | -     | 0.270  | 0.0067                | -      | 0.0106 |
| C      | 0.090       | -     | 0.200  | 0.0035                | -      | 0.0079 |
| D      | 23.900      | -     | 24.100 | 0.9409                | -      | 0.9488 |
| E      | 23.900      | -     | 24.100 | 0.9409                | -      | 0.9488 |
| e      | -           | 0.500 | -      | -                     | 0.0197 | -      |
| HD     | 25.900      | -     | 26.100 | 1.0200                | -      | 1.0276 |

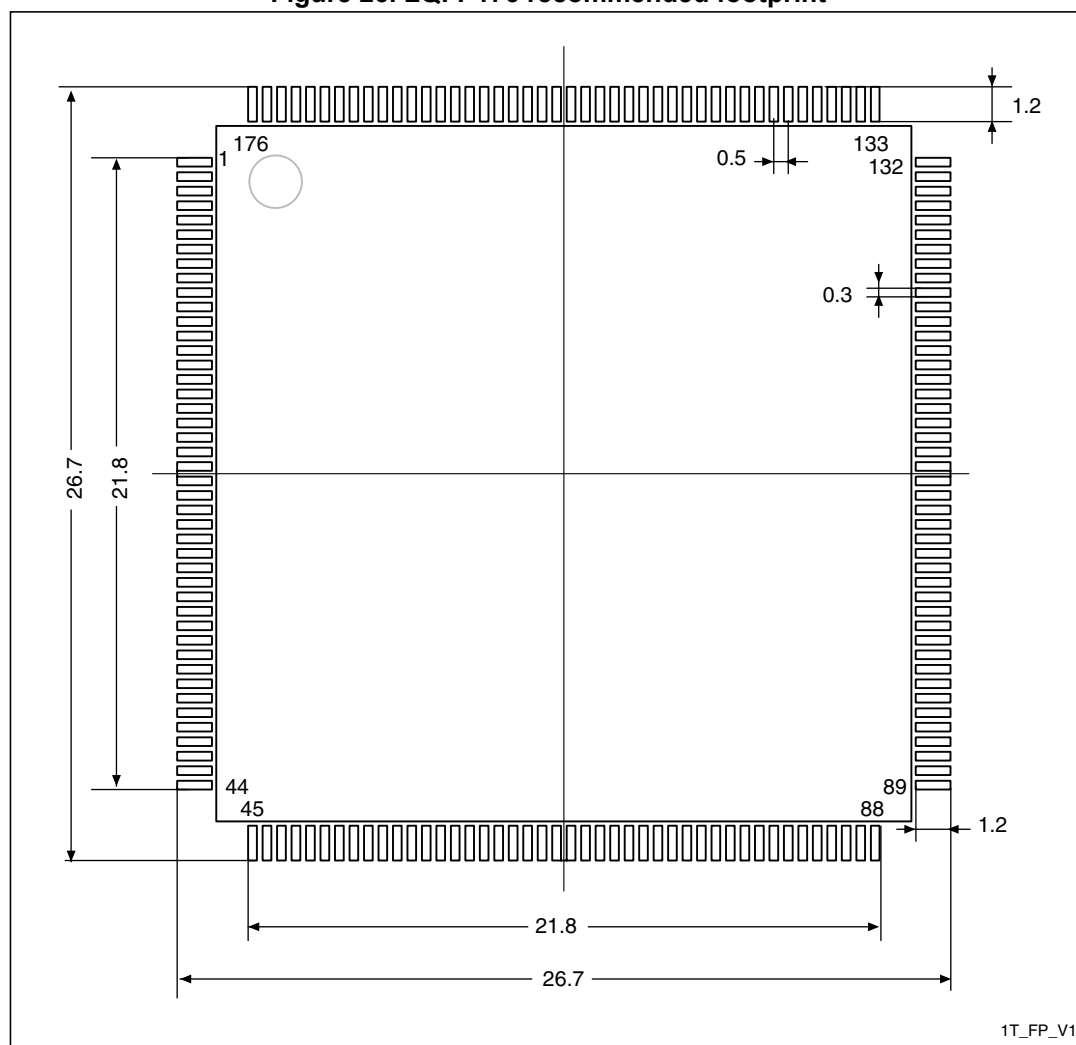


**Table 17. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package  
mechanical data (continued)**

| Symbol | millimeters |       |        | inches <sup>(1)</sup> |        |        |
|--------|-------------|-------|--------|-----------------------|--------|--------|
|        | Min         | Typ   | Max    | Min                   | Typ    | Max    |
| HE     | 25.900      | -     | 26.100 | 1.0200                | -      | 1.0276 |
| L      | 0.450       | -     | 0.750  | 0.0177                | -      | 0.0295 |
| L1     | -           | 1.000 | -      | -                     | 0.0394 | -      |
| ZD     | -           | 1.250 | -      | -                     | 0.0492 | -      |
| ZE     | -           | 1.250 | -      | -                     | 0.0492 | -      |
| ccc    | -           | -     | 0.080  | -                     | -      | 0.0031 |
| k      | 0 °         | -     | 7 °    | 0 °                   | -      | 7 °    |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

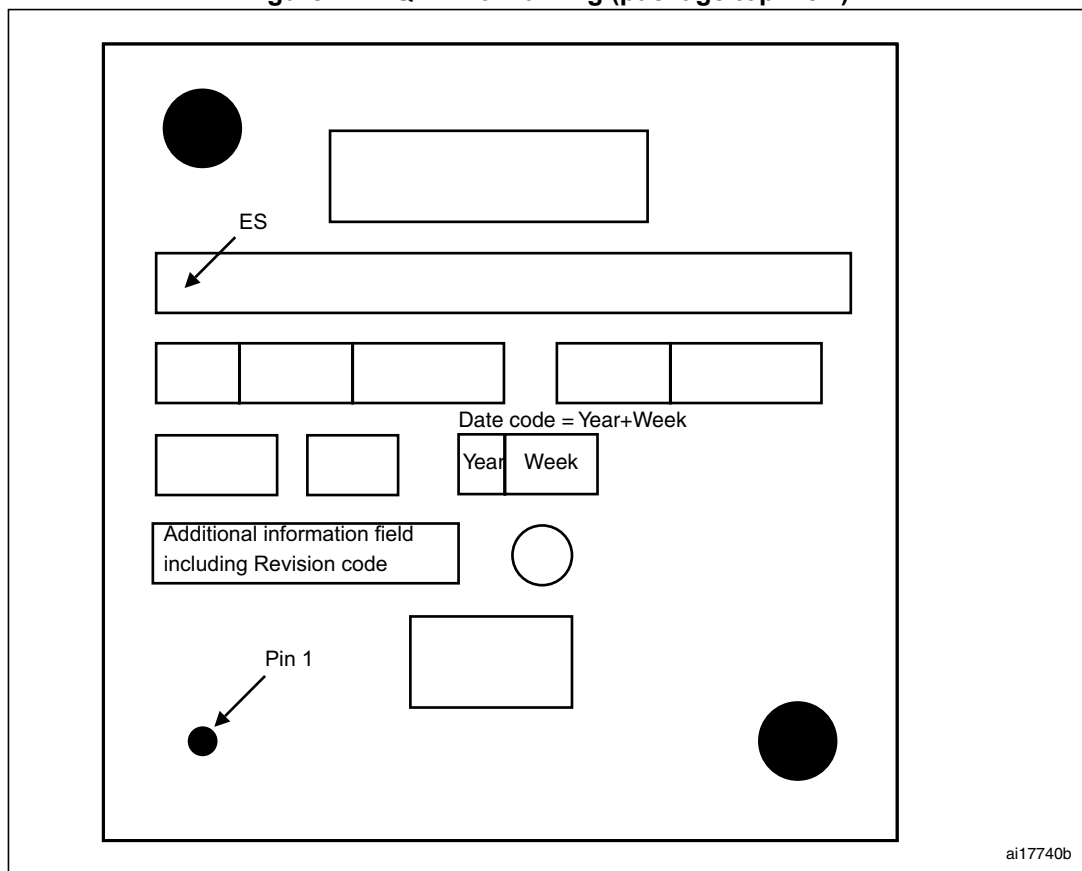
Figure 26. LQFP176 recommended footprint



1. Dimensions are expressed in millimeters.

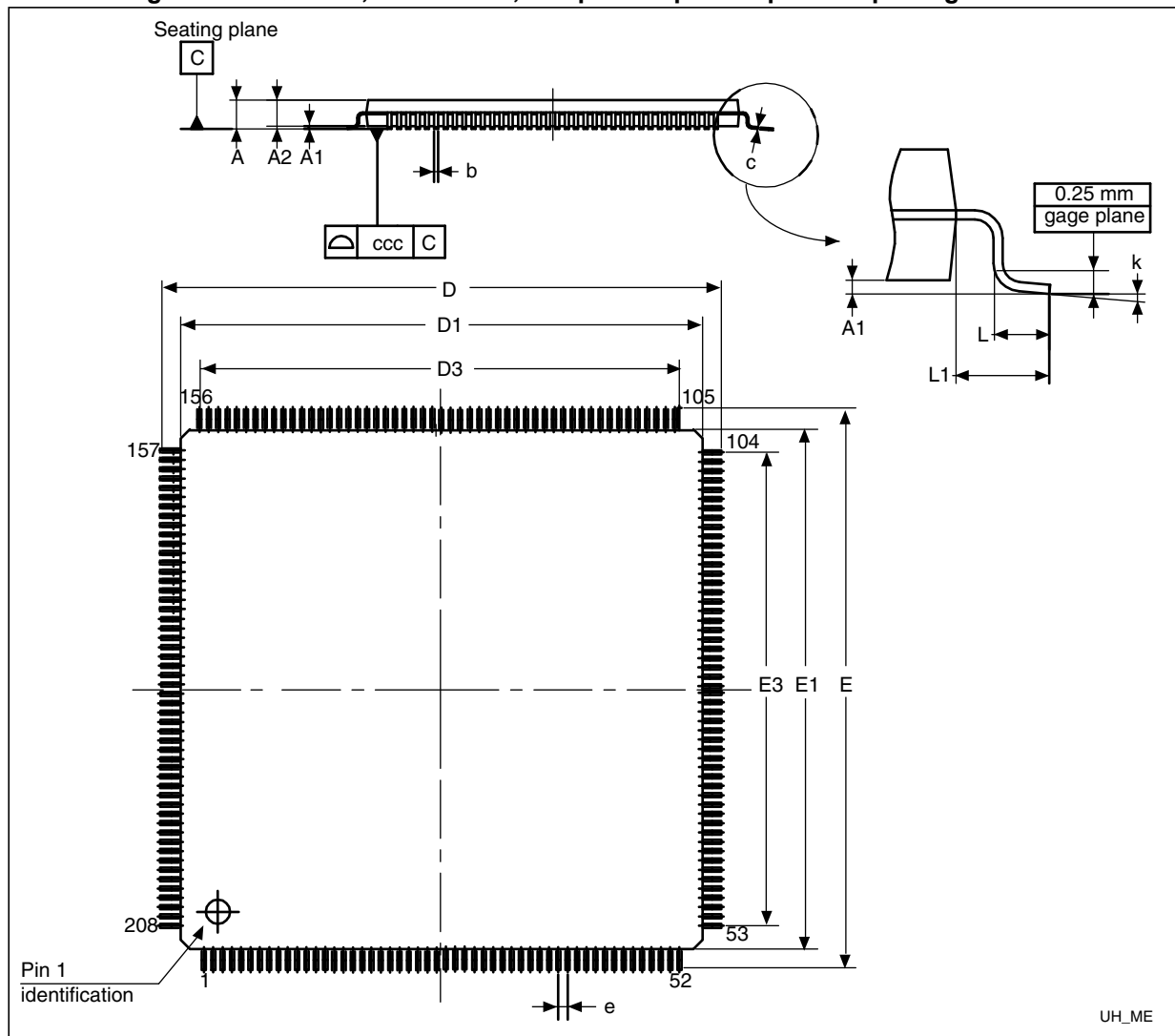
## Device marking

Figure 27. LQFP176 marking (package top view)



1. Samples marked "ES" are to be considered as "Engineering Samples": i.e. they are intended to be sent to customer for electrical compatibility evaluation and may be used to start customer qualification where specifically authorized by ST in writing. In no event ST will be liable for any customer usage in production. Only if ST has authorized in writing the customer qualification Engineering Samples can be used for reliability qualification trials.

Figure 28. LQFP208, 28 x 28 mm, 208-pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 18. LQFP208, 28 x 28 mm, 208-pin low-profile quad flat package mechanical data

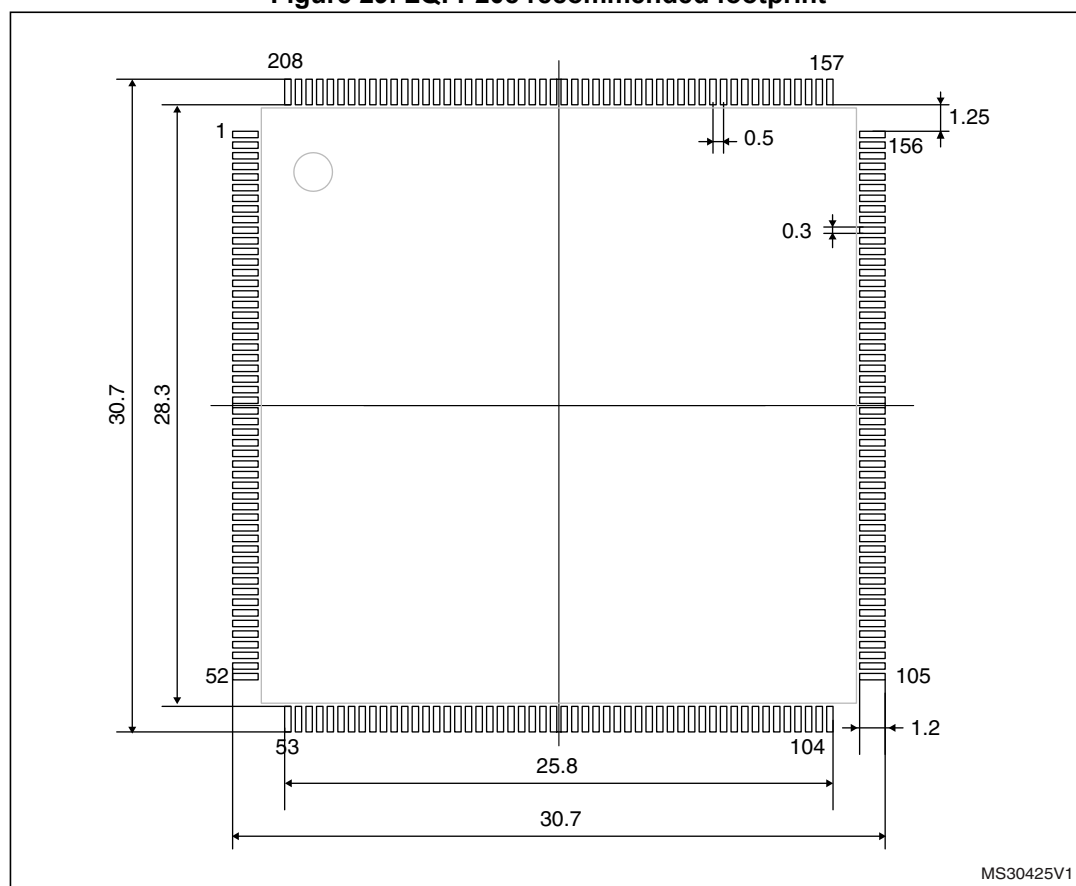
| Symbol | millimeters |        |        | inches <sup>(1)</sup> |        |        |
|--------|-------------|--------|--------|-----------------------|--------|--------|
|        | Min         | Typ    | Max    | Min                   | Typ    | Max    |
| A      | -           | -      | 1.600  | --                    | -      | 0.0630 |
| A1     | 0.050       | -      | 0.150  | 0.0020                | -      | 0.0059 |
| A2     | 1.350       | 1.400  | 1.450  | 0.0531                | 0.0551 | 0.0571 |
| b      | 0.170       | 0.220  | 0.270  | 0.0067                | 0.0087 | 0.0106 |
| c      | 0.090       | -      | 0.200  | 0.0035                | -      | 0.0079 |
| D      | 29.800      | 30.000 | 30.200 | 1.1732                | 1.1811 | 1.1890 |
| D1     | 27.800      | 28.000 | 28.200 | 1.0945                | 1.1024 | 1.1102 |

**Table 18. LQFP208, 28 x 28 mm, 208-pin low-profile quad flat package mechanical data (continued)**

| Symbol | millimeters |        |        | inches <sup>(1)</sup> |        |        |
|--------|-------------|--------|--------|-----------------------|--------|--------|
|        | Min         | Typ    | Max    | Min                   | Typ    | Max    |
| D3     | -           | 25.500 | -      | -                     | 1.0039 | -      |
| E      | 29.800      | 30.000 | 30.200 | 1.1732                | 1.1811 | 1.1890 |
| E1     | 27.800      | 28.000 | 28.200 | 1.0945                | 1.1024 | 1.1102 |
| E3     | -           | 25.500 | -      | -                     | 1.0039 | -      |
| e      | -           | 0.500  | -      | -                     | 0.0197 | -      |
| L      | 0.450       | 0.600  | 0.750  | 0.0177                | 0.0236 | 0.0295 |
| L1     | -           | 1.000  | -      | -                     | 0.0394 | -      |
| k      | 0°          | 3.5°   | 7.0°   | 0°                    | 3.5°   | 7.0°   |
| ccc    | -           | -      | 0.080  | -                     | -      | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

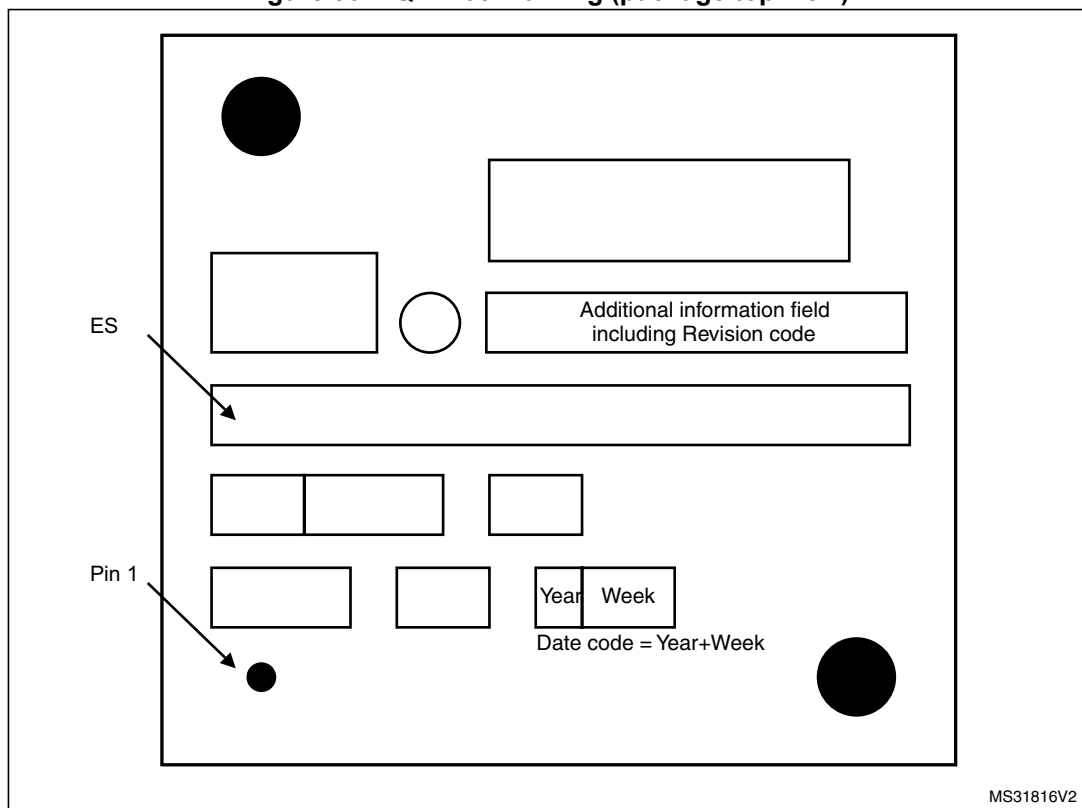
**Figure 29. LQFP208 recommended footprint**



1. Dimensions are expressed in millimeters.

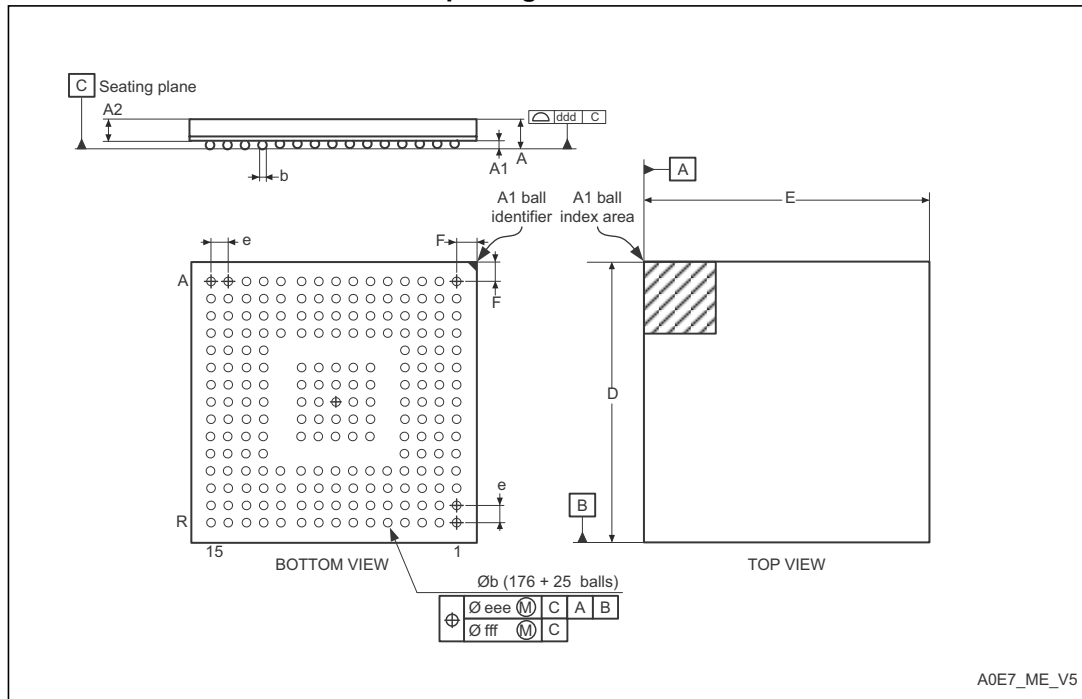
## Device marking

Figure 30. LQFP208 marking (package top view)



1. Samples marked "ES" are to be considered as "Engineering Samples": i.e. they are intended to be sent to customer for electrical compatibility evaluation and may be used to start customer qualification where specifically authorized by ST in writing. In no event ST will be liable for any customer usage in production. Only if ST has authorized in writing the customer qualification Engineering Samples can be used for reliability qualification trials.

**Figure 31. UFBGA176+25 - ultra thin fine pitch ball grid array 10 × 10 × 0.6 mm, package outline**



1. Drawing is not to scale.

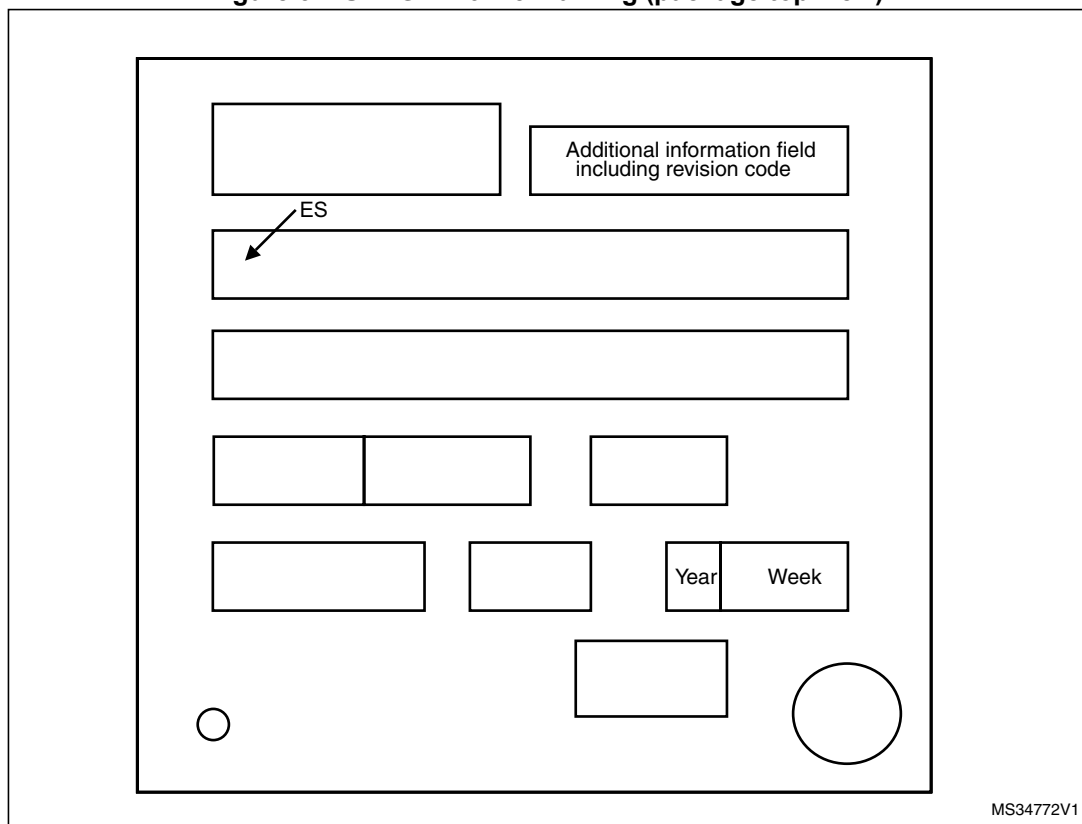
**Table 19. UFBGA176+25 - ultra thin fine pitch ball grid array 10 × 10 × 0.6 mm mechanical data**

| Symbol | millimeters |        |        | inches <sup>(1)</sup> |        |        |
|--------|-------------|--------|--------|-----------------------|--------|--------|
|        | Min         | Typ    | Max    | Min                   | Typ    | Max    |
| A      | 0.460       | 0.530  | 0.600  | 0.0181                | 0.0209 | 0.0236 |
| A1     | 0.050       | 0.080  | 0.110  | 0.002                 | 0.0031 | 0.0043 |
| A2     | 0.400       | 0.450  | 0.500  | 0.0157                | 0.0177 | 0.0197 |
| b      | 0.230       | 0.280  | 0.330  | 0.0091                | 0.0110 | 0.0130 |
| D      | 9.950       | 10.000 | 10.050 | 0.3917                | 0.3937 | 0.3957 |
| E      | 9.950       | 10.000 | 10.050 | 0.3917                | 0.3937 | 0.3957 |
| e      | -           | 0.650  | -      | -                     | 0.0256 | -      |
| F      | 0.400       | 0.450  | 0.500  | 0.0157                | 0.0177 | 0.0197 |
| ddd    | -           | -      | 0.080  | -                     | -      | 0.0031 |
| eee    | -           | -      | 0.150  | -                     | -      | 0.0059 |
| fff    | -           | -      | 0.080  | -                     | -      | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

## Device marking

Figure 32. UFBGA176+25 marking (package top view)



1. Samples marked "ES" are to be considered as "Engineering Samples": i.e. they are intended to be sent to customer for electrical compatibility evaluation and may be used to start customer qualification where specifically authorized by ST in writing. In no event ST will be liable for any customer usage in production. Only if ST has authorized in writing the customer qualification Engineering Samples can be used for reliability qualification trials.



The drawing consists of three main views: a side view at the top, a bottom view at the bottom left, and a top view at the bottom right.

- Side View:** Shows a horizontal array of balls. A "Seating plane" is indicated by a Z-axis symbol. Vertical dimensions A2, A1, and A are shown. A feature is labeled "ddd Z".
- Bottom View:** A 15x15 grid of circles representing balls. Dimensions include E1, e, F, D1, and e. A "15" is at the bottom left and a "1" is at the bottom right. A "BOTTOM VIEW" label points to the grid.
- Top View:** Shows the array from above. Dimensions include E, D, and e. A shaded rectangular area is present. A "TOP VIEW" label points to the view. A "Y" axis symbol is shown.

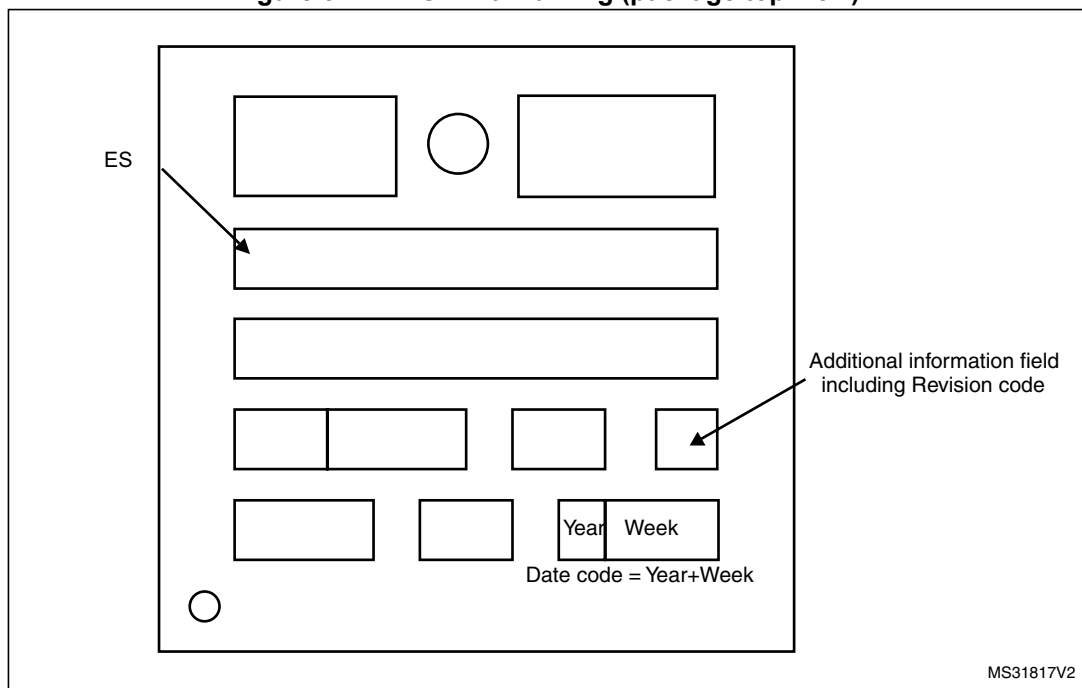
Additional details include:

- "A1 ball identifier" and "A1 ball index area" labels pointing to specific locations in the bottom and top views.
- A detail callout at the bottom center showing a cross-section of a ball with dimensions:  $\varnothing eee$ ,  $\varnothing fff$ , and a Z-axis symbol.
- A detail callout at the bottom right showing a cross-section of a ball with dimensions:  $\varnothing eee$ ,  $\varnothing fff$ , and a Z-axis symbol.
- A detail callout at the bottom right showing a cross-section of a ball with dimensions:  $\varnothing eee$ ,  $\varnothing fff$ , and a Z-axis symbol.
- A detail callout at the bottom right showing a cross-section of a ball with dimensions:  $\varnothing eee$ ,  $\varnothing fff$ , and a Z-axis symbol.

| Symbol | millimeters |        |        | inches <sup>(1)</sup> |        |        |
|--------|-------------|--------|--------|-----------------------|--------|--------|
|        | Min         | Typ    | Max    | Min                   | Typ    | Max    |
| A      | -           | -      | 1.100  | -                     | -      | 0.0433 |
| A1     | 0.150       | -      | -      | 0.0059                | -      | -      |
| A2     | -           | 0.760  | -      | -                     | 0.0299 | -      |
| A4     | -           | 0.210  | -      | -                     | 0.0083 | -      |
| b      | 0.350       | 0.400  | 0.450  | 0.0138                | 0.0157 | 0.0177 |
| D      | 12.850      | 13.000 | 13.150 | 0.5118                | 0.5118 | 0.5177 |
| D1     | -           | 11.200 | -      | -                     | 0.4409 | -      |
| E      | 12.850      | 13.000 | 13.150 | 0.5118                | 0.5118 | 0.5177 |
| E1     | -           | 11.200 | -      | -                     | 0.4409 | -      |
| e      | -           | 0.800  | -      | -                     | 0.0315 | -      |
| F      | -           | 0.900  | -      | -                     | 0.0354 | -      |
| ddd    | -           | -      | 0.080  | -                     | -      | 0.0031 |

## Device marking

Figure 34. TFBGA176 marking (package top view)



1. Samples marked "ES" are to be considered as "Engineering Samples": i.e. they are intended to be sent to customer for electrical compatibility evaluation and may be used to start customer qualification where specifically authorized by ST in writing. In no event ST will be liable for any customer usage in production. Only if ST has authorized in writing the customer qualification Engineering Samples can be used for reliability qualification trials.

## 5.2 Thermal characteristics

The maximum chip-junction temperature,  $T_J$  max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- $T_A$  max is the maximum ambient temperature in °C,
- $\Theta_{JA}$  is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D$  max is the sum of  $P_{INT}$  max and  $P_{I/O}$  max ( $P_D \text{ max} = P_{INT} \text{ max} + P_{I/O} \text{ max}$ ),
- $P_{INT}$  max is the product of  $I_{DD}$  and  $V_{DD}$ , expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$  max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual  $V_{OL} / I_{OL}$  and  $V_{OH} / I_{OH}$  of the I/Os at low and high level in the application.

**Table 21. Package thermal characteristics**

| Symbol        | Parameter                                                                   | Value | Unit |
|---------------|-----------------------------------------------------------------------------|-------|------|
| $\Theta_{JA}$ | Thermal resistance junction-ambient<br>LQFP100 - 14 × 14 mm / 0.5 mm pitch  | 43    | °C/W |
|               | Thermal resistance junction-ambient<br>WLCSP143                             | 31.2  |      |
|               | Thermal resistance junction-ambient<br>LQFP144 - 20 × 20 mm / 0.5 mm pitch  | 40    |      |
|               | Thermal resistance junction-ambient<br>LQFP176 - 24 × 24 mm / 0.5 mm pitch  | 38    |      |
|               | Thermal resistance junction-ambient<br>LQFP208 - 28 × 28 mm / 0.5 mm pitch  | 19    |      |
|               | Thermal resistance junction-ambient<br>UFBGA176 - 10 × 10 mm / 0.5 mm pitch | 39    |      |
|               | Thermal resistance junction-ambient<br>TFBGA216 - 13 × 13 mm / 0.8 mm pitch | 29    |      |

### Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from [www.jedec.org](http://www.jedec.org).

## 6 Part numbering

**Table 22. Ordering information scheme**

|                                                                                                  |       |   |     |   |   |   |   |     |  |  |  |  |  |  |  |  |
|--------------------------------------------------------------------------------------------------|-------|---|-----|---|---|---|---|-----|--|--|--|--|--|--|--|--|
| Example:                                                                                         | STM32 | F | 756 | V | I | T | 6 | xxx |  |  |  |  |  |  |  |  |
| <b>Device family</b>                                                                             |       |   |     |   |   |   |   |     |  |  |  |  |  |  |  |  |
| STM32 = ARM-based 32-bit microcontroller                                                         |       |   |     |   |   |   |   |     |  |  |  |  |  |  |  |  |
| <b>Product type</b>                                                                              |       |   |     |   |   |   |   |     |  |  |  |  |  |  |  |  |
| F = general-purpose                                                                              |       |   |     |   |   |   |   |     |  |  |  |  |  |  |  |  |
| <b>Device subfamily</b>                                                                          |       |   |     |   |   |   |   |     |  |  |  |  |  |  |  |  |
| 756= STM32F756xx, USB OTG FS/HS, camera interface, Ethernet, LCD-TFT, cryptographic acceleration |       |   |     |   |   |   |   |     |  |  |  |  |  |  |  |  |
| <b>Pin count</b>                                                                                 |       |   |     |   |   |   |   |     |  |  |  |  |  |  |  |  |
| V = 100 pins                                                                                     |       |   |     |   |   |   |   |     |  |  |  |  |  |  |  |  |
| Z = 143 and 144 pins                                                                             |       |   |     |   |   |   |   |     |  |  |  |  |  |  |  |  |
| I = 176 pins                                                                                     |       |   |     |   |   |   |   |     |  |  |  |  |  |  |  |  |
| B = 208 pins                                                                                     |       |   |     |   |   |   |   |     |  |  |  |  |  |  |  |  |
| N = 216 pins                                                                                     |       |   |     |   |   |   |   |     |  |  |  |  |  |  |  |  |
| <b>Flash memory size</b>                                                                         |       |   |     |   |   |   |   |     |  |  |  |  |  |  |  |  |
| E = 512 Kbytes of Flash memory                                                                   |       |   |     |   |   |   |   |     |  |  |  |  |  |  |  |  |
| G = 1024 Kbytes of Flash memory                                                                  |       |   |     |   |   |   |   |     |  |  |  |  |  |  |  |  |
| <b>Package</b>                                                                                   |       |   |     |   |   |   |   |     |  |  |  |  |  |  |  |  |
| T = LQFP                                                                                         |       |   |     |   |   |   |   |     |  |  |  |  |  |  |  |  |
| I = UFBGA                                                                                        |       |   |     |   |   |   |   |     |  |  |  |  |  |  |  |  |
| H = TFBGA                                                                                        |       |   |     |   |   |   |   |     |  |  |  |  |  |  |  |  |
| Y = WLCSP                                                                                        |       |   |     |   |   |   |   |     |  |  |  |  |  |  |  |  |
| <b>Temperature range</b>                                                                         |       |   |     |   |   |   |   |     |  |  |  |  |  |  |  |  |
| 6 = Industrial temperature range, −40 to 85 °C.                                                  |       |   |     |   |   |   |   |     |  |  |  |  |  |  |  |  |
| 7 = Industrial temperature range, −40 to 105 °C.                                                 |       |   |     |   |   |   |   |     |  |  |  |  |  |  |  |  |
| <b>Options</b>                                                                                   |       |   |     |   |   |   |   |     |  |  |  |  |  |  |  |  |
| xxx = programmed parts                                                                           |       |   |     |   |   |   |   |     |  |  |  |  |  |  |  |  |
| TR = tape and reel                                                                               |       |   |     |   |   |   |   |     |  |  |  |  |  |  |  |  |

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

## Appendix A Recommendations when using internal reset OFF

When the internal reset is OFF, the following integrated features are no longer supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled.
- The brownout reset (BOR) circuitry must be disabled.
- The embedded programmable voltage detector (PVD) is disabled.
- $V_{BAT}$  functionality is no more available and VBAT pin should be connected to  $V_{DD}$ .
- The over-drive mode is not supported.

### A.1 Operating conditions

Table 23. Limitations depending on the operating power supply range

| Operating power supply range    | ADC operation                  | Maximum Flash memory access frequency with no wait states ( $f_{Flashmax}$ ) | Maximum Flash memory access frequency with wait states <sup>(1)(2)</sup> | I/O operation         | Possible Flash memory operations        |
|---------------------------------|--------------------------------|------------------------------------------------------------------------------|--------------------------------------------------------------------------|-----------------------|-----------------------------------------|
| $V_{DD} = 1.7$ to $2.1 V^{(3)}$ | Conversion time up to 1.2 Msps | 20 MHz <sup>(4)</sup>                                                        | 168 MHz with 8 wait states and over-drive OFF                            | – No I/O compensation | 8-bit erase and program operations only |

1. Applicable only when the code is executed from Flash memory. When the code is executed from RAM, no wait state is required.
2. Thanks to the ART accelerator and the 128-bit Flash memory, the number of wait states given here does not impact the execution speed from Flash memory since the ART accelerator allows to achieve a performance equivalent to 0 wait state program execution.
3.  $V_{DD}/V_{DDA}$  minimum value of 1.7 V, with the use of an external power supply supervisor (refer to [Section 2.17.1: Internal reset ON](#)).
4. Prefetch is not available.

## 7 Revision history

**Table 24. Document revision history**

| Date         | Revision | Changes          |
|--------------|----------|------------------|
| 09-Sept-2014 | 1        | Initial release. |

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