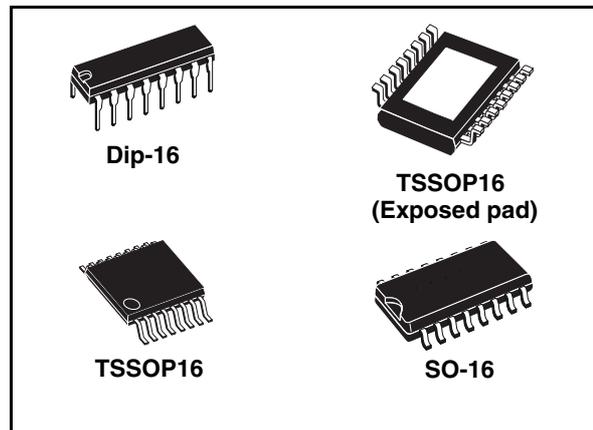


## Low voltage, low current power 8-bit shift register

### Features

- Low voltage power supply down to 3 V
- 8 constant current output channels
- Adjustable output current through external resistor
- Serial Data IN/Parallel data OUT
- 3.3 V micro driver-able
- Output current: 5-100 mA
- 30MHz clock frequency
- Available in high thermal efficiency TSSOP exposed pad
- ESD protection 2.5 kV HBM, 200 V MM



### Description

The STP08CP05 is a monolithic, low voltage, low current, power 8-bit shift register designed for LED panel displays. The STP08CP05 contains an 8-bit serial-in, parallel-out shift register that feeds a 8-bit D-type storage register. In the output stage, eight regulated current sources were designed to provide 5-100 mA constant current to drive the LEDs, the output current setup time is 11 ns (typ), thus improving the system performance.

The STP08CP05 is backward compatible in functionality and footprint with STP8C/L596. Through an external resistor, users can adjust the STP08CP05 output current, controlling in this way the light intensity of LEDs, in addition, user can

adjust LED's brightness intensity from 0% to 100% via  $\overline{OE}$  pin.

The STP08CP05 guarantees a 20 V output driving capability, allowing users to connect more LEDs in series. The high clock frequency, 30 MHz, also satisfies the system requirement of high volume data transmission. The 3.3 V of voltage supply is useful for applications that interface with any micro from 3.3 V. Compared with a standard TSSOP package, the TSSOP exposed pad increases heat dissipation capability by a 2.5 factor.

**Table 1. Device summary**

Order codes	Package	Packaging
STP08CP05B1R	DIP-16	25 parts per tube
STP08CP05MTR	SO-16 (Tape and reel)	2500 parts per reel
STP08CP05TTR	TSSOP16 (Tape and reel)	2500 parts per reel
STP08CP05XTTR	TSSOP16 exposed-pad (Tape and reel)	2500 parts per reel

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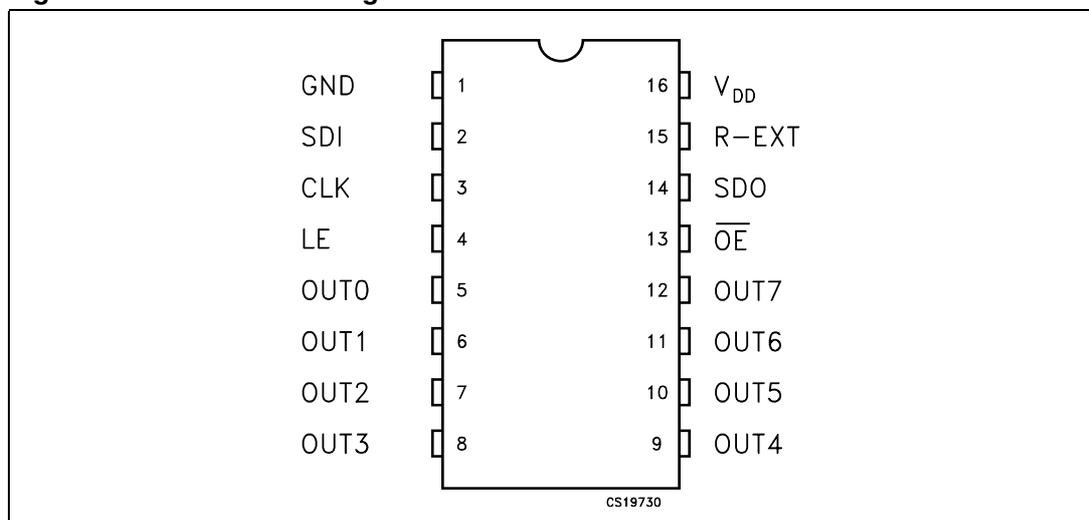
# 1 Summary description

**Table 2. Typical current accuracy**

Output voltage	Current accuracy		Output current
	Between bits	Between ICs	
≥1.3 V	±1.5 %	±3 %	20 to 100 mA

## 1.1 Pin connection and description

**Figure 1. Connections diagram**



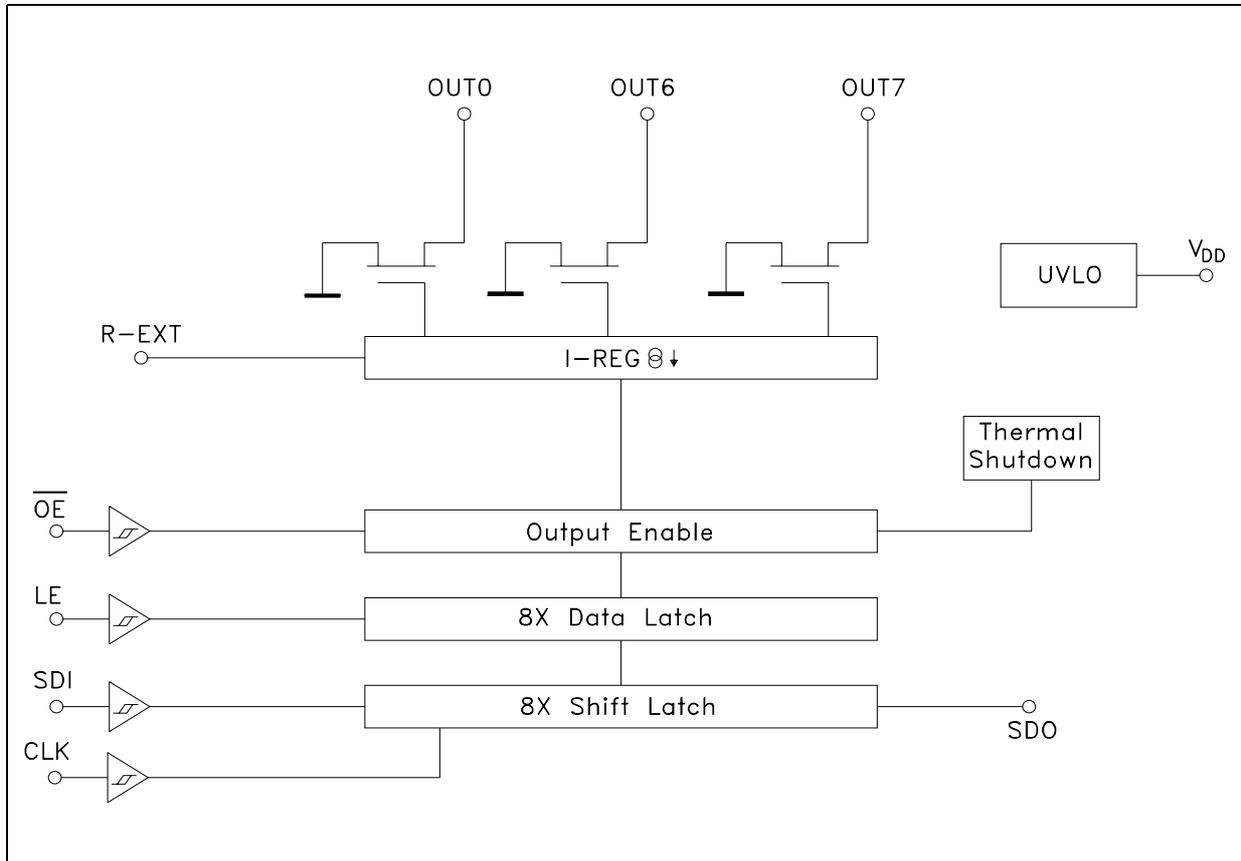
*Note: The Exposed-pad is electrically not connected*

**Table 3. Pin description**

Pin N°	Symbol	Name and function
1	GND	Ground terminal
2	SDI	Serial data input terminal
3	CLK	Clock input terminal
4	LE	Latch input terminal
5-12	OUT 0-7	Output terminal
13	$\overline{OE}$	Output enable input terminal (active low)
14	SDO	Serial data out terminal
15	R-EXT	Constant current programming
16	$V_{DD}$	5 V supply voltage terminal

## 2 Block diagram

Figure 2. Block diagram



### 3 Maximum rating

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

#### 3.1 Absolute maximum ratings

**Table 4. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply voltage $I_{GND}$	0 to 7	V
$V_O$	Output voltage	-0.5 to 20	V
$I_O$	Output current	100	mA
$I_{GND}$	GND terminal current	800	mA
$f_{CLK}$	Clock frequency	50	MHz
$T_{OPR}$	Operating temperature range	-40 to +125	°C
$T_{STG}$	Storage temperature range	-55 to +150	°C

#### 3.2 Thermal data

**Table 5. Thermal data**

Symbol	Parameter	DIP-16	SO-16	TSSOP-16	TSSOP-16 <sup>(1)</sup> (exposed pad)	Unit
$R_{thJA}$	Thermal resistance junction-ambient	90	125	140	37.5	°C/W

1. The Exposed-Pad should be soldered to the PBC to realize the thermal benefits

### 3.3 Recommended operating conditions

**Table 6. Recommended operating conditions**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{DD}$	Supply voltage		3.0		5.5	V
$V_O$	Output voltage				20	V
$I_O$	Output current	OUTn	5		100	mA
$I_{OH}$	Output current	SERIAL-OUT			+1	mA
$I_{OL}$	Output current	SERIAL-OUT			-1	mA
$V_{IH}$	Input voltage		$0.7 V_{DD}$		$V_{DD}+0.3$	V
$V_{IL}$	Input voltage		-0.3		$0.3 V_{DD}$	V
$t_{wLAT}$	LE pulse width	$V_{DD} = 3.0$ to $5.0V$	20			ns
$t_{wCLK}$	CLK pulse width		20			ns
$t_{wEN}$	$\overline{OE}$ pulse width		200			ns
$t_{SETUP(D)}$	Setup time for DATA		7			ns
$t_{HOLD(D)}$	Hold time for DATA		4			ns
$t_{SETUP(L)}$	Setup time for LATCH		15			ns
$f_{CLK}$	Clock frequency		Cascade operation <sup>(1)</sup>			30

1. In order to achieve high cascade data transfer, please consider  $t_r/t_f$  timings carefully.

## 4 Electrical characteristics

**Table 7. Electrical characteristics**

 ( $V_{DD} = 3.3\text{ V}$  to  $5\text{ V}$ ,  $T = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified.)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{IH}$	Input voltage high level		$0.7 V_{DD}$		$V_{DD}$	V
$V_{IL}$	Input voltage low level		GND		$0.3V_{DD}$	V
$I_{OH}$	Output leakage current	$V_{OH} = 20\text{ V}$		0.5	10	$\mu\text{A}$
$V_{OL}$	Output voltage (Serial-OUT)	$I_{OL} = 1\text{ mA}$		0.03	0.4	V
$V_{OH}$	Output voltage (Serial-OUT)	$I_{OH} = -1\text{ mA}$	$V_{OH} - V_{DD} = -0.4\text{ V}$			V
$I_{OL1}$	Output current	$V_O = 0.3\text{ V}$ , $R_{ext} = 3.9\text{ k}\Omega$	4.25	5	5.75	mA
$I_{OL2}$		$V_O = 0.3\text{ V}$ , $R_{ext} = 970\ \Omega$	19.4	20	20.6	
$I_{OL3}$		$V_O = 1.3\text{ V}$ , $R_{ext} = 190\ \Omega$	97	100	103	
$\Delta I_{OL1}$	Output current error between bit (All Output ON)	$V_O = 0.3\text{ V}$ , $R_{EXT} = 3.9\text{ k}\Omega$		$\pm 5$	$\pm 8$	%
$\Delta I_{OL2}$		$V_O = 0.3\text{ V}$ , $R_{EXT} = 970\ \Omega$		$\pm 1.5$	$\pm 2.75$	
$\Delta I_{OL3}$		$V_O = 1.3\text{ V}$ , $R_{EXT} = 190\ \Omega$		$\pm 1.2$	$\pm 2.5$	
$R_{SIN(up)}$	Pull-up resistor		150	300	600	$\text{K}\Omega$
$R_{SIN(down)}$	Pull-down resistor		100	200	400	$\text{K}\Omega$
$I_{DD(OFF1)}$	Supply current (OFF)	$R_{EXT} = 980$ OUT 0 to 7 = OFF		4	5	mA
$I_{DD(OFF2)}$		$R_{EXT} = 250$ OUT 0 to 7 = OFF		11.2	13.5	
$I_{DD(ON1)}$	Supply current (ON)	$R_{EXT} = 980$ OUT 0 to 7 = ON		4.5	5	
$I_{DD(ON2)}$		$R_{EXT} = 250$ OUT 0 to 7 = ON		11.7	13.5	
Thermal	Thermal protection <sup>(1)</sup>			170		$^{\circ}\text{C}$

1. Guaranteed by desing (not tested)  
The thermal protection switches OFF only the outputs

## 5 Switching characteristics

**Table 8. Switching characteristics** ( $V_{DD} = 5\text{ V}$ ,  $T = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified.)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit	
$t_{PLH1}$	Propagation delay time, CLK- $\overline{\text{OUTn}}$ , LE = H, $\overline{\text{OE}} = \text{L}$	$V_{DD} = 3.3\text{ V}$ $V_{IL} = \text{GND}$ $I_O = 20\text{ mA}$ $R_{EXT} = 1\text{ K}\Omega$ $V_{IH} = V_{DD}$ $C_L = 10\text{ pF}$ $V_L = 3.0\text{ V}$ $R_L = 60\text{ }\Omega$	$V_{DD} = 3.3\text{ V}$		35	50	ns
			$V_{DD} = 5\text{ V}$		18	28	
$t_{PLH2}$	Propagation delay time, LE- $\overline{\text{OUTn}}$ , $\overline{\text{OE}} = \text{L}$		$V_{DD} = 3.3\text{ V}$		48	74	ns
			$V_{DD} = 5\text{ V}$		30	50	
$t_{PLH3}$	Propagation delay time, $\overline{\text{OE}}-\overline{\text{OUTn}}$ , LE = H		$V_{DD} = 3.3\text{ V}$		55	82	ns
			$V_{DD} = 5\text{ V}$		37	58	
$t_{PLH}$	Propagation delay time, CLK-SDO		$V_{DD} = 3.3\text{ V}$		21	28	ns
			$V_{DD} = 5\text{ V}$		17	22	
$t_{PHL1}$	Propagation delay time, CLK- $\overline{\text{OUTn}}$ , LE = H, $\overline{\text{OE}} = \text{L}$		$V_{DD} = 3.3\text{ V}$		11	17	ns
			$V_{DD} = 5\text{ V}$		7	11	
$t_{PHL2}$	Propagation delay time, LE- $\overline{\text{OUTn}}$ , $\overline{\text{OE}} = \text{L}$		$V_{DD} = 3.3\text{ V}$		24	40	ns
			$V_{DD} = 5\text{ V}$		21	31	
$t_{PHL3}$	Propagation delay time, $\overline{\text{OE}}-\overline{\text{OUTn}}$ , LE = H		$V_{DD} = 3.3\text{ V}$		20	35	ns
			$V_{DD} = 5\text{ V}$		18	28	
$t_{PHL}$	Propagation delay time, CLK-SDO	$V_{DD} = 3.3\text{ V}$		24	32	ns	
		$V_{DD} = 5\text{ V}$		19	25		
$t_{ON}$	Output rise time 10~90% of voltage waveform	$V_{DD} = 3.3\text{ V}$		26	40	ns	
		$V_{DD} = 5\text{ V}$		11	17		
$t_{OFF}$	Output fall time 90~10% of voltage waveform	$V_{DD} = 3.3\text{ V}$		5	10	ns	
		$V_{DD} = 5\text{ V}$		4	8		
$t_r$	CLK rise time <sup>(1)</sup>				5000	ns	
$t_f$	CLK fall time <sup>(1)</sup>				5000	ns	

1. In order to achieve high cascade data transfer, please consider  $t_r/t_f$  timings carefully.

## 6 Equivalent circuit and outputs

Figure 3.  $\overline{OE}$  terminal

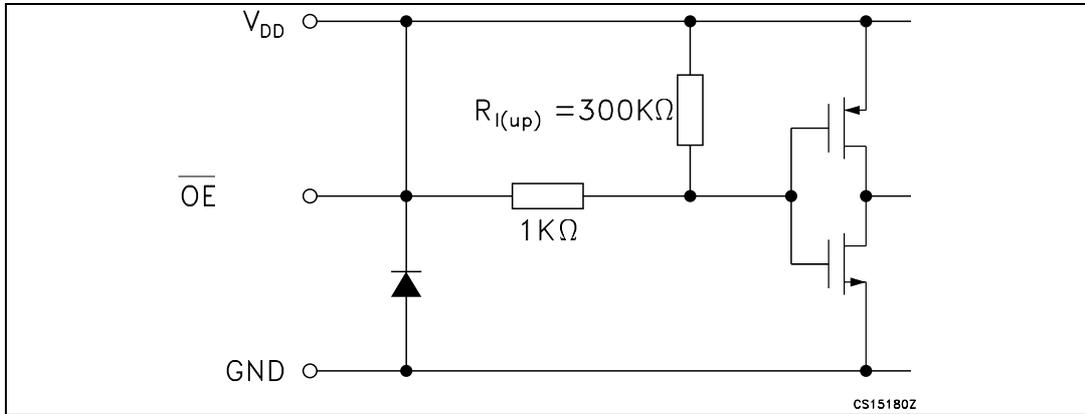


Figure 4. LE terminal

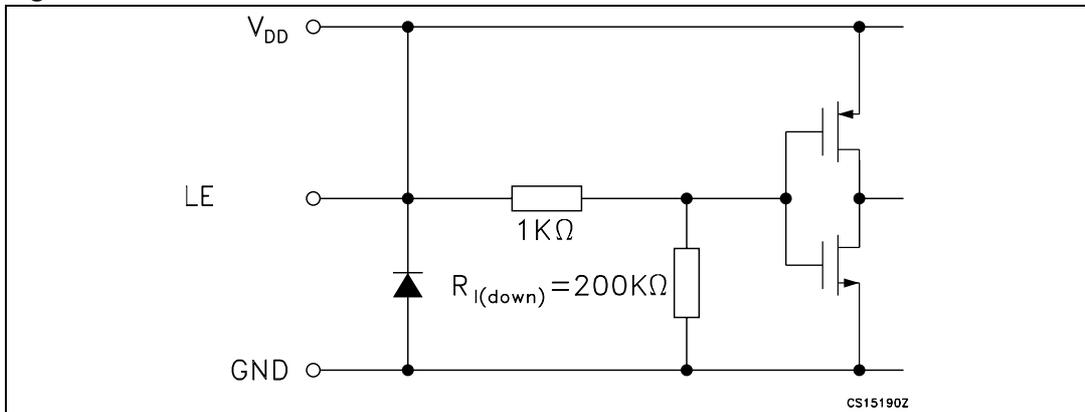


Figure 5. CLK, SDI terminal

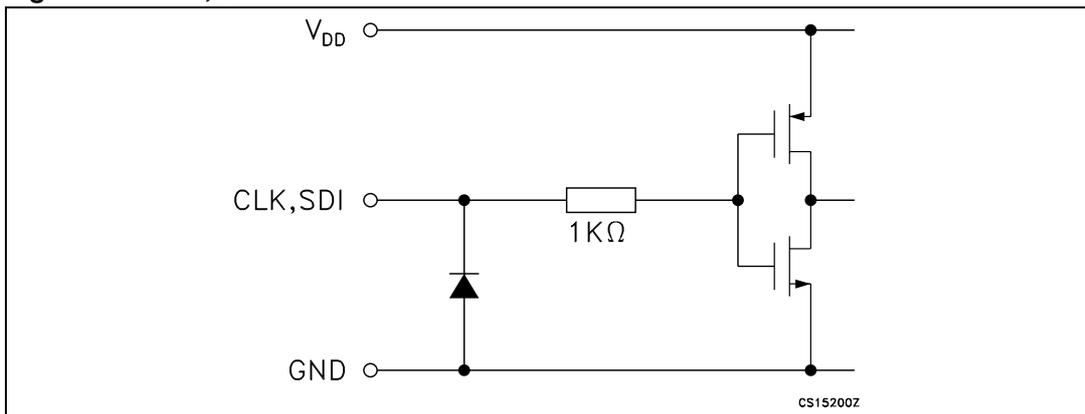
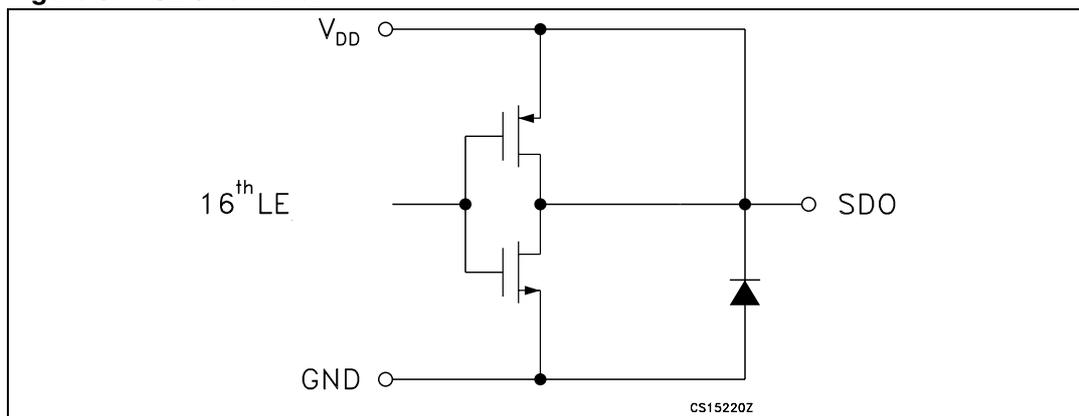


Figure 6. SDO terminal



## 7 Truth table and timing diagram

### 7.1 Truth table

Table 9. Truth table

Clock	LE	$\overline{OE}$	SDI	$\overline{OUT0}$ ..... $\overline{OUT0}$ ..... $\overline{OUT7}$	SDO
	H	L	Dn	Dn ..... Dn -5 ..... Dn -7	Dn -7
	L	L	Dn + 1	No Change	Dn -7
	H	L	Dn + 2	$\overline{Dn +2}$ ..... $\overline{Dn -3}$ ..... $\overline{Dn -5}$	Dn -5
	X	L	Dn + 3	$\overline{Dn +2}$ ..... $\overline{Dn -3}$ ..... $\overline{Dn -5}$	Dn -5
	X	H	Dn + 3	OFF	Dn -5

Note:  $OUT0$  to  $OUT7 = ON$  when  $Dn = H$ ;  $OUT0$  to  $OUT7 = OFF$  when  $Dn = L$ .

## 7.2 Timing diagram

Figure 7. Timing diagram

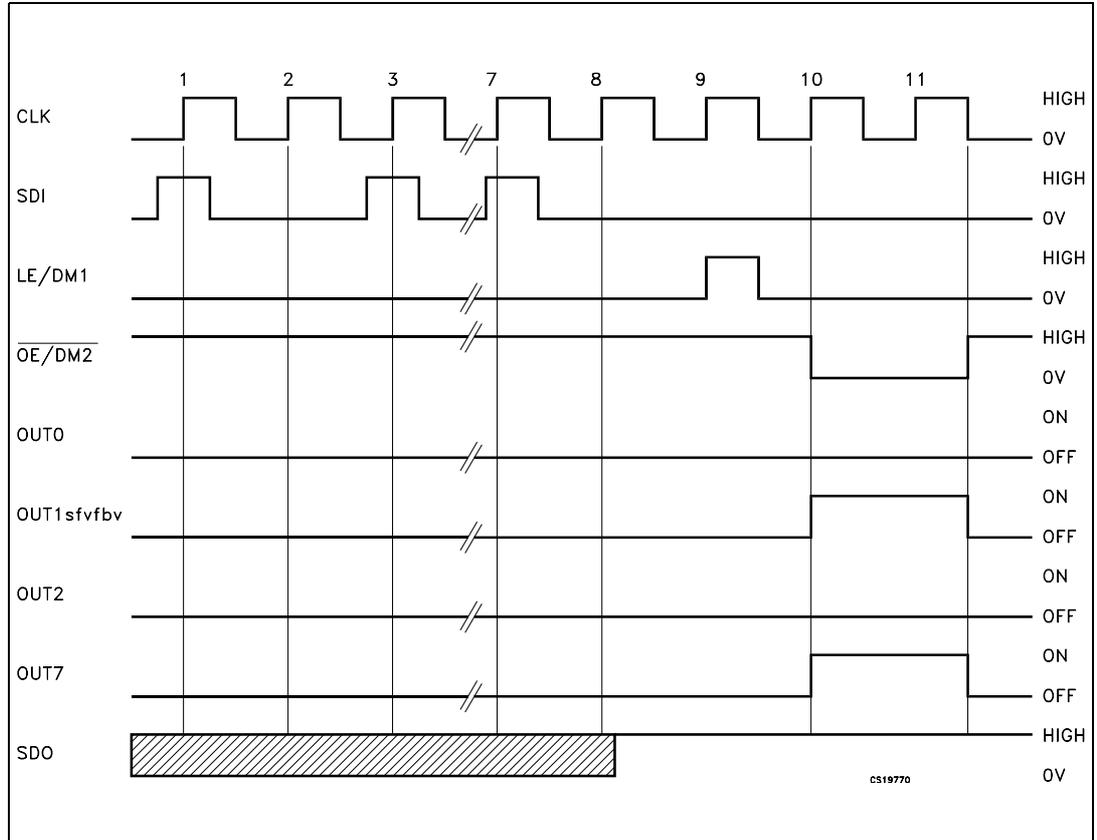


Figure 8. Clock, serial-in, serial-out

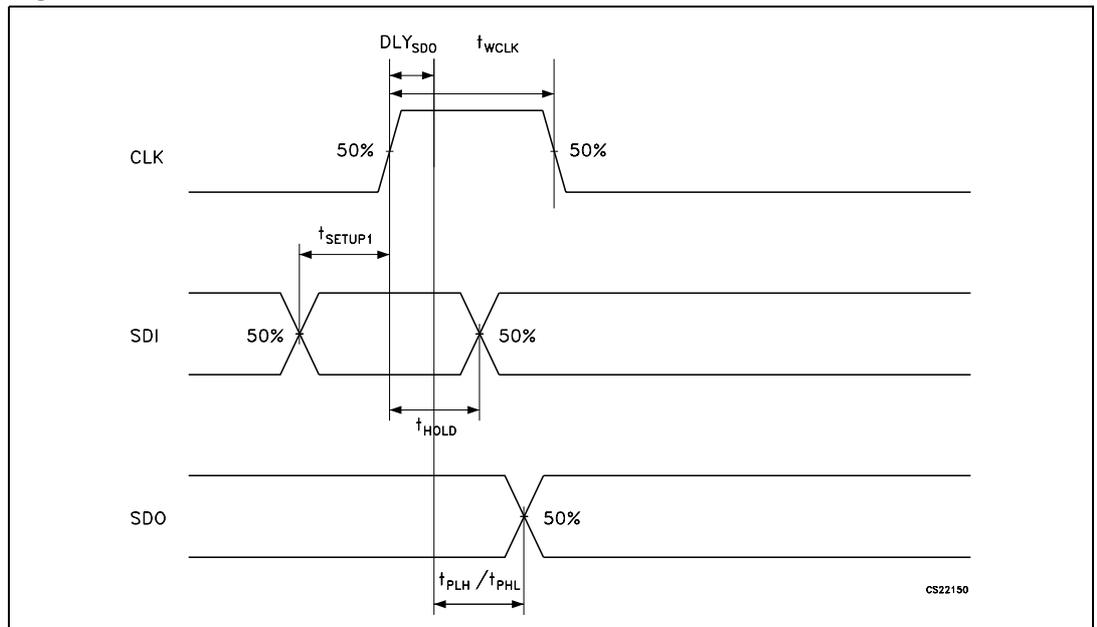


Figure 9. Clock, serial-in, latch, enable, outputs

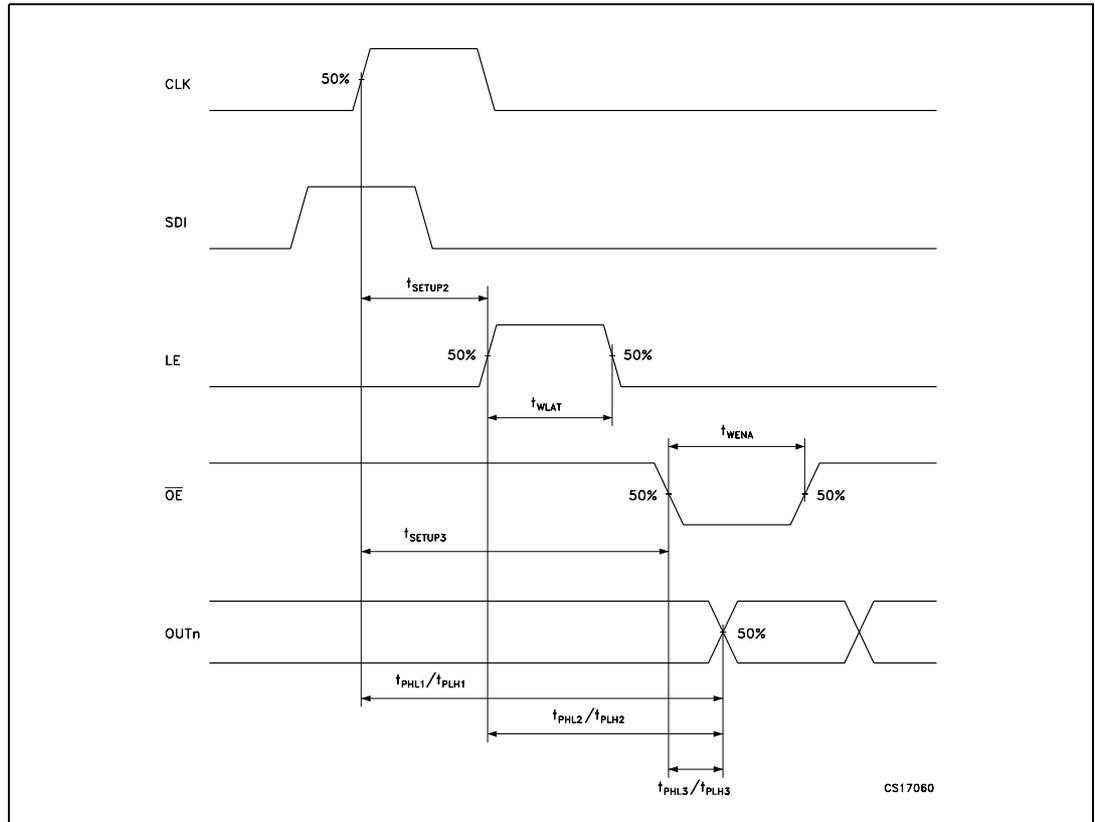
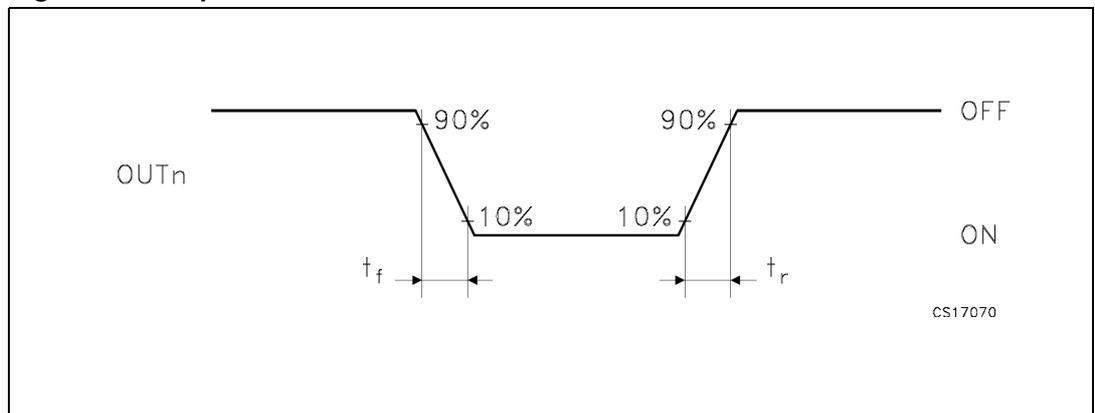


Figure 10. Outputs



## 8 Typical characteristics

Figure 11. Output current- $R_{EXT}$  resistor

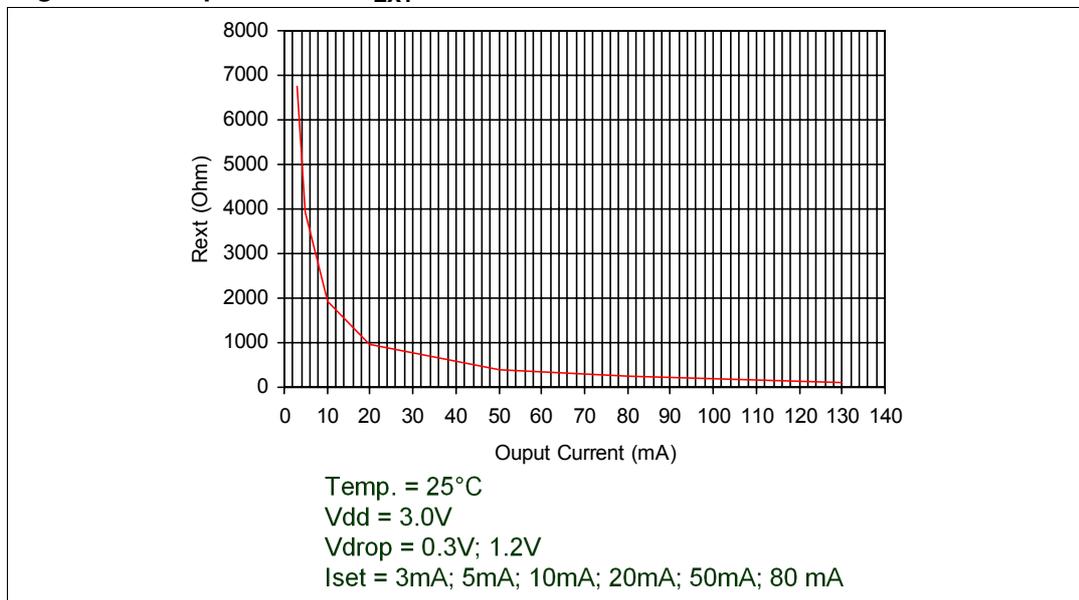
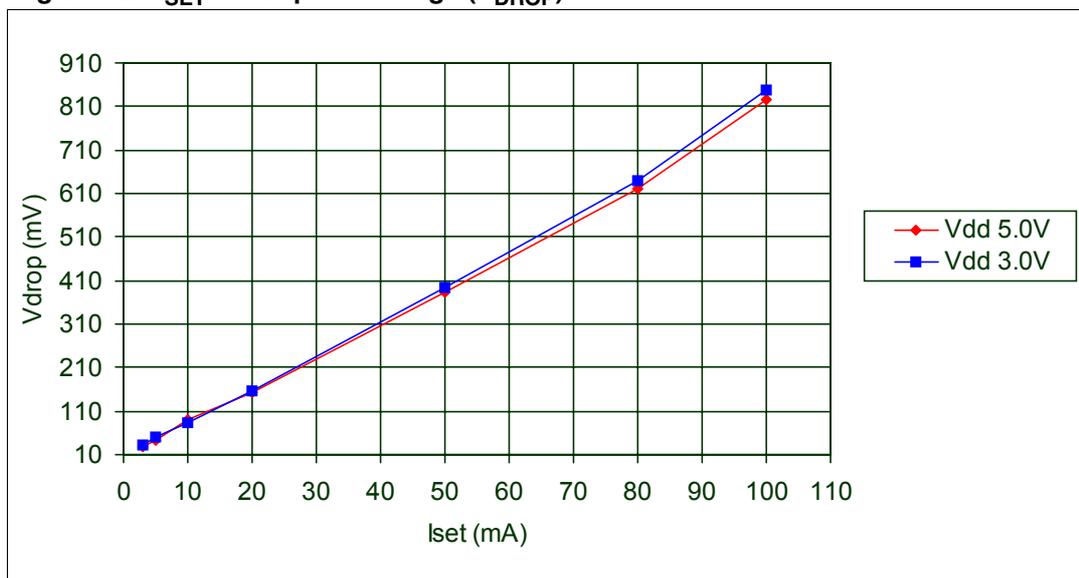


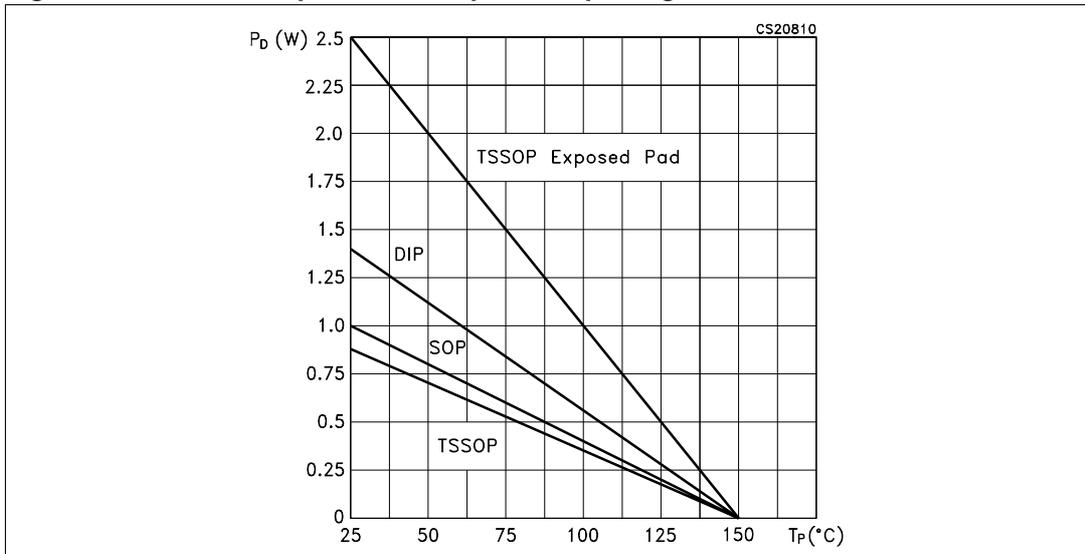
Table 10. Output current- $R_{EXT}$  resistor

Output current (mA)	3	5	10	20	50	80	100	130
$R_{ext}$ ( $\Omega$ )	6740	3930	1913	963	386	241	192	124

Figure 12.  $I_{SET}$  vs drop out voltage ( $V_{DROP}$ )Table 11.  $I_{SET}$  vs drop out voltage ( $V_{DROP}$ )

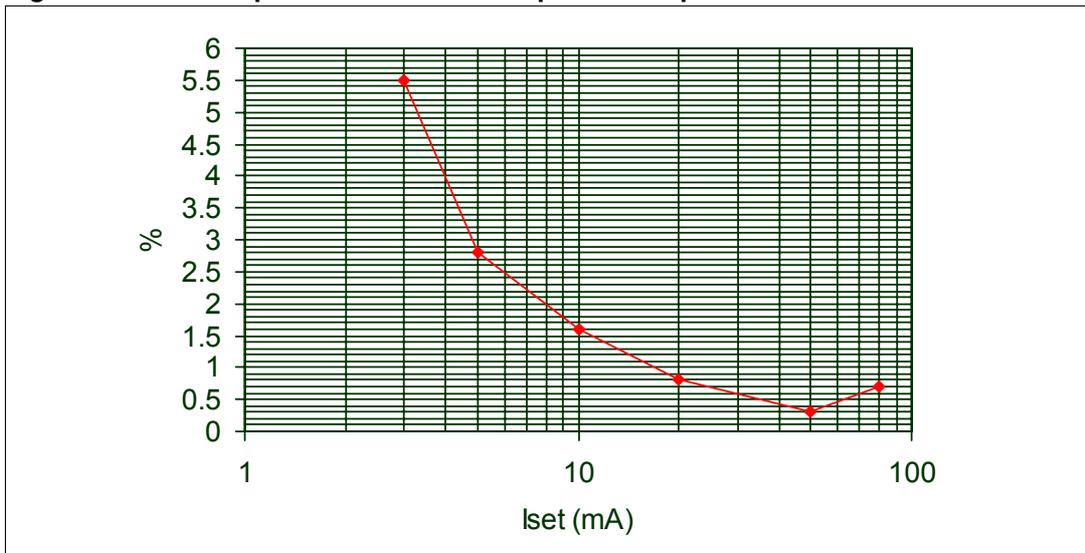
Vdd (V)	I set (mA)	Rext ( $\Omega$ )	Vdrop Min (mV)	Vdrop Max (mV)	Vdrop AVG (mV)
3	3	6470	30.6	31.2	30.93
	5	3930	46.5	52.9	48.63
	10	1910	80.9	100	82.26
	20	963	150	161	157
	50	386	392	396	394.3
	80	241	636	646	640.3
	100	192	846	850	848
5	3	6470	25.6	29	26.96
	5	3930	40.8	41.7	41.16
	10	1910	80.1	105	89.2
	20	963	153	154	154
	50	386	379	386	382
	80	241	618	626	621
	100	192	825	830	827

**Figure 13. Power dissipation vs temperature package**



*Note:* The Exposed-Pad should be soldered to the PBC to realize the thermal benefits.

**Figure 14. Current precision between outputs vs output current**



## 9 Test circuit

Figure 15. DC characteristics

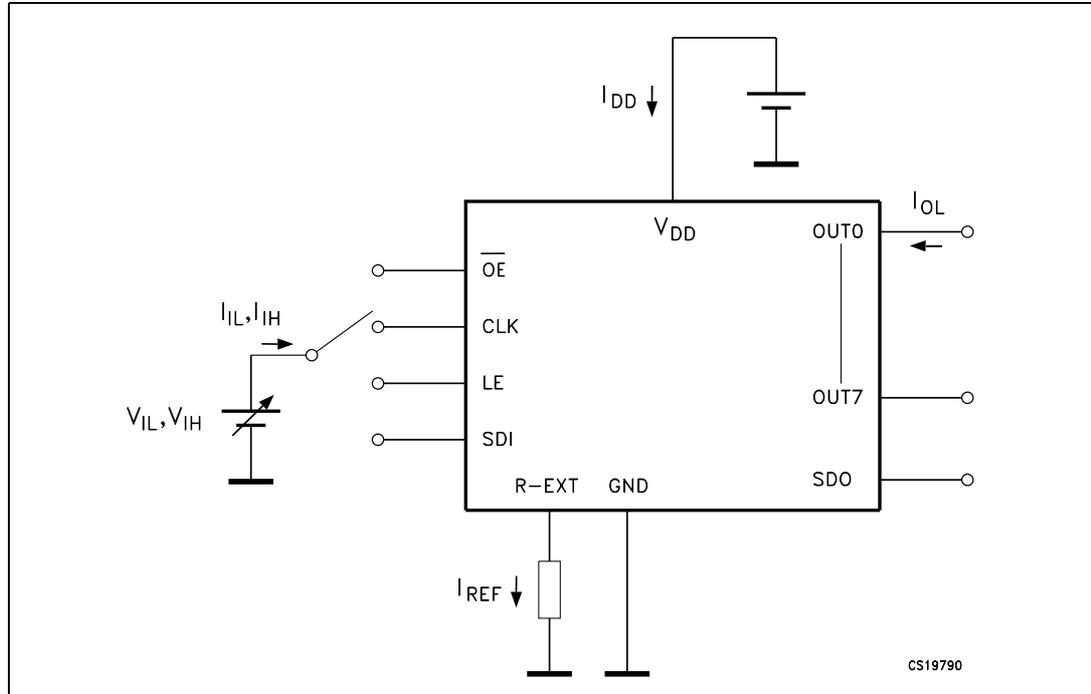


Figure 16. AC characteristics

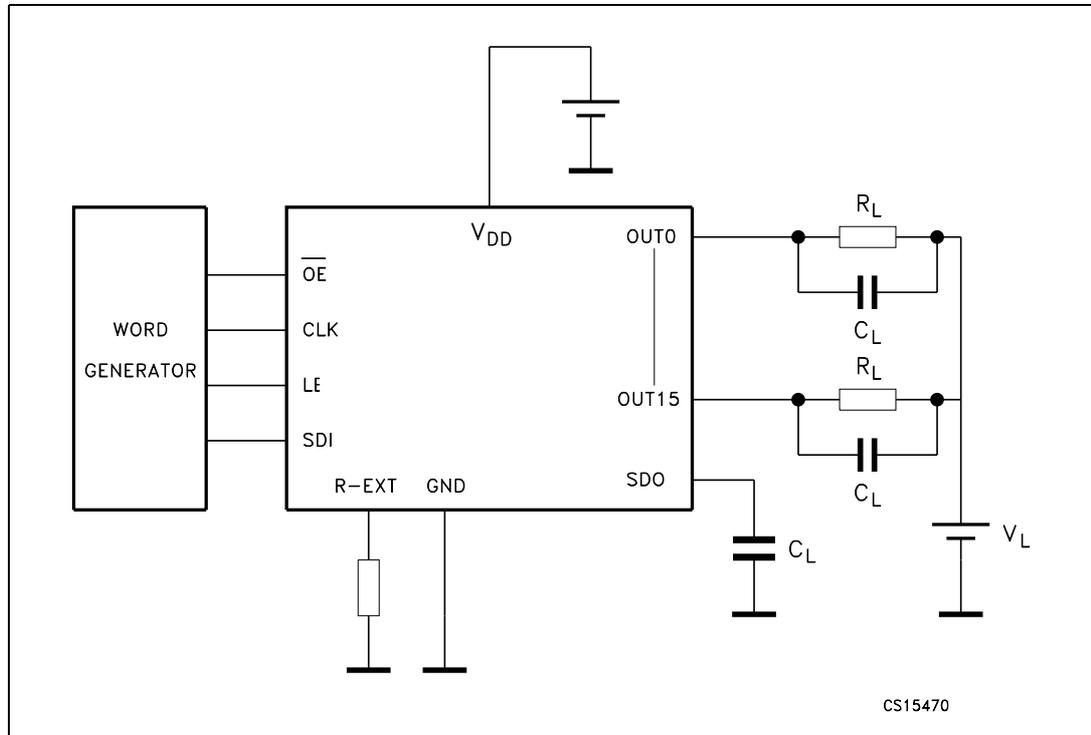
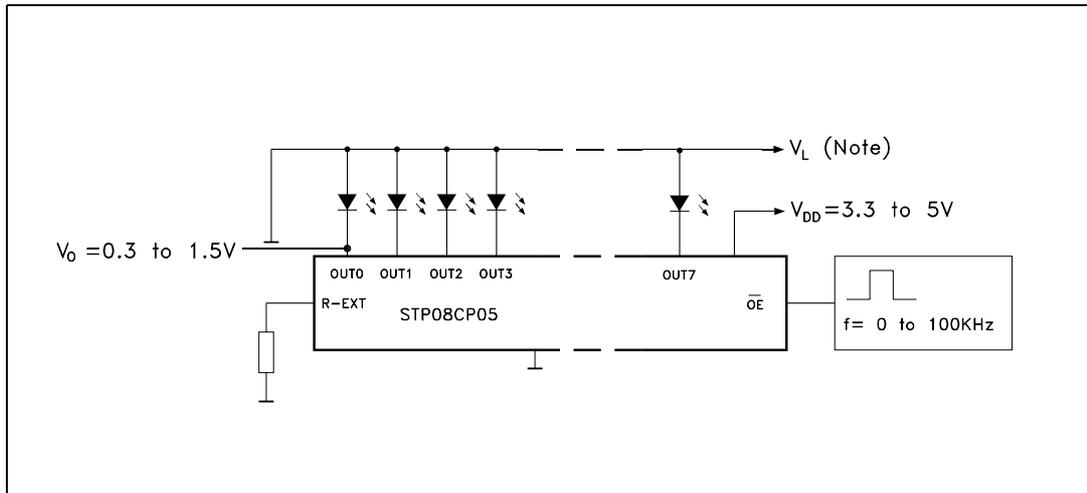


Figure 17. Typical application schematic



## 10 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK<sup>®</sup> packages. These packages have a lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

Figure 18. DIP-16 mechanical data

**Plastic DIP-16 (0.25) MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
l			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

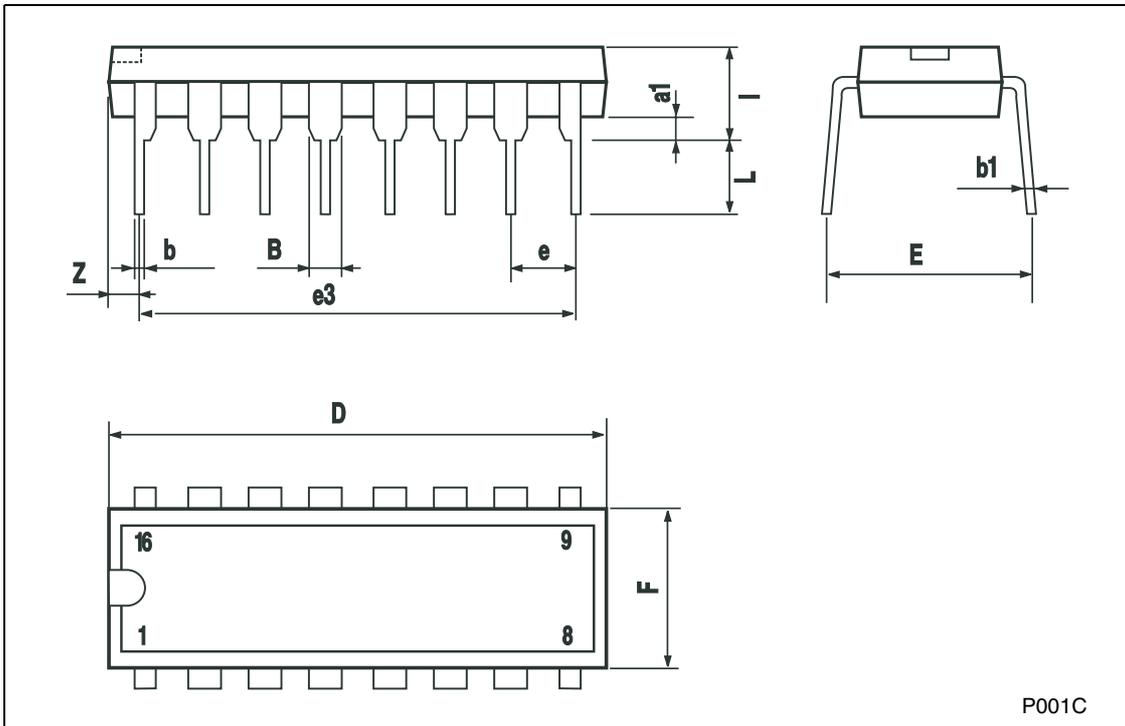


Figure 19. TSSOP16 mechanical data

TSSOP16 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

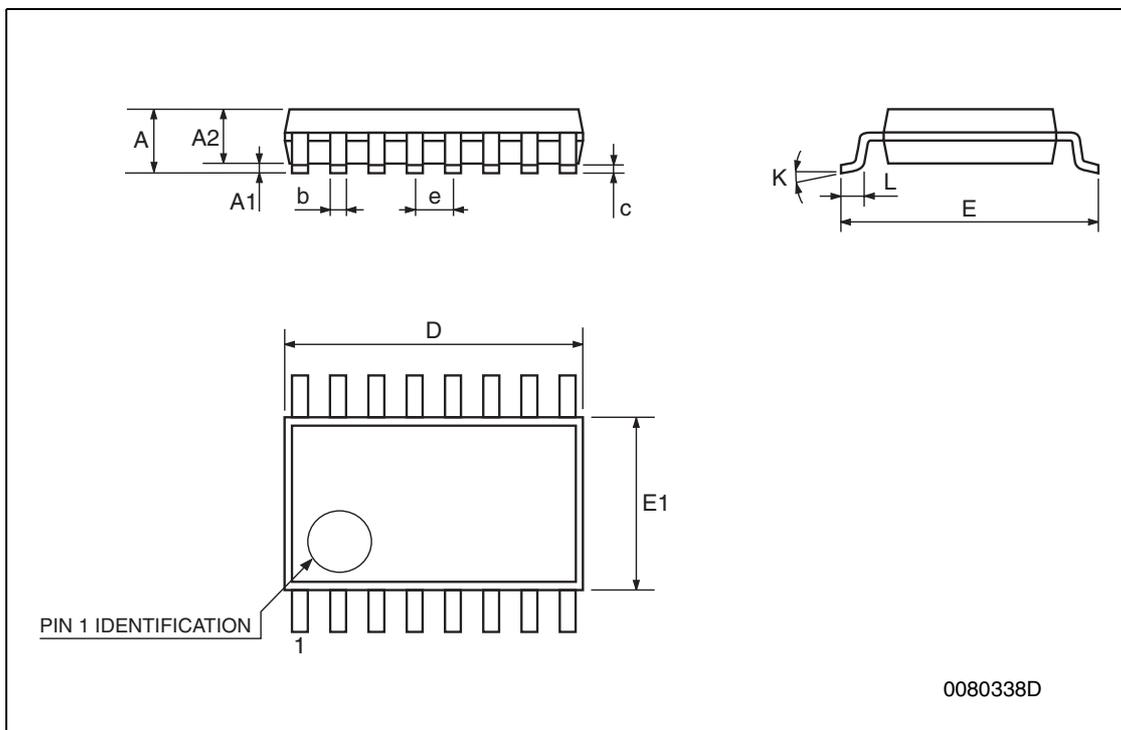


Figure 20. TSSOP16 exposed pad mechanical data

TSSOP16 EXPOSED PAD MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1			0.15		0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
D1	1.7			0.067		
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.5	0.169	0.173	0.177
E2	1.5			0.059		
e		0.65			0.0256	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

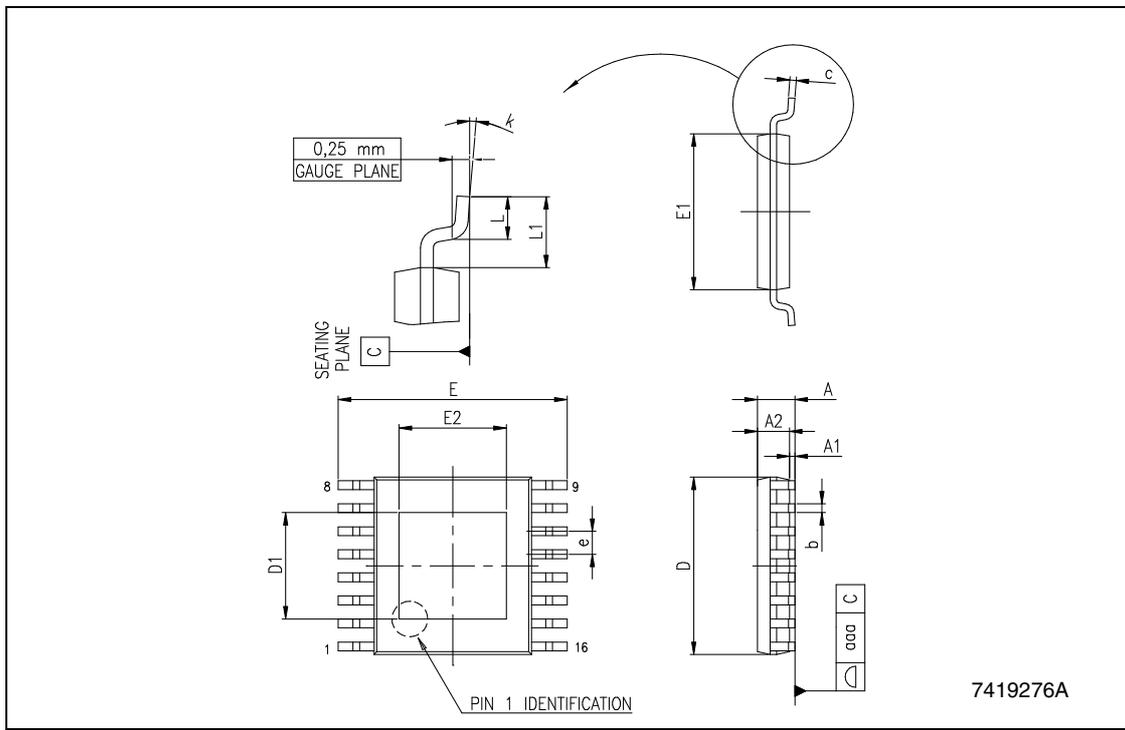


Figure 21. TSSOP16 tape and reel

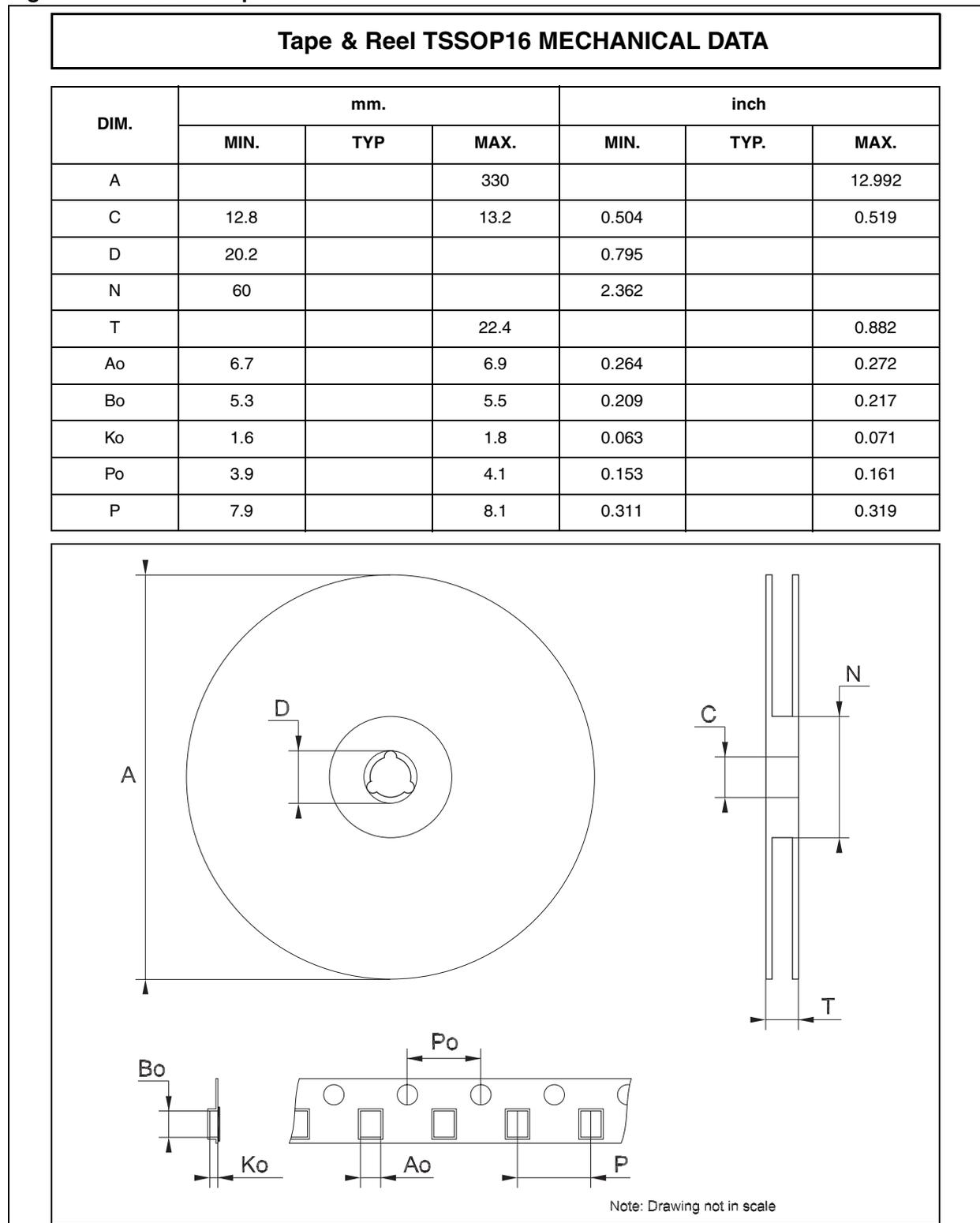
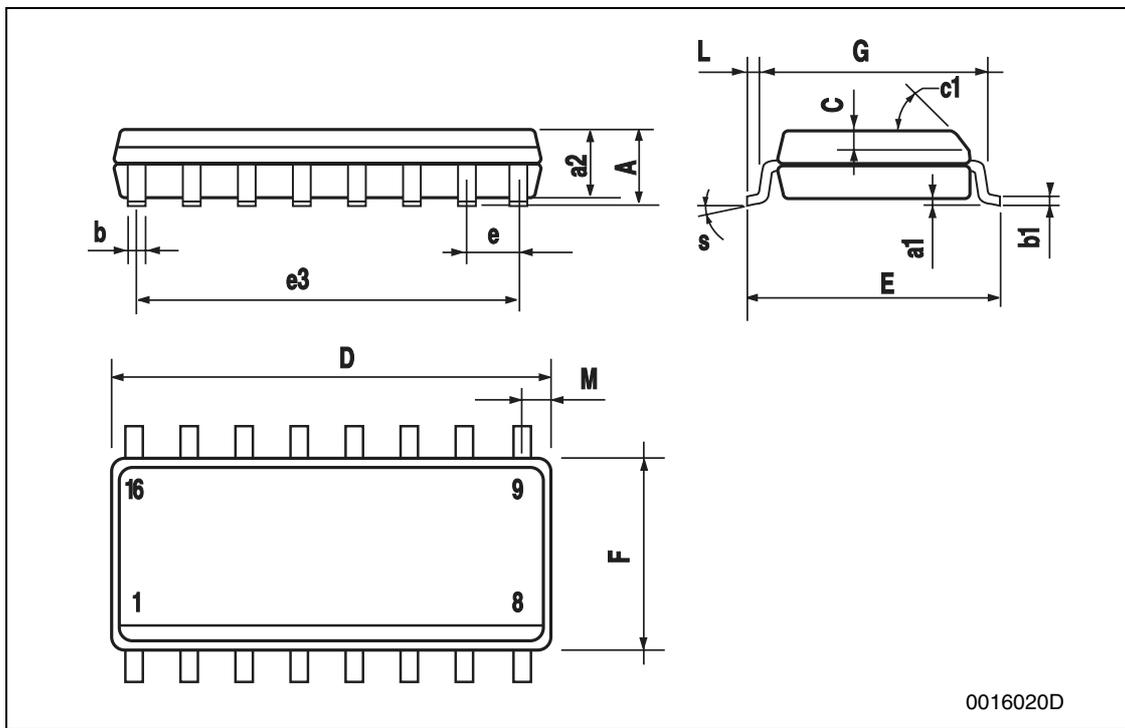


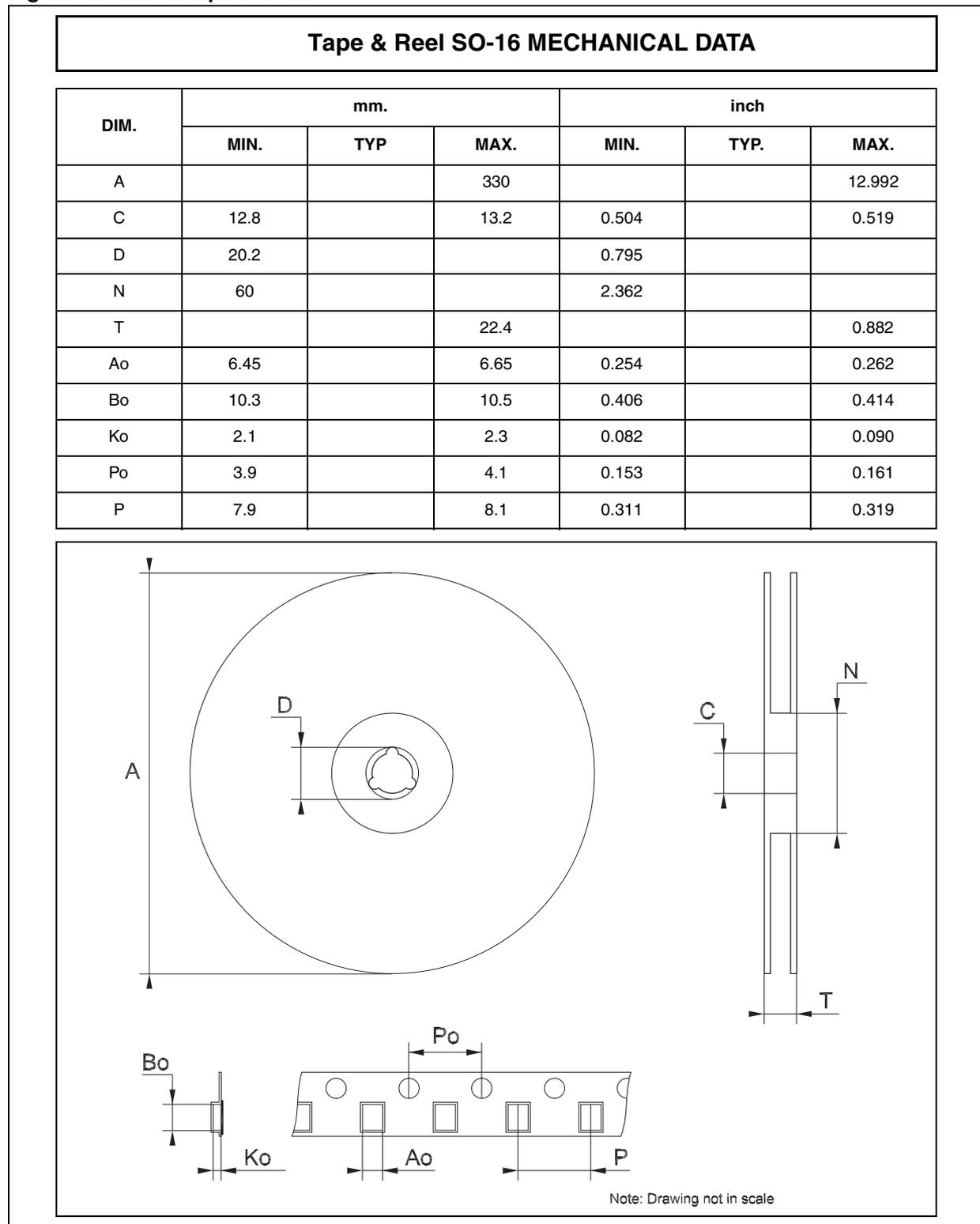
Figure 22. SO-16 mechanical data

SO-16 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.004		0.010
a2			1.64			0.063
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



0016020D

Figure 23. SO-16 tape and reel



## 11 Revision history

**Table 12. Revision history**

Date	Revision	Changes
23-May-2007	1	First release
28-Jun-2007	2	Updated <a href="#">Table 7 on page 7</a>
14-Feb-2008	3	Updated <a href="#">Table 8 on page 8</a> and added <a href="#">Figure 11</a> and <a href="#">Figure 12 on page 15</a>

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