



STP20NM65N STF20NM65N

N-channel 650 V, 0.250 Ω , 15 A TO-220, TO-220FP
second generation MDmesh™ Power MOSFET

Features

Order codes	V_{DS} @ T_{jmax}	$R_{DS(on)}$ max.	I_D
STP20NM65N	710 V	0.270 Ω	15 A
STF20NM65N			

- 100 % avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Application

- Switching applications

Description

These devices are N-channel Power MOSFETs realized using the second generation MDmesh™ technology. This revolutionary Power MOSFET associates a new vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

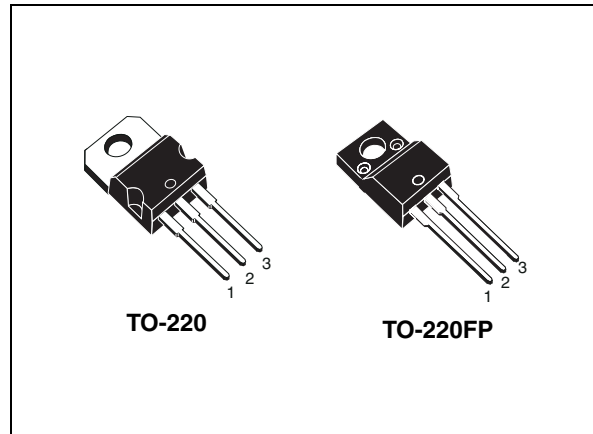


Figure 1. Internal schematic diagram

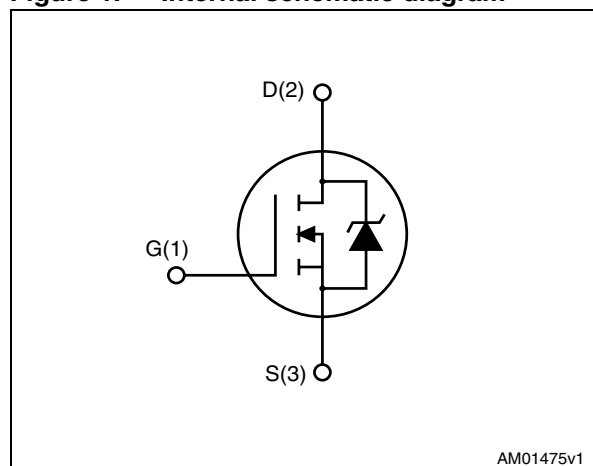


Table 1. Device summary

Order codes	Marking	Package	Packaging
STP20NM65N	20NM65N	TO-220	Tubes
STF20NM65N	20NM65N	TO-220FP	Tubes

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220	TO-220FP	
V_{DS}	Drain source voltage	650		V
V_{GS}	Gate source voltage	± 25		V
I_D	Drain current continuous $T_C = 25\text{ }^{\circ}\text{C}$	15	15 ⁽¹⁾	A
I_D	Drain current continuous $T_C = 100\text{ }^{\circ}\text{C}$	9.45		A
$I_{DM}^{(2)}$	Drain current pulsed	60		A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	125	30	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope	15		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heatsink ($t = 1\text{ s}$; $T_C = 25\text{ }^{\circ}\text{C}$)		2500	V
T_{stg} T_J	Storage temperature Max. operating junction temperature	-55 to 150 150		$^{\circ}\text{C}$

1. Limited only by maximum temperature allowed.
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 15\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS\text{ peak}} \leq V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameters	Value		Unit
		TO-220	TO-220FP	
R_{thjc}	Thermal resistance junction-case max.	1	4.17	$^{\circ}\text{C}/\text{W}$
R_{thja}	Thermal resistance junction-ambient max.	62.50		$^{\circ}\text{C}/\text{W}$
T_J	Max. lead temperature for soldering purposes	300		$^{\circ}\text{C}$

Table 4. Avalanche characteristics

Symbol	Parameters	Value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max)	4	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	115	mJ

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified).

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	650			V
I_{DSS}	Zero gate voltage drain current ($V_{GS}=0$)	$V_{DS} = \text{max rating}$ $V_{DS} = \text{max rating @ } 125\text{ °C}$			1 100	μA μA
I_{GSS}	Gate body leakage ($V_{DS}=0$)	$V_{GS} = \pm 25\text{ V}$, $V_{DS}=0$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = V_{DS}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$I_D = 7.5\text{ A}$, $V_{GS} = 10\text{ V}$		0.250	0.270	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	1280	-	pF
C_{oss}	Output capacitance			110		pF
C_{rss}	Reverse capacitance			10		pF
$C_{oss\text{ eq}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0$ to $V_{GS} = 0$	-	260	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	4.8	-	Ω
Q_g	Total gate charge	$V_{DD} = 520\text{ V}$, $I_D = 15\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 16)	-	44	-	nC
Q_{gs}	Gate source charge			8		nC
Q_{gd}	Gate-drain charge			22		nC

1. $C_{oss\text{ eq}}$: defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80 % V_{DSS} .

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 325\text{ V}$, $I_D = 7.5\text{ A}$ $R_g = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 15)	-	15	-	ns
t_r	Rise time			13.5		ns
$t_{d(off)}$	Turn-off-delay time	(see Figure 15)	-	75	-	ns
t_f	Fall time			21		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}^{(1)}$	Source drain current Source drain current (pulsed)		-		15 60	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 15\text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 15\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 17)	-	455		ns
Q_{rr}	Reverse recovery charge			5.5		nC
I_{RRM}	Reverse recovery current			24.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 15\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 17)	-	710		ns
Q_{rr}	Reverse recovery charge			8		nC
I_{RRM}	Reverse recovery current			24		A

1. Pulse width limited by safe operating area.

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5 %.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220

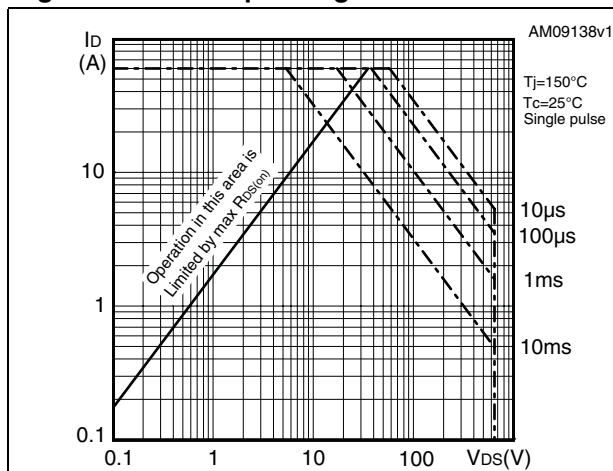


Figure 3. Thermal impedance for TO-220

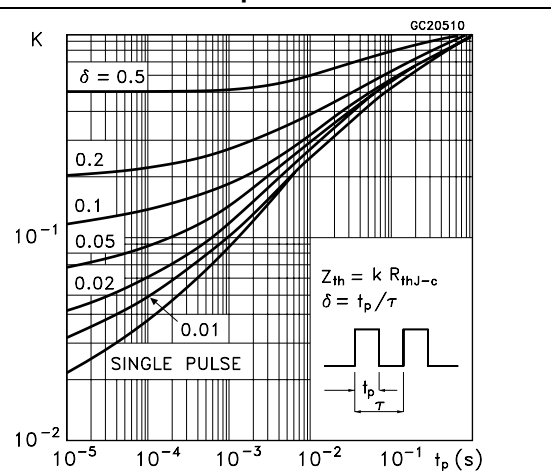


Figure 4. Safe operating area for TO-220FP

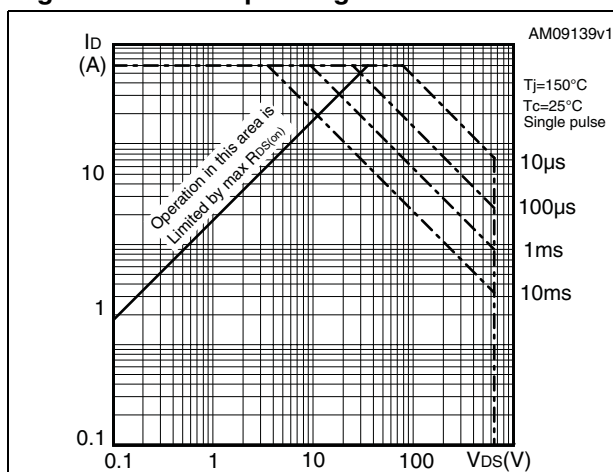


Figure 5. Thermal impedance for TO-220FP

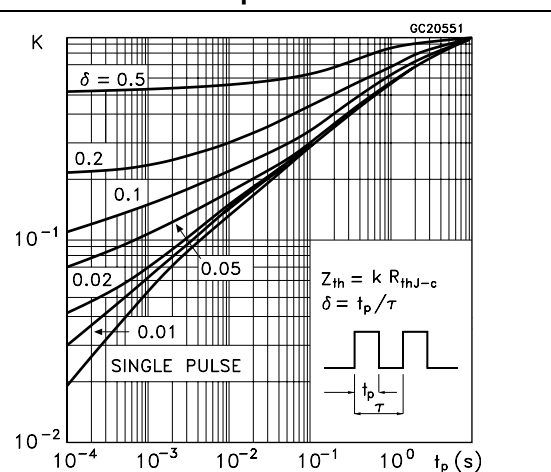


Figure 6. Output characteristics

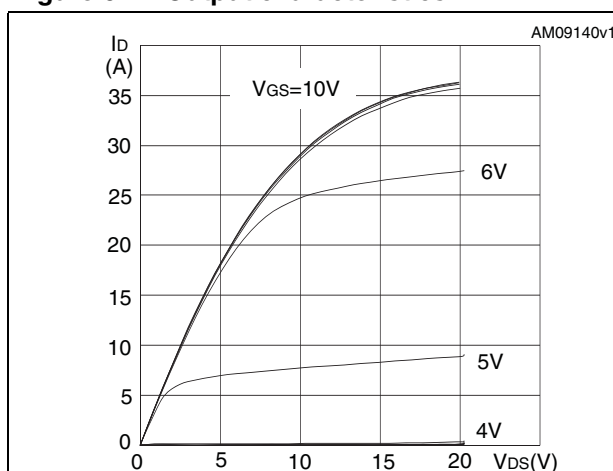


Figure 7. Transfer characteristics

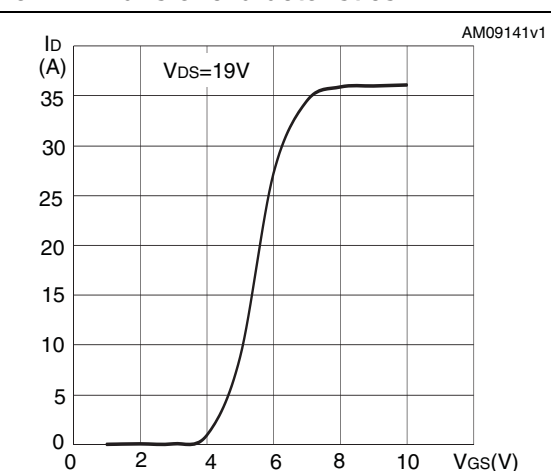


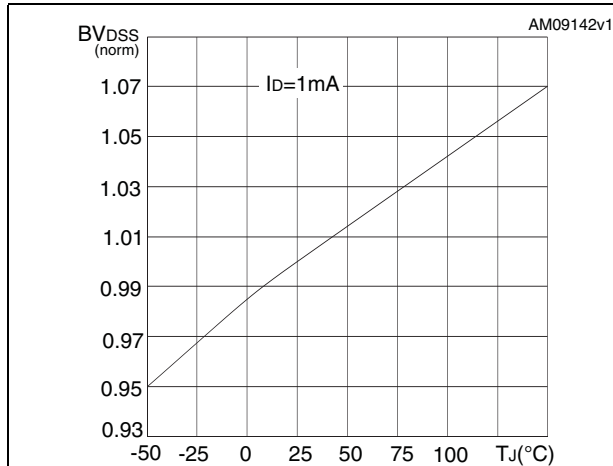
Figure 8. Normalized $B_{V_{DS}}$ vs temperature

Figure 9. Static drain-source on resistance

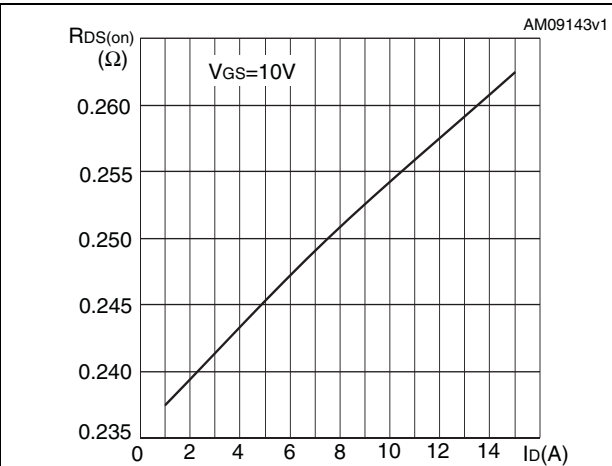


Figure 10. Gate charge vs gate-source voltage

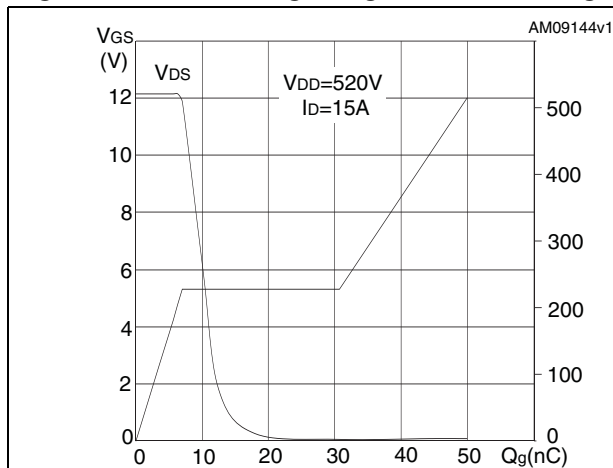


Figure 11. Capacitance variations

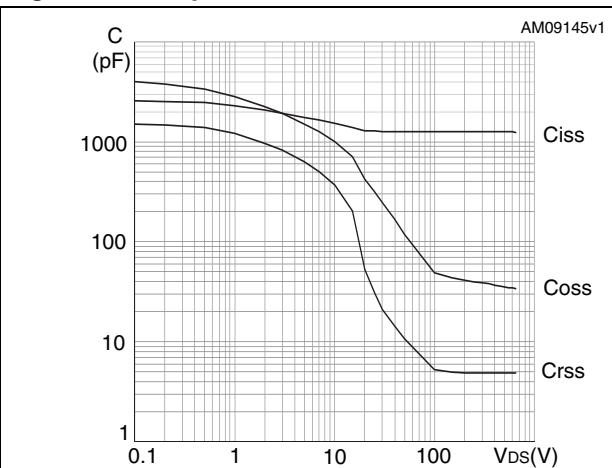


Figure 12. Normalized gate threshold voltage vs temperature

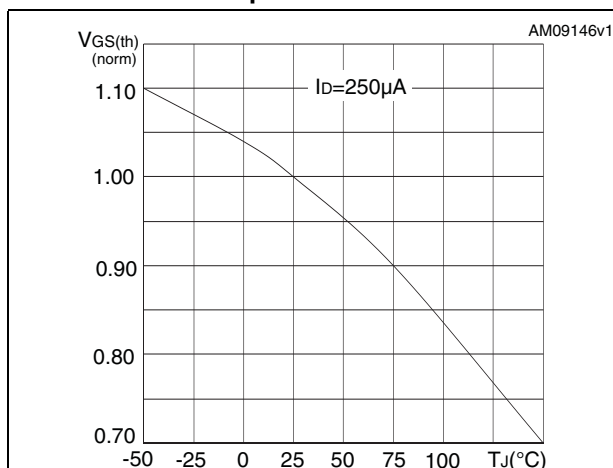


Figure 13. Normalized on resistance vs temperature

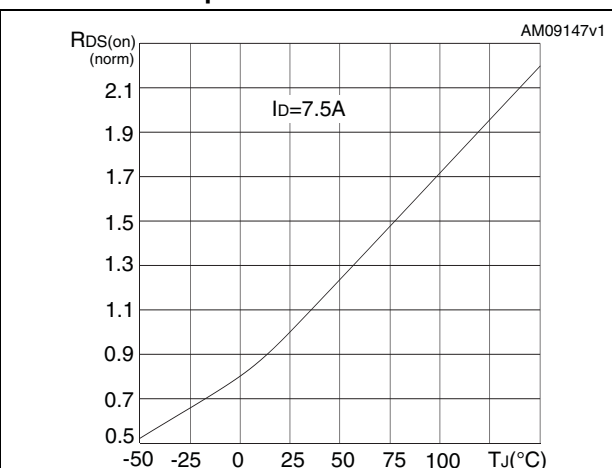
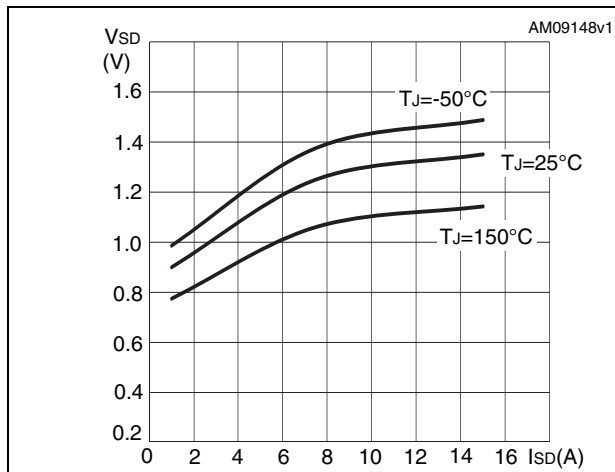


Figure 14. Source-drain diode forward characteristics

3 Test circuits

Figure 15. Switching times test circuit for resistive load

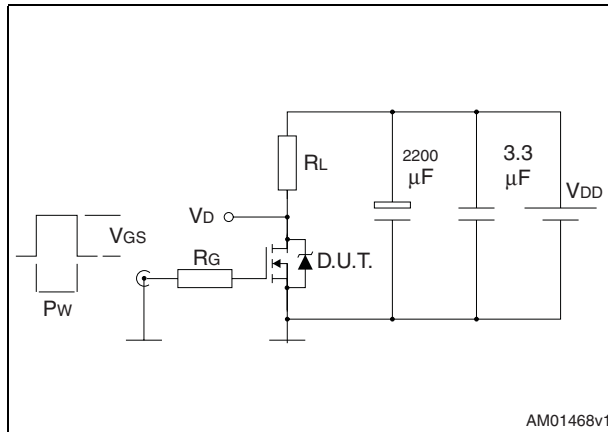


Figure 16. Gate charge test circuit

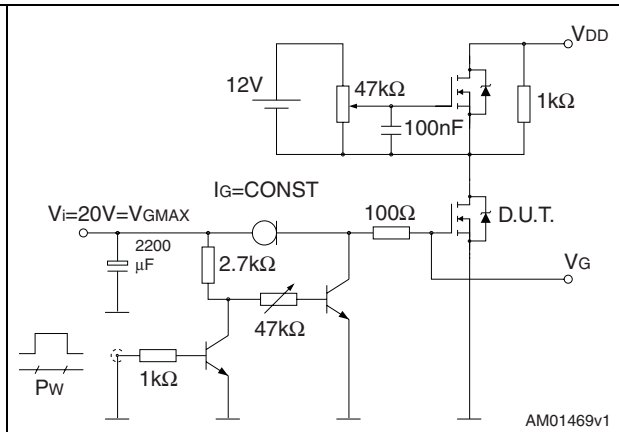


Figure 17. Test circuit for inductive load switching and diode recovery times

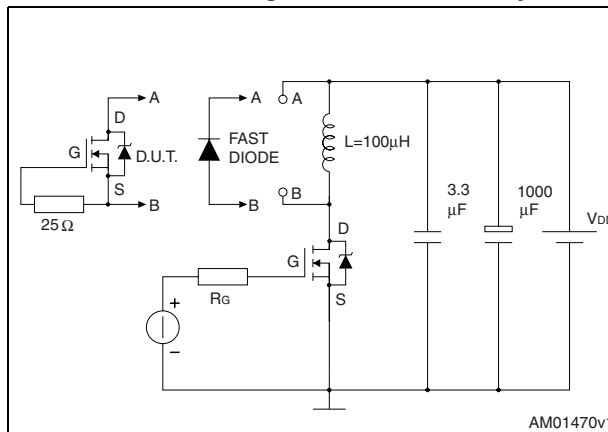


Figure 18. Unclamped inductive load test circuit

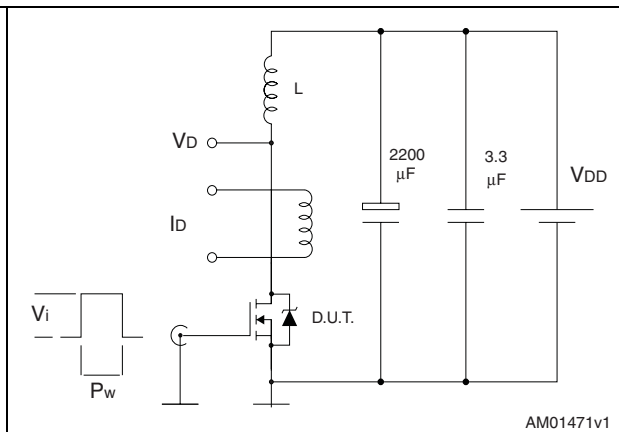


Figure 19. Unclamped inductive waveform

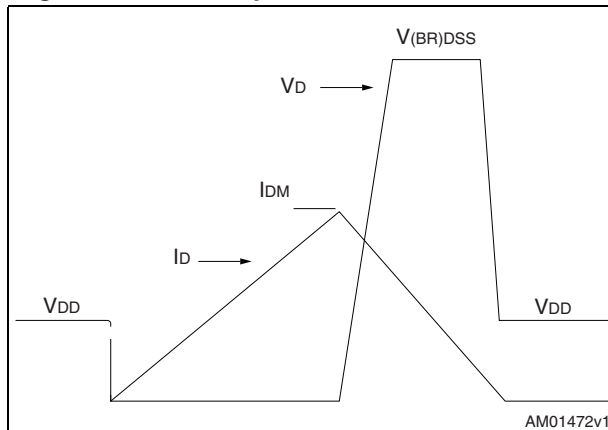
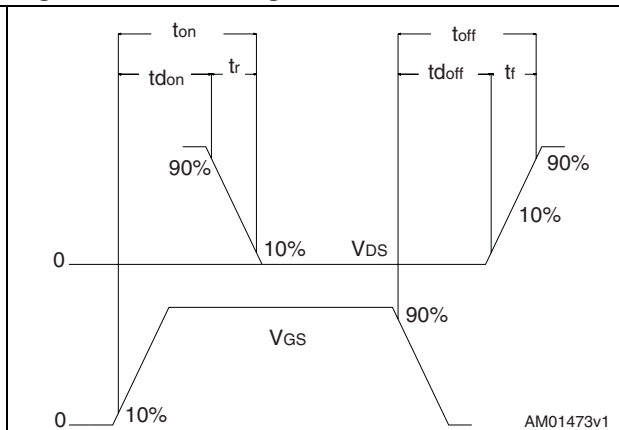


Figure 20. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 21. TO-220 type A drawing

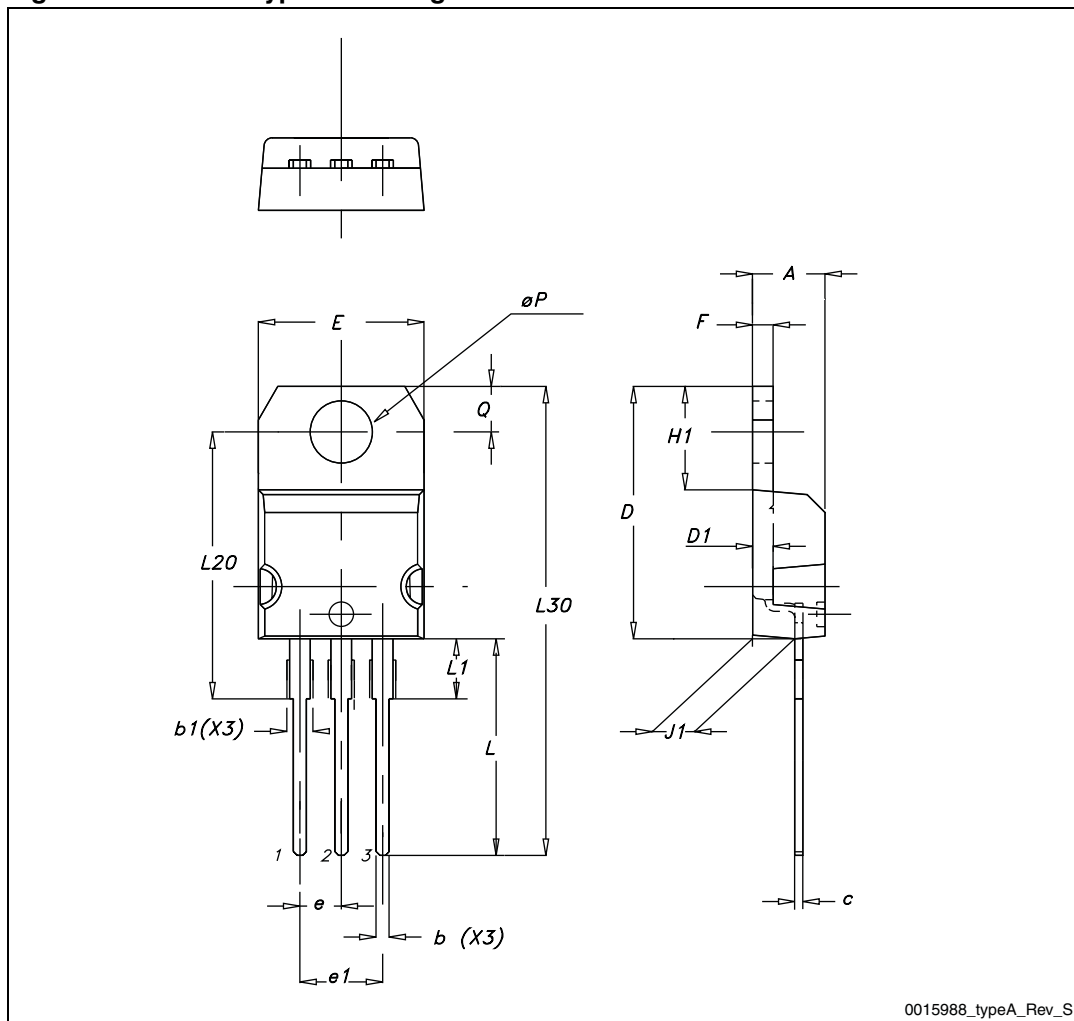
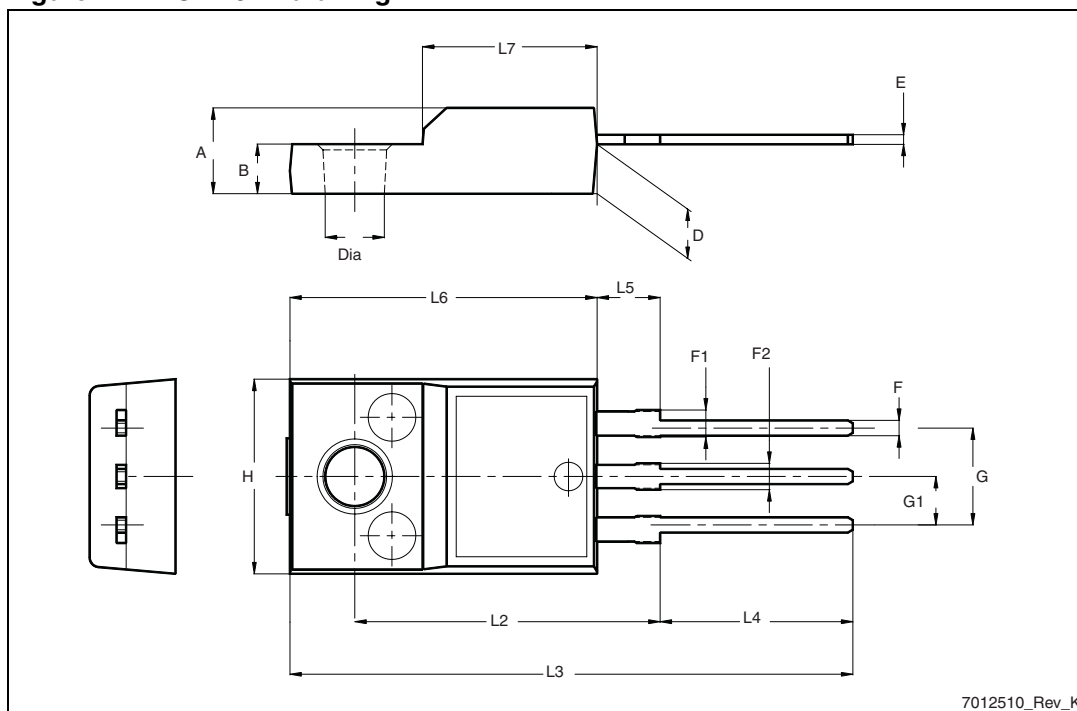


Table 10. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 22. TO-220FP drawing



5 Revision history

Table 11. Revision history

Date	Revision	Changes
12-Sep-2007	1	Initial release.
23-May-2011	2	Updated Chapter 4: Package mechanical data .

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