

P-channel 20 V, 0.075 Ω typ., 1.4 A STripFET™ VII DeepGATE™ Power MOSFET in a SOT-23 package

Datasheet – target specification

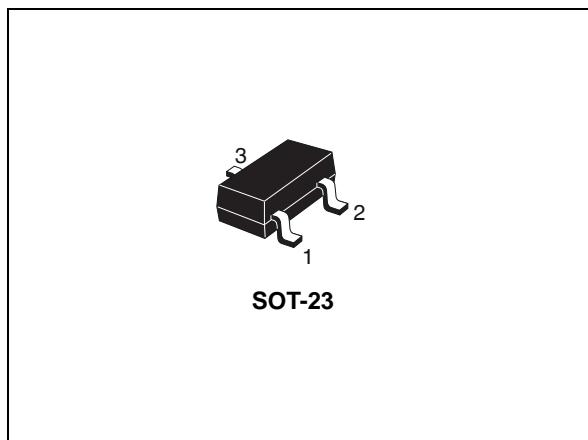


Figure 1. Internal schematic diagram

Features

Order code	V_{DS}	$R_{DS(on)} \text{ max}$	I_D
STR1P2UH7	20 V	0.1 Ω @ 4.5 V	1.4 A

- Ultra logic level
- Extremely low on-resistance $R_{DS(on)}$

Applications

- Switching applications

Description

This device exhibits low on-state resistance and capacitance for improved conduction and switching performance.

Table 1. Device summary

Order code	Marking	Package	Packaging
STR1P2UH7	1L2U	SOT23	Tape and reel

Note: For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	20	V
V_{GS}	Gate-source voltage	± 8	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	1.4	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	0.9	A
$I_{DM}^{(1)(2)}$	Drain current (pulsed)	5.6	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25^\circ\text{C}$	0.35	W
T_{stg}	Storage temperature	- 55 to 150	$^\circ\text{C}$
T_j	Max. operating junction temperature	150	$^\circ\text{C}$

1. The value is rated according to $R_{thj\text{-}pcb}$
2. Pulse width limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}pcb}^{(1)}$	Thermal resistance junction-pcb max, single operation	357	$^\circ\text{C/W}$

1. When mounted on 1inch² FR-4 board, 2 oz Cu

Note: For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

2 Electrical characteristics

($T_C = 25^\circ\text{C}$ unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$I_D = 250 \mu\text{A}$, $V_{GS} = 0$	20			V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 20 \text{ V}$, $V_{GS} = 0$			1	μA
I_{GSS}	Gate-body leakage current	$V_{GS} = \pm 8 \text{ V}$, $V_{DS} = 0$			10	nA
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	0.4		1	V
$R_{DS(\text{on})}$	Static drain-source on-resistance	$V_{GS} = 4.5 \text{ V}$, $I_D = 0.7 \text{ A}$		0.075	0.1	Ω
		$V_{GS} = 2.5 \text{ V}$, $I_D = 0.7 \text{ A}$		0.1	0.135	Ω
		$V_{GS} = 1.8 \text{ V}$, $I_D = 0.7 \text{ A}$		0.15	0.2	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 15 \text{ V}$, $f = 1 \text{ MHz}$, $V_{GS} = 0$	-	530	-	pF
C_{oss}	Output capacitance		-	90	-	pF
C_{rss}	Reverse transfer capacitance		-	50	-	pF
Q_g	Total gate charge	$V_{DD} = 15 \text{ V}$, $I_D = 1.4 \text{ A}$, $V_{GS} = 4.5 \text{ V}$ (see Figure 3)	-	5.5	-	nC
Q_{gs}	Gate-source charge		-	1	-	nC
Q_{gd}	Gate-drain charge		-	1.5	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(\text{on})}$	Turn-on delay time	$V_{DD} = 15 \text{ V}$, $I_D = 1.4 \text{ A}$, $R_G = 1 \Omega$, $V_{GS} = 4.5 \text{ V}$ (see Figure 4)	-	5	-	ns
t_r	Rise time		-	13	-	ns
$t_{d(\text{off})}$	Turn-off delay time		-	13	-	ns
t_f	Fall time		-	20	-	ns

Note: For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	-	1.4	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-	-	5.6	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 1 \text{ A}, V_{GS} = 0$	-	-	1	V
t_{rr}	Reverse recovery time	$V_{DD} = 16 \text{ V}$ $di/dt = 100 \text{ A}/\mu\text{s}, I_{SD} = 1 \text{ A}$ $T_j=150 \text{ }^\circ\text{C}$ (see Figure 4)	-	15		ns
Q_{rr}	Reverse recovery charge		-	5		nC
I_{RRM}	Reverse recovery current		-	0.7		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Note: For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

3 Test circuits

Figure 2. Switching times test circuit for resistive load

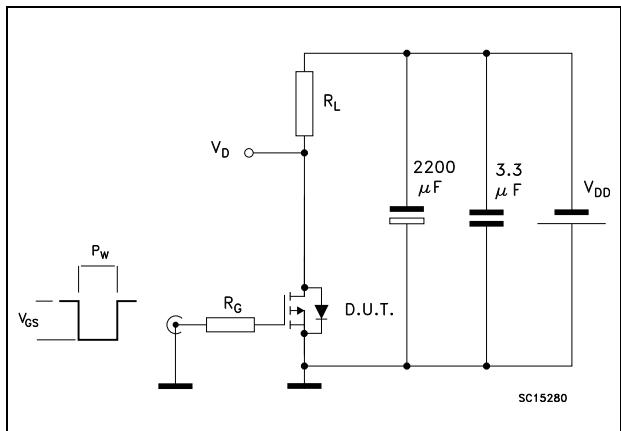


Figure 3. Gate charge test circuit

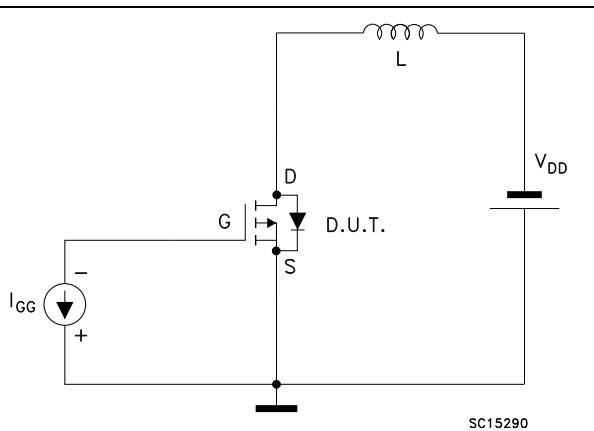
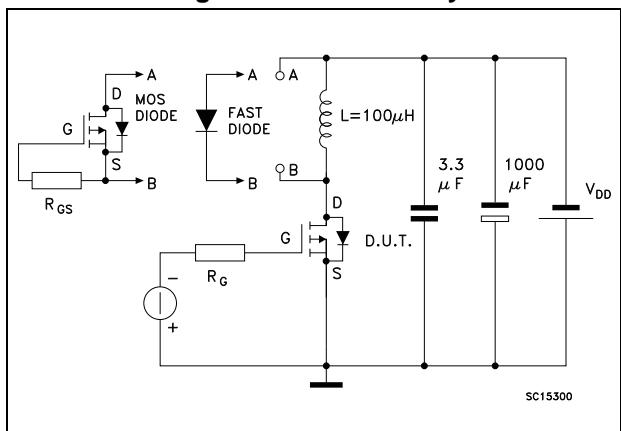


Figure 4. Test circuit for inductive load switching and diode recovery times



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.
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Table 8. SOT-23 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.89		1.40
A1	0		0.10
B	0.30		0.51
C	0.085		0.18
D	2.75		3.04
e	0.85		1.05
e1	1.70		2.10
E	1.20		1.75
H	2.10		3.00
L		0.60	
S	0.35		0.65
L1	0.25		0.55
a	0°		8°

Figure 5. SOT-23 mechanical drawing

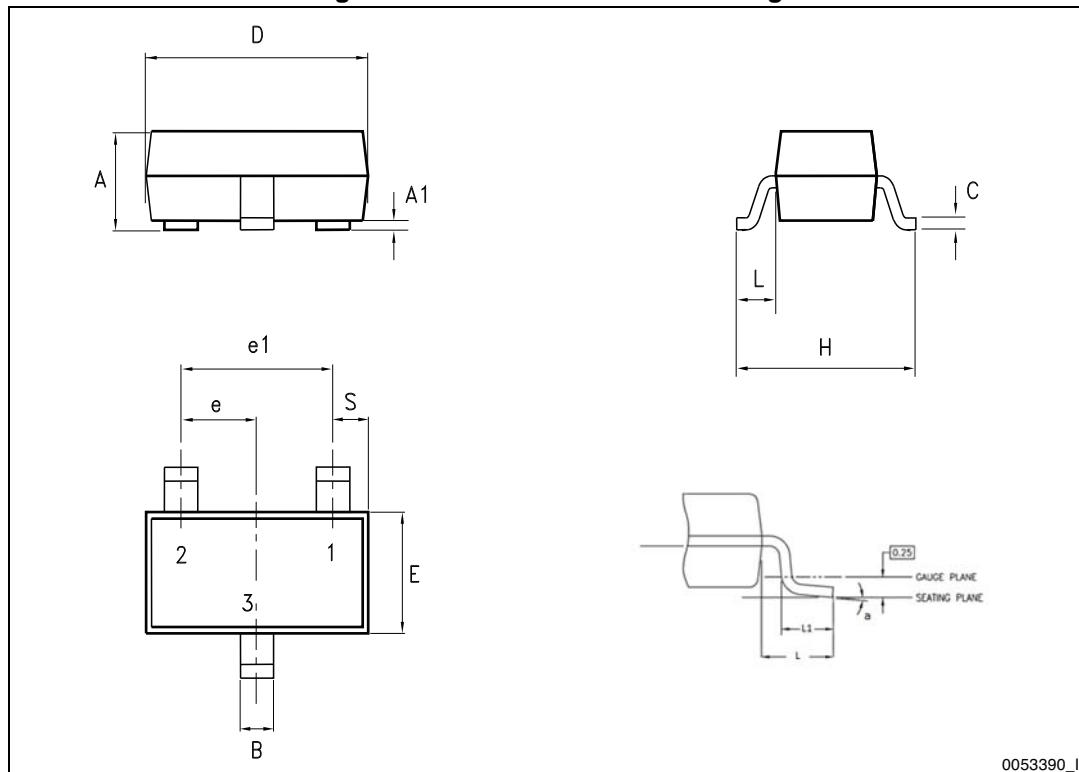
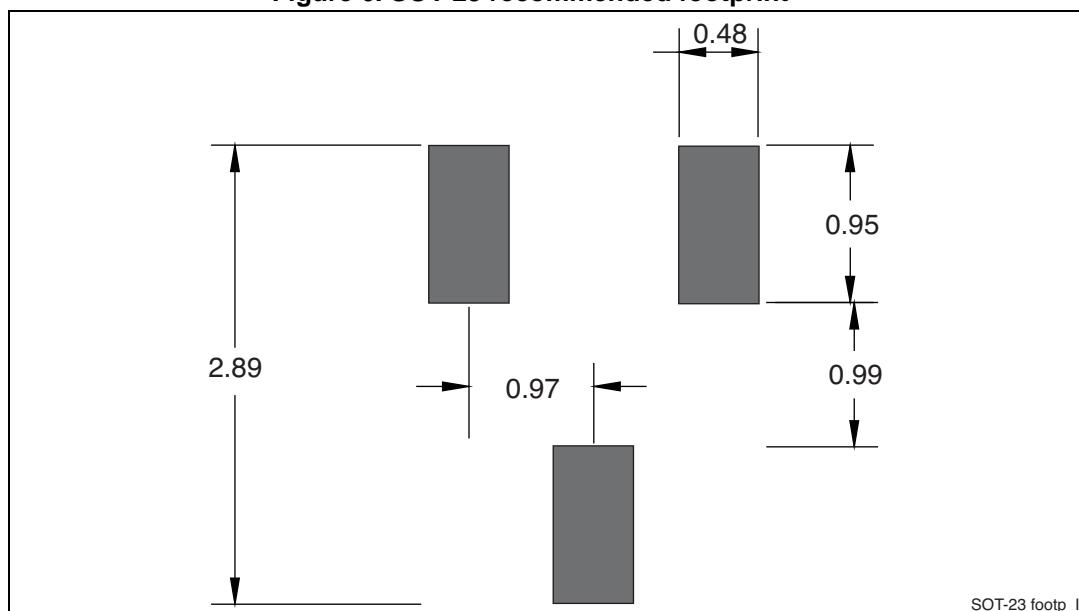


Figure 6. SOT-23 recommended footprint (a)



a. Dimensions are in mm.

5 Revision history

Table 9. Document revision history

Date	Revision	Changes
22-Jul-2013	1	First release.

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