STR4A100 Series

Application Note

General Descriptions

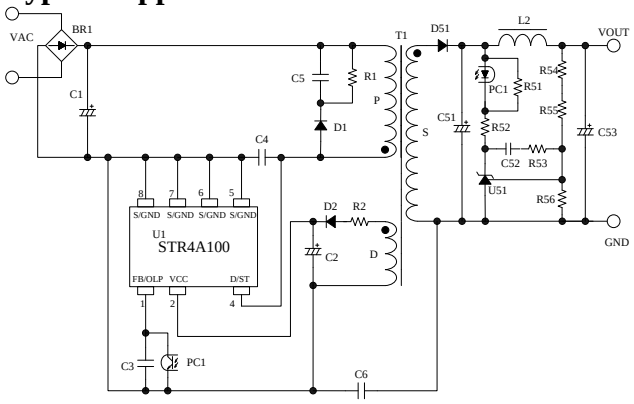
The STR4A100 series are power ICs for switching power supplies, incorporating a sense MOSFET and a current mode PWM controller IC.

The low standby power is accomplished by the automatic switching between the PWM operation in normal operation and the burst-oscillation under light load conditions. The product achieves high cost-performance power supply systems with few external components.

Features

- Auto Standby Function
  No Load Power Consumption < 10mW
- Operation Mode
  - Normal Operation ---------- PWM Mode
  - Standby ---------- Burst Oscillation Mode
- Current Mode Type PWM Control
- Random Switching Function
- Slope Compensation Function
- Leading Edge Blanking Function
- Build-in Startup Circuit
- Bias Assist Function
- Soft Start Function
- Protections
  Overcurrent Protection (OCP) --------- Pulse-by-Pulse
  Overload Protection (OLP) ---------- Auto-Restart
  Overvoltage Protection (OVP) ---------- Auto-Restart
  Thermal Shutdown Protection (TSD) ---- Auto-Restart

Typical Application Circuit



Package

DIP8

SOIC8

Not to Scale

Lineup

- Electrical Characteristics
  $V_{D/ST}$(max.) = 730 V
  Packages : D:DIP8, S:SOIC8

Products	$f_{OSC(AVG)}$	$R_{DS(ON)}$ (max.)	$I_{DLIM(H)}$
STR4A162D	65kHz	24.6 Ω	0.365 A
STR4A162S			
STR4A164HD	100kHz	12.9 Ω	0.485 A

- Output Power, P_{OUT}*

Products	Adapter		Open frame	
	AC230V	AC85 ~265V	AC230V	AC85 ~265V
STR4A162D	5.5 W	4.5 W	7.5 W	6 W
STR4A162S	5 W	4 W	7 W	5.5 W
STR4A164HD	9 W	7 W	13 W	10.5 W

* The output power is based on the thermal ratings, and the peak output power can be 120 to 140 % of the value stated here. At low output voltage, small core and short ON Duty, the output power may be less than the value stated here.

Applications

- White goods
- Auxiliary power for Flat TVs
- Low power AC/DC adapter
- Battery Chargers
- Other SMPS

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1. Absolute Maximum Ratings

- Refer to the datasheet of each product for these details.
- The polarity value for current specifies a sink as "+," and a source as "−," referencing the IC.
- Unless otherwise specified T_A = 25 °C, 5 pin = 6 pin = 7 pin = 8 pin

Characteristic	Symbol	Test Conditions	Pins	Rating	Units	Notes
FB/OLP Pin Voltage	V_{FB}		1 – 5	−0.3 to 14	V	
FB/OLP Pin Source Current	I_{FB}		1 – 5	1.0	mA	
VCC Pin Voltage	V_{CC}		2 – 5	32	V	
D/ST Pin Voltage	$V_{D/ST}$		4 – 5	−0.3 to 730	V	
Drain Peak Current	I_{DP}	Positive: Single pulse Negative: Within 2μs of pulse width	4 – 5	−0.2 to 0.7	A	4A162D
				−0.2 to 0.66	A	4A162S
				−0.2 to 0.98	A	4A164HD
Power Dissipation (1)	P_D	(2)	–	1.49	W	4A162D
				1.34	W	4A162S
				1.55	W	4A164HD
Operating Ambient Temperature	T_{OP}		–	−40 to 125	°C	
Storage Temperature	T_{stg}		–	−40 to 125	°C	
Junction Temperature	T_j		–	150	°C	

(1) Refer to MOSFET Temperature versus Power Dissipation Curve
(2) When embedding this hybrid IC onto the printed circuit board (cupper area in a 15mm×15mm)

2. Recommended Operating Conditions

Recommended operating conditions means the operation conditions maintained normal function shown in electrical characteristics.

Characteristic	Symbol	Rating		Units	Notes
		Min.	Max.		
D/ST Pin Voltage in Operation	$V_{D/ST(OP)}$	−0.3	584	V	
VCC Pin Voltage in Operation	$V_{CC(OP)}$	11	27	V	

3. Electrical Characteristics

- Refer to the datasheet of each product for these details.
- The polarity value for current specifies a sink as "+," and a source as "−," referencing the IC.
- Unless otherwise specified, T_A = 25 °C, V_{CC} = 18 V, 5 pin = 6 pin = 7 pin = 8 pin, V_{FB} = 3 V, $V_{D/ST}$ = 10 V

Characteristic	Symbol	Test Conditions	Pins	Rating			Units	Notes
				Min.	Typ.	Max.		
Power Supply Startup Operation								
Operation Start Voltage	$V_{CC(ON)}$	V_{FB} = 0 V	2−8	13.8	15.2	16.8	V	
Operation Stop Voltage (1)	$V_{CC(OFF)}$		2−8	7.3	8.1	8.9	V	
Circuit Current in Operation	$I_{CC(ON)}$	V_{CC} = 12 V	2−8	—	—	2.5	mA	
Startup Circuit Operation Voltage	$V_{STARTUP}$	V_{FB} = 0 V V_{CC} = 13.5 V	8−3	19	29	39	V	
Startup Current	$I_{STARTUP}$	V_{FB} = 0 V V_{CC} = 13.5 V $V_{D/ST}$ = 100 V	2−8	−3.7	−2.1	−0.9	mA	
Startup Current Biasing Threshold Voltage (1)	$V_{CC(BIAS)}$	V_{FB} = 0 V	2−8	7.9	9.4	10.5	V	
PWM Operation								
Average PWM Switching Frequency	$f_{OSC(AVG)}$		8−3	58	65	72	kHz	4A162D/S
				90	100	110	kHz	4A164HD
PWM Frequency Modulation Deviation	Δf		8−3	—	5	—	kHz	4A162D/S
				—	7	—	kHz	4A164HD
Maximum ON Duty	D_{MAX}		8−3	65	74	83	%	4A162D/S
				65	73	82	%	4A164HD
Protection Function								
Leading Edge Blanking Time (2)	t_{BW}		—	—	290	—	ns	4A162D/S
				—	250	—	ns	4A164HD
Drain Current Limit Compensation ON Duty (2)	D_{DPC}		—	—	36	—	%	
Drain Current Limit (ON Duty = 0 %)	$I_{DLIM(L)}$		4−8	0.290	0.322	0.354	A	
Drain Current Limit (ON Duty ≥ 36 %)	$I_{DLIM(H)}$		4−8	0.336	0.365	0.394	A	
Maximum Feedback Current	$I_{FB(MAX)}$	V_{CC} = 12 V V_{FB} = 0 V	1−8	−120	−77	−45	µA	
Minimum Feedback Current	$I_{FB(MIN)}$	V_{FB} = 6.8 V	1−8	−28	−13	−6	µA	
FB/OLP Pin Oscillation Stop Threshold Voltage	$V_{FB(OFF)}$		1−8	0.98	1.23	1.48	V	
OLP Threshold Voltage	$V_{FB(OLP)}$		1−8	7.3	8.1	8.9	V	
OLP Operation Current	$I_{CC(OLP)}$	V_{FB} = OPEN	2−8	—	230	—	µA	
OLP Delay Time	t_{OLP}	V_{FB} = OPEN	—	58	76	94	ms	
FB/OLP Pin Clamp Voltage	$V_{FB(CLAMP)}$		1−8	10.5	12.0	13.5	V	
OVP Threshold Voltage	$V_{CC(OVP)}$		2−8	27.5	29.5	31.5	V	
Thermal Shutdown Operating Temperature (2)	$T_{j(TSD)}$		—	135	—	—	°C	
Thermal Shutdown Hysteresis (2)	$T_{j(TSDHYS)}$		—	—	70	—	°C	

(1) $V_{CC(BIAS)} > V_{CC(OFF)}$ always.
(2) Design assurance

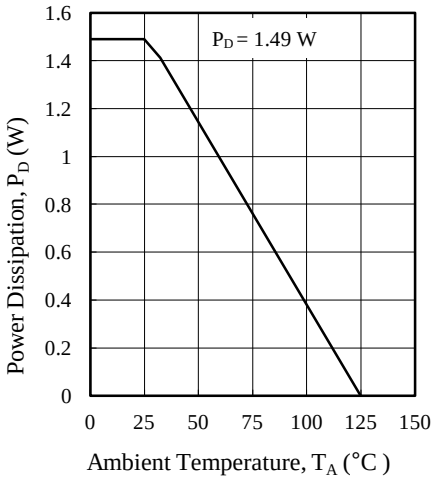
Characteristic	Symbol	Test Conditions	Pins	Ratings			Units	Notes
				Min.	Typ.	Max.		
MOSFET								
Drain Leakage Current	I_{DSS}	Ta = 125 °C V_{FB} = 0 V $V_{D/ST}$ = 584 V	4−8	—	—	50	μA	
On Resistance	$R_{DS(ON)}$	I_D = 37 mA	4−8	—	21.0	24.6	Ω	4A162D/S
		I_D = 52 mA		—	11.0	12.9	Ω	4A164HD
Switching Time	t_f		4−8	—	—	250	ns	
Thermal Characteristics								
Thermal Resistance (2)	θ_{j-F}	(3)	—	—	—	18	°C /W	4A162D
				—	—	21	°C /W	4A162S
				—	—	16	°C /W	4A164HD
	θ_{j-C}	(4)	—	—	—	15	°C /W	4A162D
				—	—	16	°C /W	4A162S
				—	—	15	°C /W	4A164HD

(2) Design assurance
(3) Frame temperature (T_F) measured at the root of the 7 pin(S/GND).
(4) Case temperature (T_C) measured at the center of the case top surface.

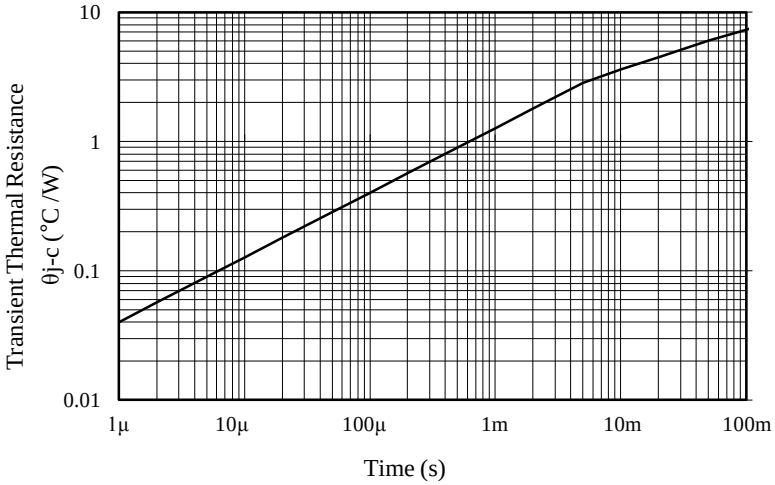
4. Performance Curves

● **STR4A162D**

Ambient Temperature versus Power Dissipation Curve

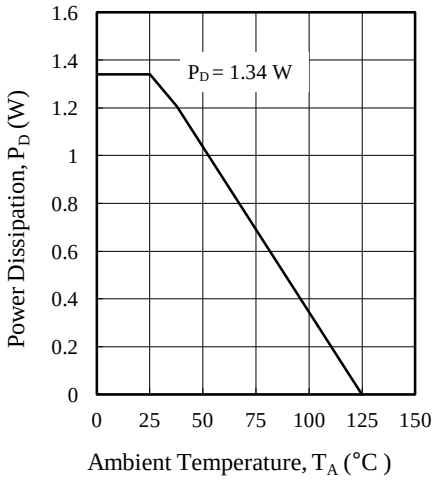


Transient Thermal Resistance Curve

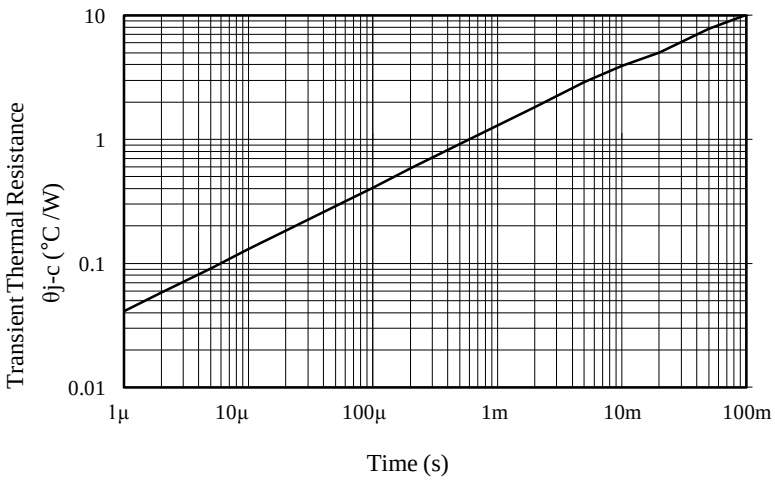


● **STR4A162S**

Ambient Temperature versus Power Dissipation Curve

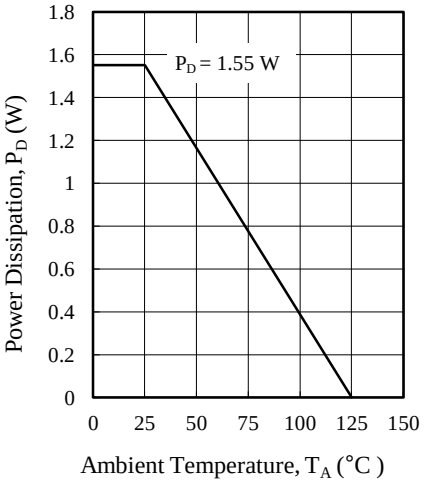


Transient Thermal Resistance Curve

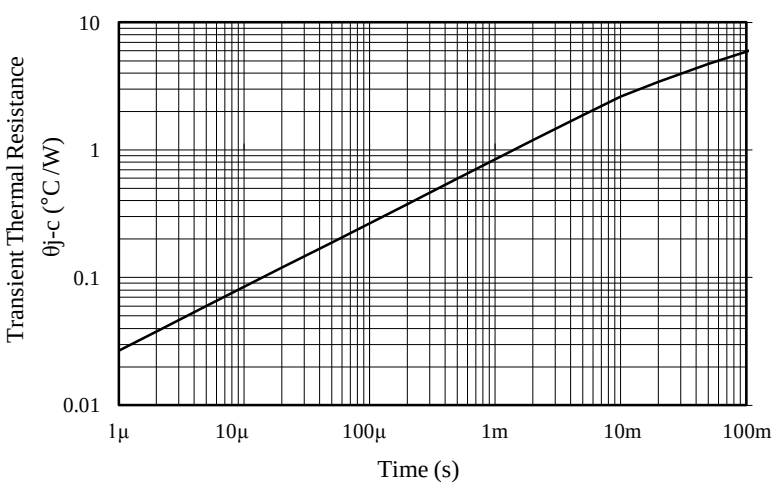


● **STR4A164HD**

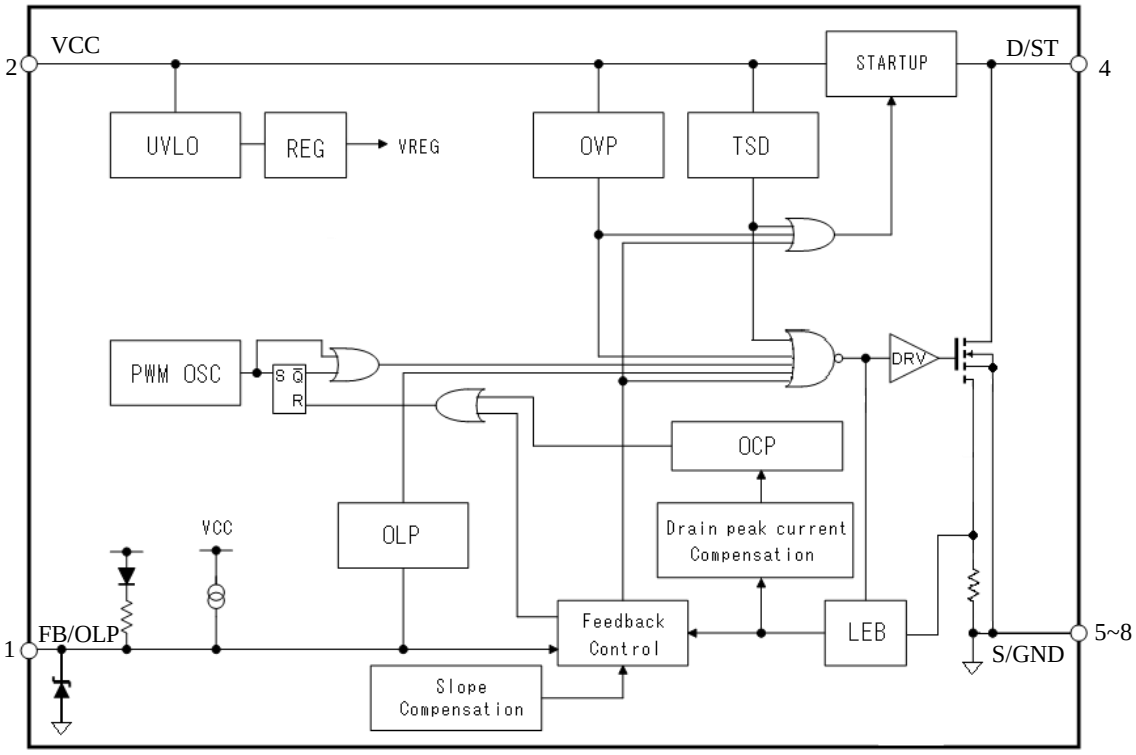
Ambient Temperature versus Power Dissipation Curve



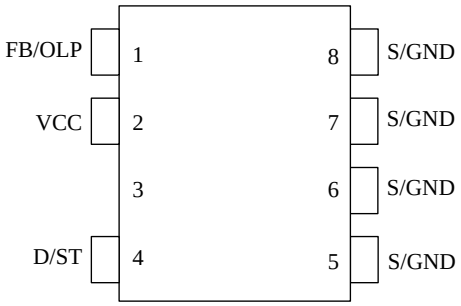
Transient Thermal Resistance Curve



5. Functional Block Diagram



6. Pin Configuration Definitions



Pin	Name	Descriptions
1	FB/OLP	Input of constant voltage control signal and input of OLP signal
2	VCC	Power supply voltage input for Control Part and input of Overvoltage Protection (OVP) signal
3	—	(Pin removed)
4	D/ST	MOSFET Drain and input of startup current
5	S/GND	MOSFET Source and ground
6		
7		
8		

7. Typical Application Circuit

- The PCB traces S/GND pins should be as wide as possible, in order to enhance thermal dissipation.
- In applications having a power supply specified such that V_{DS} has large transient surge voltages, a clamp snubber circuit of a capacitor-resistor-diode (CRD) combination should be added on the primary winding P, or a damper snubber circuit of a capacitor (C) or a resistor-capacitor (RC) combination should be added between the D/ST pin and the S/GND pin.

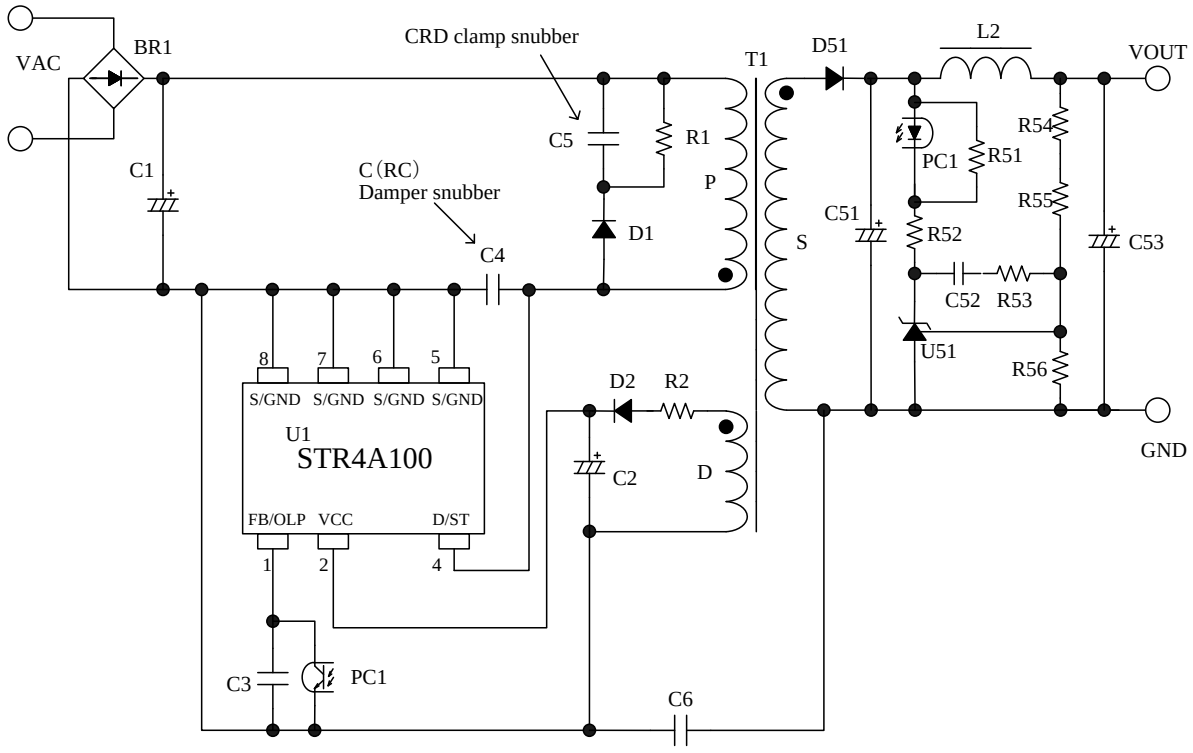
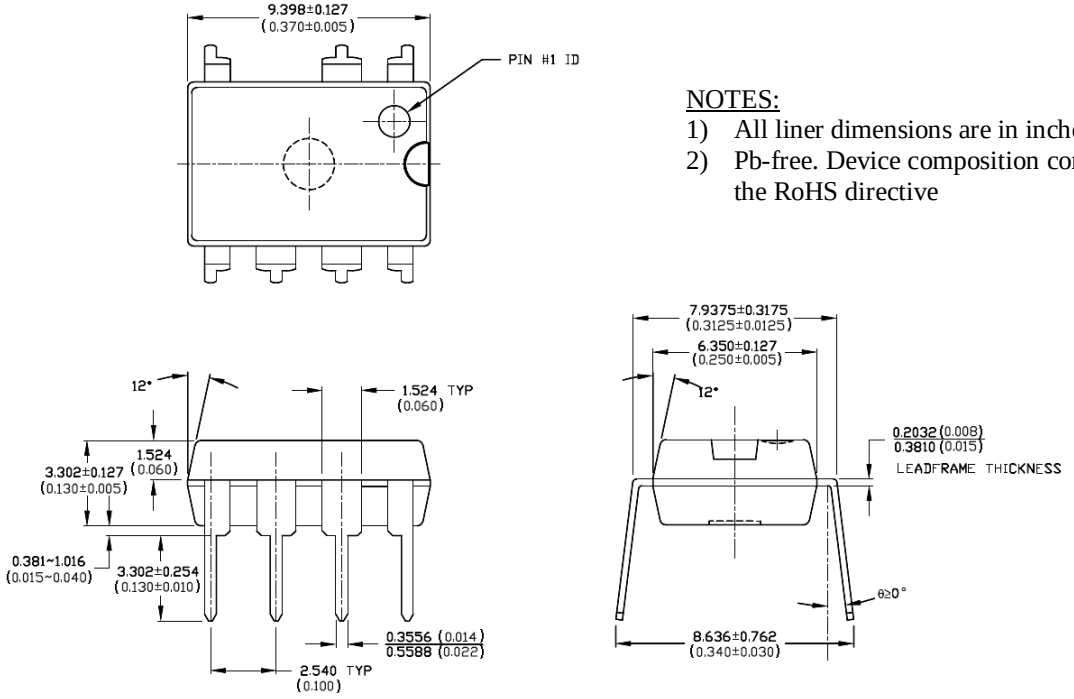


Figure 7-1 Typical application circuit

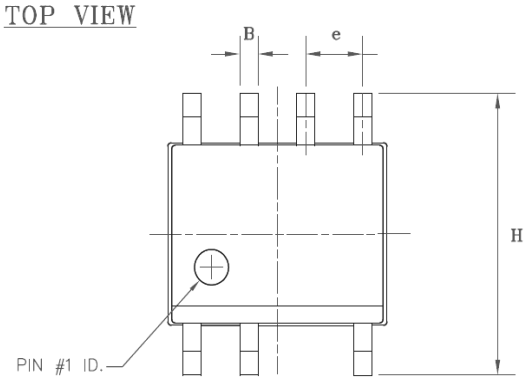
8. Package Outline

- DIP8

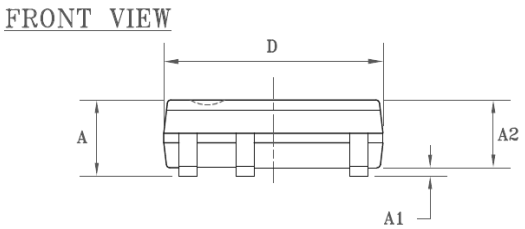


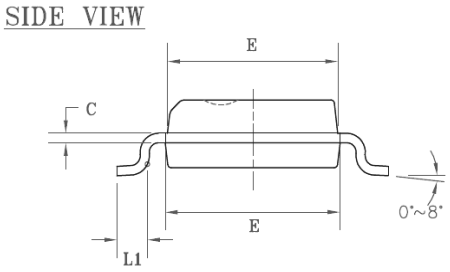
NOTES:
1) All liner dimensions are in inches
2) Pb-free. Device composition compliant with the RoHS directive

- SOIC8



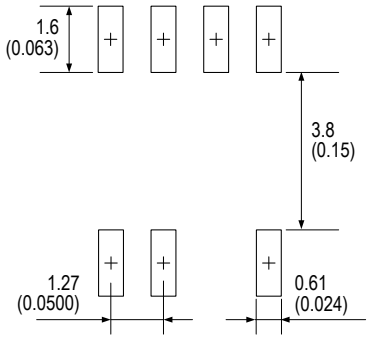
Dimension	MM		INCH	
	Min.	Max.	Min.	Max.
A	–	1.7272	–	0.068
A1	0.1270	0.2286	0.005	0.009
A2	1.3970	1.4986	0.055	0.059
B	0.3302	0.5080	0.013	0.020
C	0.1905	0.2413	0.0075	0.0095
D	4.8514	5.0038	0.191	0.197
E	3.8354	3.9878	0.151	0.157
E1	3.7338	3.8862	0.147	0.153
e	1.2700 BSC		0.05 BSC	
H	5.8928	6.1976	0.232	0.244
L1	0.5080	0.7620	0.020	0.030
θ	0	8°	0	8°





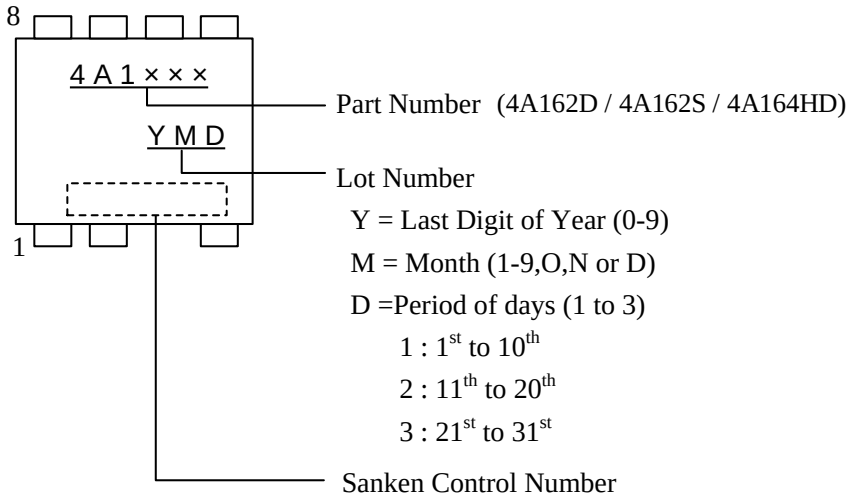
NOTES:
1) All liner dimensions are in inches
2) Pb-free. Device composition compliant with the RoHS directive

Land Pattern Example (not to scale)



Unit : mm (inch)

9. Marking Diagram



10. Operational Description

- All of the parameter values used in these descriptions are typical values, unless they are specified as minimum or maximum.
- With regard to current direction, "+" indicates sink current (toward the IC) and "–" indicates source current (from the IC).

10.1 Startup Operation

Figure 10-1 shows the circuit around VCC pin.

The IC incorporates the startup circuit. The circuit is connected to D/ST pin. When D/ST pin voltage reaches to Startup Circuit Operation Voltage $V_{STARTUP}$ = 29 V, the startup circuit starts operation.

During the startup process, the constant current, $I_{STARTUP}$ = −2.1 mA, charges C2 at VCC pin. When VCC pin voltage increases to $V_{CC(ON)}$ = 15.2 V, the control circuit starts switching operation.

During the IC operation, the voltage rectified the auxiliary winding voltage, V_D, of Figure 10-1 becomes a power source to the VCC pin.

After switching operation begins, the startup circuit turns off automatically so that its current consumption becomes zero.

The approximate value of auxiliary winding voltage is about 15 V to 20 V, taking account of the winding turns of D winding so that VCC pin voltage becomes within the specification of input and output voltage variation of power supply.

$$V_{CC(BIAS)}(\max.) < V_{CC} < V_{CC(OVP)}(\min.)$$

$$\Rightarrow 10.5(V) < V_{CC} < 27.5(V) \quad (1)$$

The startup time of IC is determined by C2 capacitor value. The approximate startup time t_{START} is calculated as follows:

$$t_{START} = C2 \times \frac{V_{CC(ON)} - V_{CC(INT)}}{|I_{STRATUP}|} \quad (2)$$

where,

t_{START} : Startup time of IC (s)

$V_{CC(INT)}$: Initial voltage on VCC pin (V)

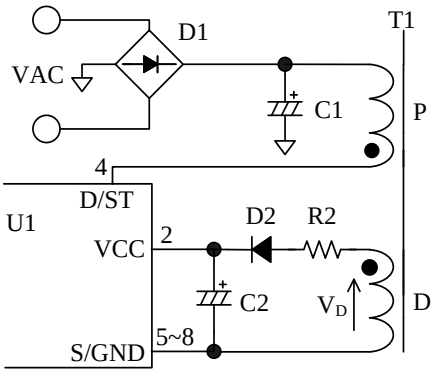


Figure 10-1 VCC pin peripheral circuit

10.2 Undervoltage Lockout (UVLO)

Figure10-2 shows the relationship of VCC pin voltage and circuit current I_{CC}. When VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.1 V, the control circuit stops operation by UVLO (Undervoltage Lockout) circuit, and reverts to the state before startup.

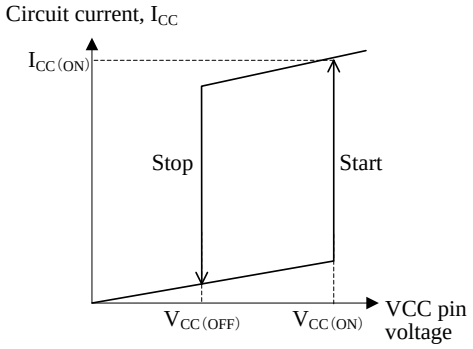


Figure10-2 Relationship between VCC pin voltage and I_{CC}

10.3 Bias Assist Function

Figure 10-3 shows VCC pin voltage behavior during the startup period.

After VCC pin voltage increases to $V_{CC(ON)}$ = 15.2 V at startup, the IC starts the operation. Then circuit current increases and VCC pin voltage decreases. At the same time, the auxiliary winding voltage V_D increases in proportion to output voltage. These are all balanced to produce VCC pin voltage.

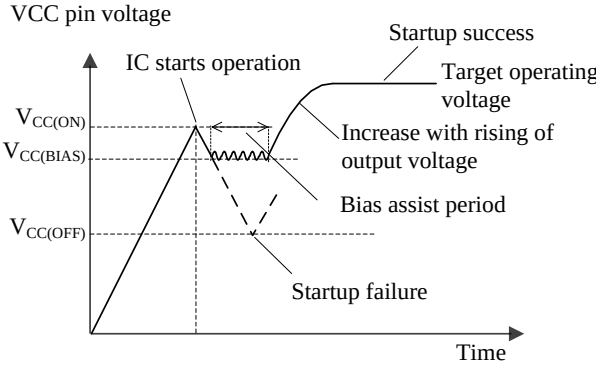


Figure 10-3 VCC pin voltage during startup period

The surge voltage is induced at output winding at turning off a power MOSFET. When the output load is light at startup, the surge voltage causes the unexpected feedback control. This results the lowering of the output power and VCC pin voltage. When the VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.1V, the IC stops switching operation and a startup failure occurs. In order to prevent this, the Bias Assist function is activated when the VCC pin voltage decreases to the startup current threshold biasing voltage, $V_{CC(BIAS)}$= 9.4V. While the Bias Assist function is activated, any decrease of the VCC pin voltage is counteracted by providing the startup current,

$I_{STARTUP}$, from the startup circuit. Thus, the VCC pin voltage is kept almost constant.

By the Bias Assist function, the value of C2 is allowed to be small and the startup time becomes shorter. Also, because the increase of VCC pin voltage becomes faster when the output runs with excess voltage, the response time of the OVP function becomes shorter.

It is necessary to check and adjust the startup process based on actual operation in the application, so that poor starting conditions may be avoided.

10.4 Soft Start Function

Figure 10-4 shows the behavior of VCC pin voltage and drain current during the startup period.

The IC activates the soft start circuitry during the startup period. Soft start time is fixed to around 6 ms. during the soft start period, over current threshold is increased step-wisely (5 steps). This function reduces the voltage and the current stress of MOSFET and secondary side rectifier diode.

Since the Leading Edge Blanking Function (refer to Section 10.5 Constant Output Voltage Control) is deactivated during the soft start period, there is the case that ON time is less than the leading edge blanking time, t_{BW} = 290 ns.

After the soft start period, D/ST pin current, I_D, is limited by the Drain Current Limit, I_{DLIM}, until the output voltage increases to the target operating voltage. This period is given as t_{LIM}.

In case t_{LIM} is longer than the OLP Delay Time, t_{CCD} , the output power is limited by the OLP protection operation (OLP).

Thus, it is necessary to adjust the value of output capacitor and the turn ratio of auxiliary winding D so that the t_{LIM} is less than t_{OLP} = 58 ms (min.).

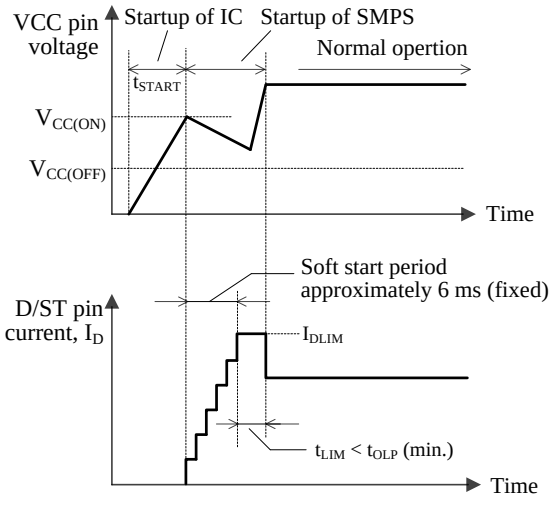


Figure 10-4 V_{CC} and I_D behavior during startup

10.5 Constant Output Voltage Control

The IC achieves the constant voltage control of the power supply output by using the current-mode control method, which enhances the response speed and provides the stable operation.

The FB/OLP pin voltage is internally added the slope compensation at the feedback control (refer to Section 5.Functional Block Diagram), and the target voltage, V_{SC}, is generated. The IC compares the voltage, V_{ROCP}, of a current detection resistor with the target voltage, V_{SC}, by the internal FB comparator, and controls the peak value of V_{ROCP} so that it gets close to V_{SC}, as shown in Figure10-5 and Figure10-6.

- Light load conditions
  When load conditions become lighter, the output voltage, V_{OUT}, increases. Thus, the feedback current from the error amplifier on the secondary-side also increases. The feedback current is sunk at the FB/OLP pin, transferred through a photo-coupler, PC1, and the FB/OLP pin voltage decreases. Thus, V_{SC} decreases, and the peak value of V_{ROCP} is controlled to be low, and the peak drain current of I_D decreases.
  This control prevents the output voltage from increasing.

- Heavy load conditions
  When load conditions become greater, the IC performs the inverse operation to that described above. Thus, V_{SC} increases and the peak drain current of I_D increases.
  This control prevents the output voltage from decreasing.

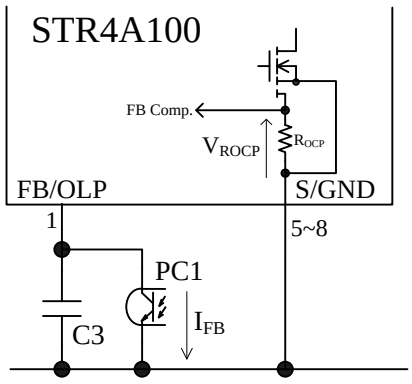


Figure10-5 FB/OLP pin peripheral circuit

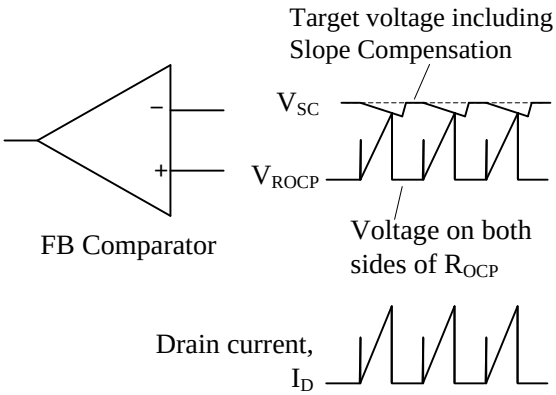


Figure10-6 Drain current, I_D, and FB comparator operation in steady operation

In the current mode control method, when the drain current waveform becomes trapezoidal in continuous operating mode, even if the peak current level set by the target voltage is constant, the on-time fluctuates based on the initial value of the drain current.

This results in the on-time fluctuating in multiples of the fundamental operating frequency as shown in Figure 10-7. This is called the subharmonics phenomenon.

In order to avoid this, the IC incorporates the Slope Compensation function. Because the target voltage is added a down-slope compensation signal, which reduces the peak drain current as the on-duty gets wider relative to the FB/OLP pin signal to compensate V_{SC}, the subharmonics phenomenon is suppressed.

Even if subharmonic oscillations occur when the IC has some excess supply being out of feedback control, such as during startup and load shorted, this does not affect performance of normal operation.

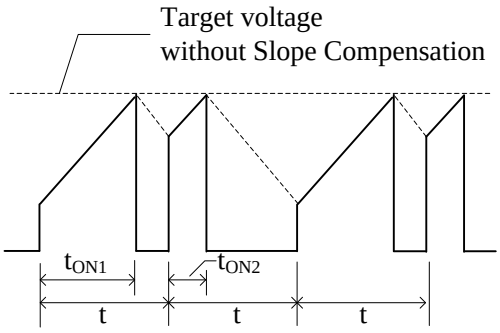


Figure 10-7 Drain current, I_D, waveform in subharmonic oscillation

In the current mode control method, the FB comparator and/or the OCP comparator may respond to the surge voltage resulting from the drain surge current in turning-on the power MOSFET. As a result, the power MOSFET may turn off irregularly. In order to prevent this response to the surge voltage in turning-on the power MOSFET, the Leading Edge Blanking, t_{BW}= 290 ns, is built-in.

10.6 Random Switching Function

The IC modulates its switching frequency randomly by superposing the modulating frequency on $f_{OSC(AVG)}$ in normal operation. This function reduces the conduction noise compared to others without this function, and simplifies noise filtering of the input lines of power supply.

10.7 Automatic Standby Mode Function

Automatic standby mode is activated automatically when the drain current, I_D, reduces under light load conditions, at which I_D is less than 20% to 25% of the maximum drain current (it is in the Overcurrent Protection state). The operation mode becomes burst oscillation, as shown in Figure 10-8. Burst mode reduces switching losses and improves power supply efficiency because of periodic non-switching intervals.

Generally, to improve efficiency under light load conditions, the frequency of the burst mode becomes just a few kilohertz. Because the IC suppresses the peak drain current well during burst mode, audible noises can be reduced.

If the VCC pin voltage decreases to $V_{CC(BIAS)}$= 9.4 V during the transition to the burst mode, the Bias Assist function is activated and stabilizes the Standby mode operation, because $I_{STARTUP}$ is provided to the VCC pin so that the VCC pin voltage does not decrease to $V_{CC(OFF)}$.

However, if the Bias Assist function is always activated during steady-state operation including standby mode, the power loss increases. Therefore, the VCC pin voltage should be more than $V_{CC(BIAS)}$, for example, by adjusting the turns ratio of the auxiliary winding and secondary winding and/or reducing the value of R2 in Figure 11-2 (refer to Section 11.1 Peripheral Components for a detail of R2).

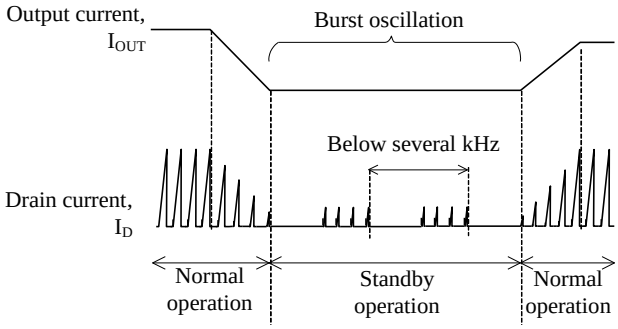


Figure 10-8 Auto Standby mode timing

10.8 Overcurrent Protection Function (OCP)

Overcurrent Protection Function (OCP) detects each drain peak current level of a power MOSFET on pulse-by-pulse basis, and limits the output power when the current level reaches to Drain Current Limit.

ICs with PWM control usually have some propagation delay time. The steeper the slope of the actual drain current at a high AC input voltage is, the larger the actual drain peak current is, compared to the Drain Current Limit. Thus, the peak current has some variation depending on the AC input voltage in the drain current limitation state.

In order to reduce the variation of peak current in the drain current limitation state, the IC incorporates a built-in Input Compensation function.

The Input Compensation function superposes a signal with a constant slope (Figure10-9) into the internal current detection signal and varies the internal threshold voltage.

When AC input voltage is low (ON Duty is broad), the Drain Current Limit after compensation increases. The difference of peak drain current become small compared with the case where the AC input voltage is high (ON Duty is narrow).

The compensation signal depends on ON Duty. The

relation between the ON Duty and the drain current limit after compensation I_{DLIM}' is expressed as Equation (5). When ON Duty is broader than 36 %, the drain current limit becomes a constant value $I_{DLIM(H)}$.

$$I_{DLIM}' = \frac{I_{DLIM(H)} - I_{DLIM(L)}}{36(\%)} \times Duty + I_{DLIM(L)} \quad (3)$$

where,
Duty : MOSFET ON Duty (%)
$I_{DLIM(H)}$: Drain current limit (ON Duty ≥ 36 %)
$I_{DLIM(L)}$: Drain current limit (ON Duty = 0 %)

	$I_{DLIM(H)}$	$I_{DLIM(L)}$
STR4A162	0.365 A	0.322 A
STR4A164	0.485 A	0.428 A

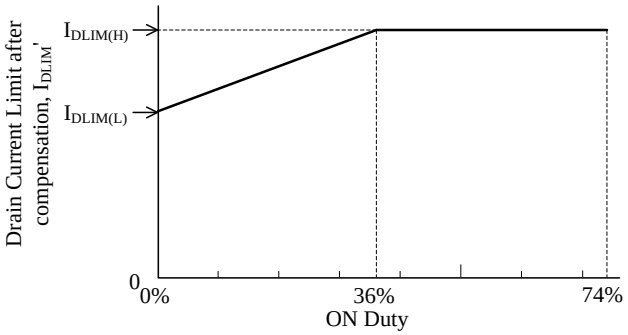


Figure10-9 Relationship between ON Duty and Drain Current Limit after compensation

10.9 Overvoltage Protection (OVP)

When a voltage between VCC pin and S/GND terminal increases to $V_{CC(OVP)}$ = 29.5 V or more, OVP Function is activated and stops switching operation.

When OVP Function is activated, VCC pin voltage decreases to Operation Stop Voltage $V_{CC(OFF)}$ = 8.1 V. After that, the IC reverts to the initial state by UVLO (Undervoltage Lockout) circuit, and the IC starts operation when VCC pin voltage increases to $V_{CC(ON)}$ = 15.2 V by Startup Current. Thus the intermittent operation by UVLO is repeated in OVP condition.

This intermittent operation reduces the stress of parts such as power MOSFET and secondary side rectifier diode. In addition, this operation reduces power consumption because the switching period in this intermittent operation is short compared with oscillation stop period. When the abnormal condition is removed, the IC returns to normal operation automatically.

In case the VCC pin voltage is provided by using auxiliary winding of transformer, the overvoltage conditions such as FB pin open can be detected because the VCC pin voltage is proportional to FB pin voltage. The approximate value of output voltage $V_{OUT(OVP)}$ in OVP condition is calculated by using Equation (4).

$$V_{OUT(OVP)} = \frac{\text{Output voltage in normal operation}}{\text{VCC pin voltage in normal operation}} \times 29.5(\text{V}) \quad (4)$$

10.10 Overload Protection Function (OLP)

Figure10-10 shows the FB/OLP pin peripheral circuit, and Figure10-11shows each waveform for OLP operation.

When the peak drain current of I_D is limited by OCP operation, the output voltage, V_{OUT}, decreases and the feedback current from the secondary photo-coupler becomes zero. Thus, the feedback current, I_{FB}, charges C3 connected to the FB/OLP pin and the FB/OLP pin voltage increases. When the FB/OLP pin voltage increases to $V_{FB(OLP)}$ = 8.1 V or more for the OLP delay time, t_{OLP} = 76 ms or more, the OLP function is activated and the IC stops switching operation.

When the OLP function is activated, the Bias Assist function is disabled. Thus the intermittent operation by UVLO is repeated during OLP state. When the fault condition is removed, the IC returns to normal operation automatically.

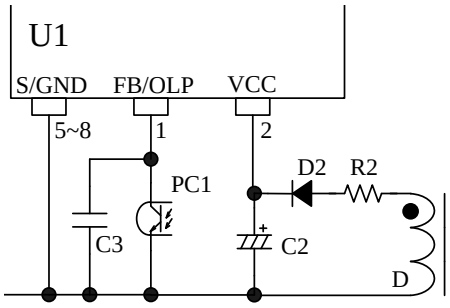


Figure10-10 FB/OLP pin peripheral circuit

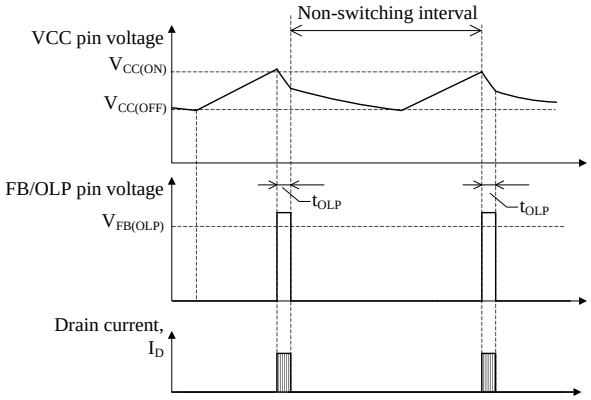


Figure10-11 OLP operational waveforms

10.11 Thermal Shutdown Function (TSD)

When the temperature of control circuit increases to $T_{j(TSD)}$ = 135 °C (min.) or more, Thermal Shutdown function is activated and stops switching operation.

When the OLP function is activated, the Bias Assist function is disabled. Thus the intermittent operation by UVLO is repeated. When the temperature of the IC decreases to $T_{j(TSD)} - T_{j(TSDHYS)}$, the IC returns to normal operation automatically.

11. Design Notes

11.1 External Components

Take care to use properly rated, including derating as necessary and proper type of components.

- **Output Electrolytic Capacitor**
  Apply proper derating to ripple current, voltage, and temperature rise. Use of high ripple current and low impedance types, designed for switch mode power supplies, is recommended.

- **FB/OLP Pin Peripheral Circuit**
  Figure 11-1 performs high frequency noise rejection and phase compensation, and should be connected close to these pins. The value of C3 is recommended to be about 2200p to 0.01µF, and should be selected based on actual operation in the application.

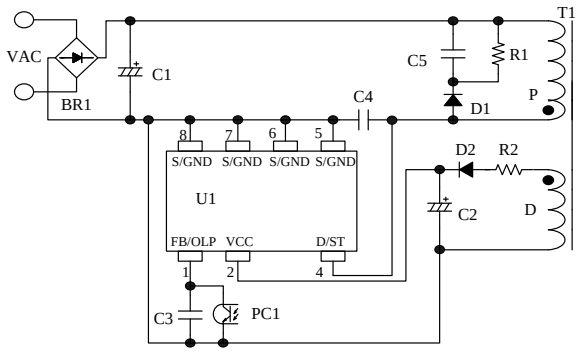


Figure 11-1 The IC peripheral circuit

- **VCC Pin Peripheral Circuit**
  The value of C2 in Figure 11-1 is generally recommended to be 10µ to 47µF (refer to Section 10.1 Startup Operation, because the startup time is determined by the value of C2)
  In actual power supply circuits, there are cases in which the VCC pin voltage fluctuates in proportion to the output current, I_{OUT} (see Figure 11-2), and the Overvoltage Protection function (OVP) on the VCC pin may be activated. This happens because C2 is charged to a peak voltage on the auxiliary winding D, which is caused by the transient surge voltage coupled from the primary winding when the power MOSFET turns off.

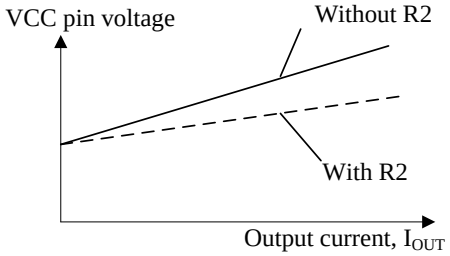


Figure 11-2 Variation of VCC pin voltage and power

For alleviating C2 peak charging, it is effective to add some value R2, of several tenths of ohms to several ohms, in series with D2 (see Figure 11-1). The optimal value of R2 should be determined using a transformer matching what will be used in the actual application, because the variation of the auxiliary winding voltage is affected by the transformer structural design.

- **D/ST Pin**
  Figure 11-3 shows D/ST pin peripheral circuit and Figure 11-4 shows D/ST pin waveform in normal operation.
  The internal power MOSFET connected to D/ST pin is permanently damaged when the D/ST pin voltage and the current exceed the Absolute Maximum Ratings. The D/ST pin voltage is tuned to be less than about 90 % of the Absolute Maximum Ratings (657 V) in all condition of actual operation, and the value of transformer and components should be selected based on actual operation in the application. And the D/ST pin voltage in normal operation is tuned to be the Recommended Operating Conditions, $V_{D/ST(OP)}$ < 584 V.
  The fast recovery diodes are recommended for using as D1, D2 and D51. (for D1, SARS is also recommended)

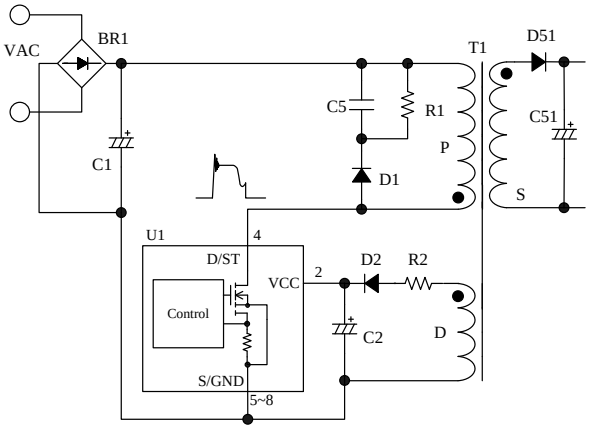


Figure 11-3 D/ST pin peripheral circuit

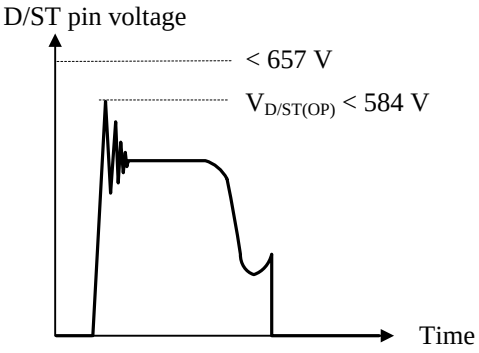


Figure 11-4 D/ST pin voltage waveform in normal operation

● **Phase Compensation**

A typical phase compensation circuit with a secondary shunt regulator (U51) is shown in Figure 11-5.

C52 and R53 are for phase compensation. The value of C52 and R53 are recommended to be around 0.047μF to 0.47μF and 4.7 kΩ to 220 kΩ, respectively. They should be selected based on actual operation in the application.

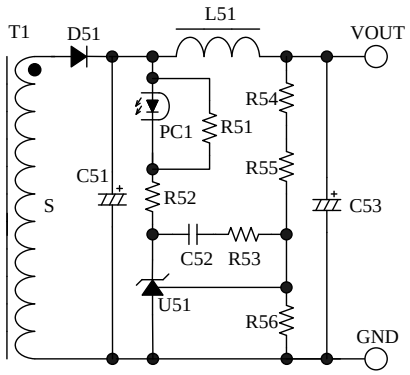


Figure 11-5 Peripheral circuit around secondary shunt regulator (U51)

• **Transformer**

Apply proper design margin to core temperature rise by core loss and copper loss.

Because the switching currents contain high frequency currents, the skin effect may become a consideration.

Choose a suitable wire gauge in consideration of the RMS current and a current density of about 3 to 4A/mm^2.

If measures to further reduce temperature are still necessary, the following should be considered to increase the total surface area of the wiring:

▫ Increase the number of wires in parallel.
▫ Use litz wires.
▫ Thicken the wire gauge.

Fluctuation of the VCC pin voltage by I_{OUT} worsens in the following cases, requiring a transformer designer to pay close attention to the placement of the auxiliary winding D:

▫ Poor coupling between the primary and secondary windings (this causes high surge voltage and is seen in a design with low output voltage and high output current)
▫ Poor coupling between the auxiliary winding D and the secondary stabilized output winding where the output line voltage is controlled constant by the output voltage feedback (this is susceptible to surge voltage)

In order to reduce the influence of surge voltage on the VCC pin, Figure11-6 shows winding structural examples that are considered the placement of the auxiliary winding D.

▫ Winding structural example (a): Separating the auxiliary winding D from the primary windings P1 and P2.
where: P1 and P2 are windings divided the primary winding into two.

▫ Winding structural example (b): Placing the auxiliary winding D within the secondary-side stabilized output winding, S1, in order to improve the coupling of those windings.
where: S1 is a stabilized output winding of secondary-side windings, controlled to constant voltage.

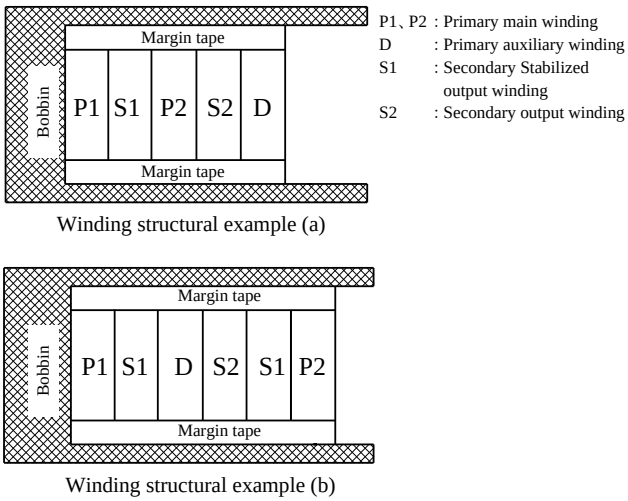


Figure11-6 Winding structural examples

11.2 PCB Trace Layout and Component Placement

PCB circuit trace design and component layout significantly affects operation, EMI noise, and power dissipation. Therefore, pay extra attention to these designs. In general, trace loops shown in Figure11-7 where high frequency currents flow should be wide, short, and small to reduce line impedance. In addition, earth ground traces affect radiated EMI noise, and wide, short traces should be taken into account.

Switch-mode power supplies consist of current traces with high frequency and high voltage, and thus trace design and component layouts should be done to comply with all safety guidelines.

Furthermore, because the power MOSFET has a positive thermal coefficient of $R_{DS(ON)}$, consider it when preparing a thermal design.

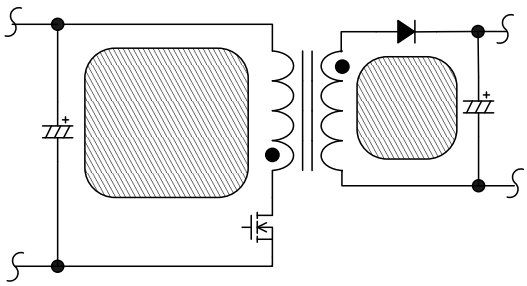


Figure11-7 High frequency current loops (hatched areas)

Figure11-8shows the circuit design example.

● IC Peripheral Circuit

(1) S/GND pin Trace Layout: S/GND pin to C1 to T1 (winding P) to D/ST pin
This is the main trace containing switching currents, and thus it should be as wide and short as possible. If C1 and the IC are distant from each other, placing a capacitor such as film capacitor (about 0.1μF and with proper voltage rating) close to the transformer or the IC is recommended to reduce impedance of the high frequency current loop.

(2) S/GND Pin Trace Layout: S/GND pin to C2(−) to T1(winding D) to R2 to D2 to C2(+) to VCC pin
This is the trace for supplying power to the IC, and thus it should be as wide and short as possible. If C2 and the IC are distant from each other, placing a capacitor such as film capacitor (about 0.1μ to 1.0μF) close to the VCC pin and the GND pin is recommended.

● Secondary Rectifier Smoothing Circuit Trace Layout: T1(winding S) to D51 to C51
This is the trace of the rectifier smoothing loop, carrying the switching current, and thus it should be as wide and short as possible.
If this trace is thin and long, inductance resulting from the loop may increase surge voltage at turning off the power MOSFET. Proper rectifier smoothing trace layout helps to increase margin against the power MOSFET breakdown voltage, and reduces stress on the clamp snubber circuit and losses in it.

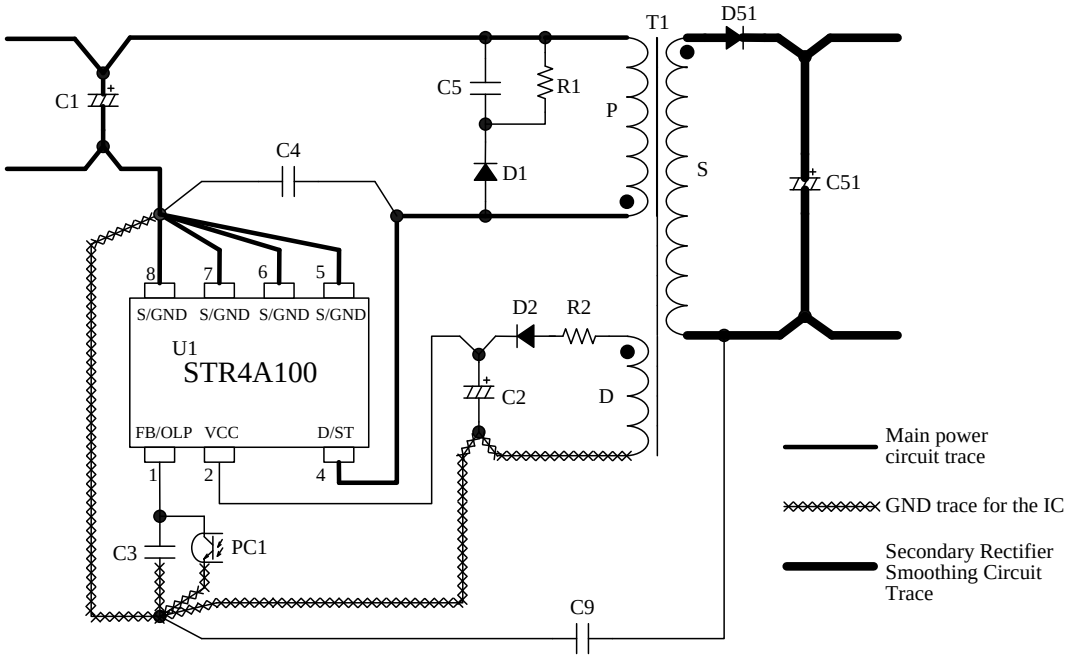


Figure11-8 Peripheral circuit example around the IC

12. Pattern Layout Example

The following show the PCB pattern layout example and the schematic of circuit using STR4A100 series (DIP8 type). Only the parts in the schematic are used. Other parts in PCB are leaved open.

Top view Bottom view

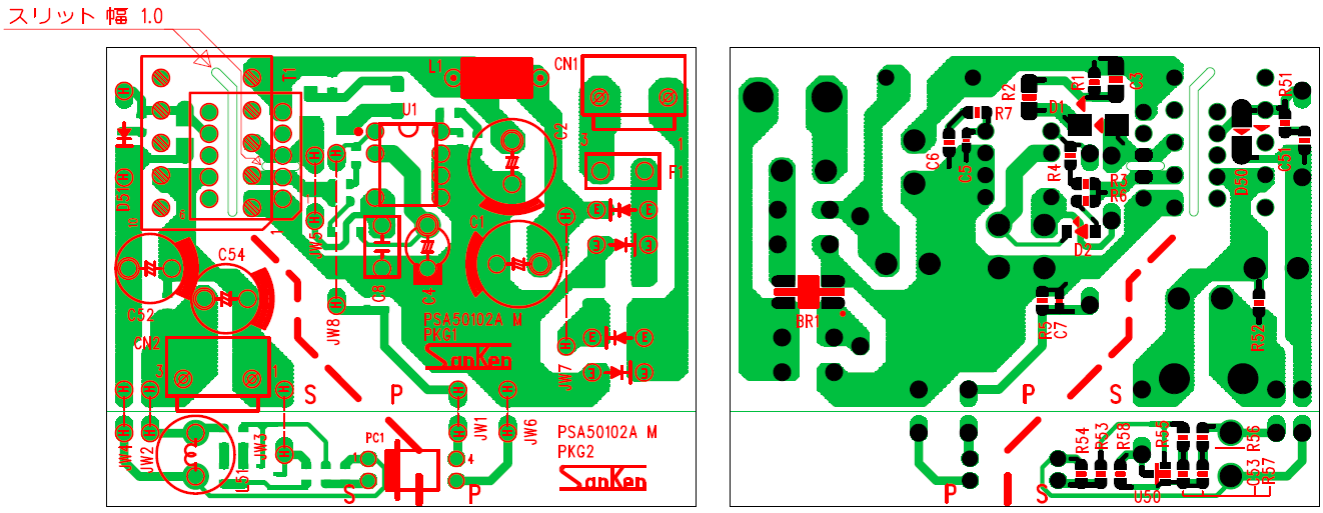


Figure 12-1 PCB circuit trace layout example (DIP8 type)

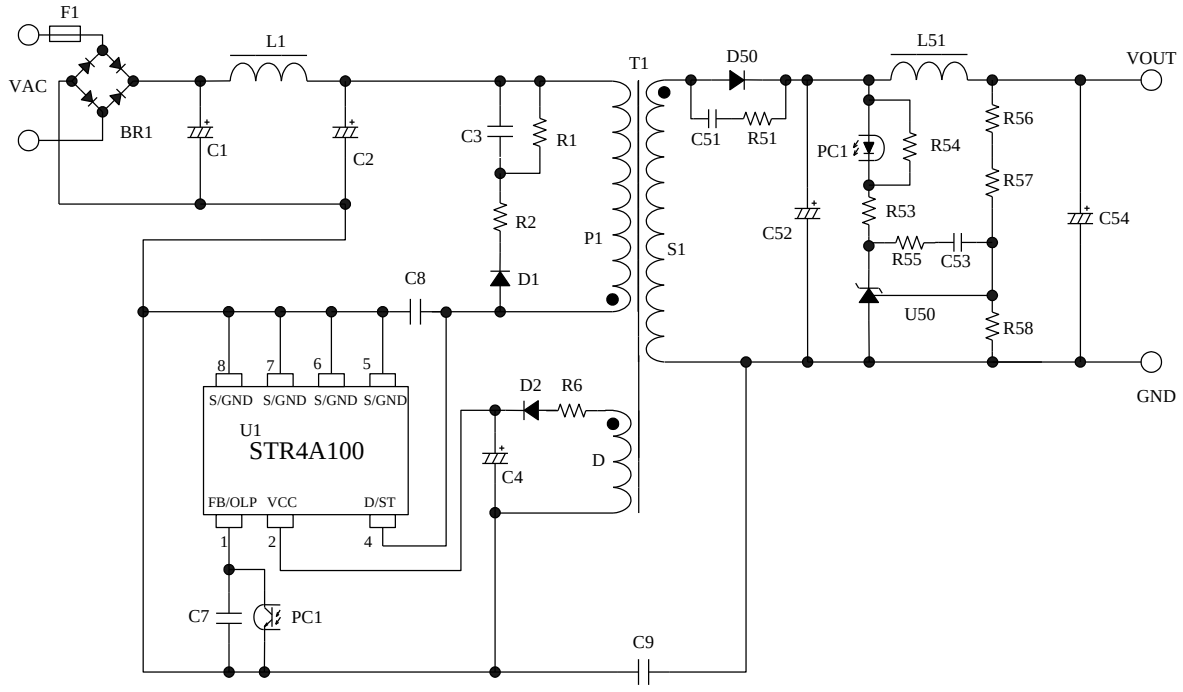


Figure 12-2 Circuit schematic for PCB circuit trace layout

The above circuit symbols correspond to these of Figure 12-1.

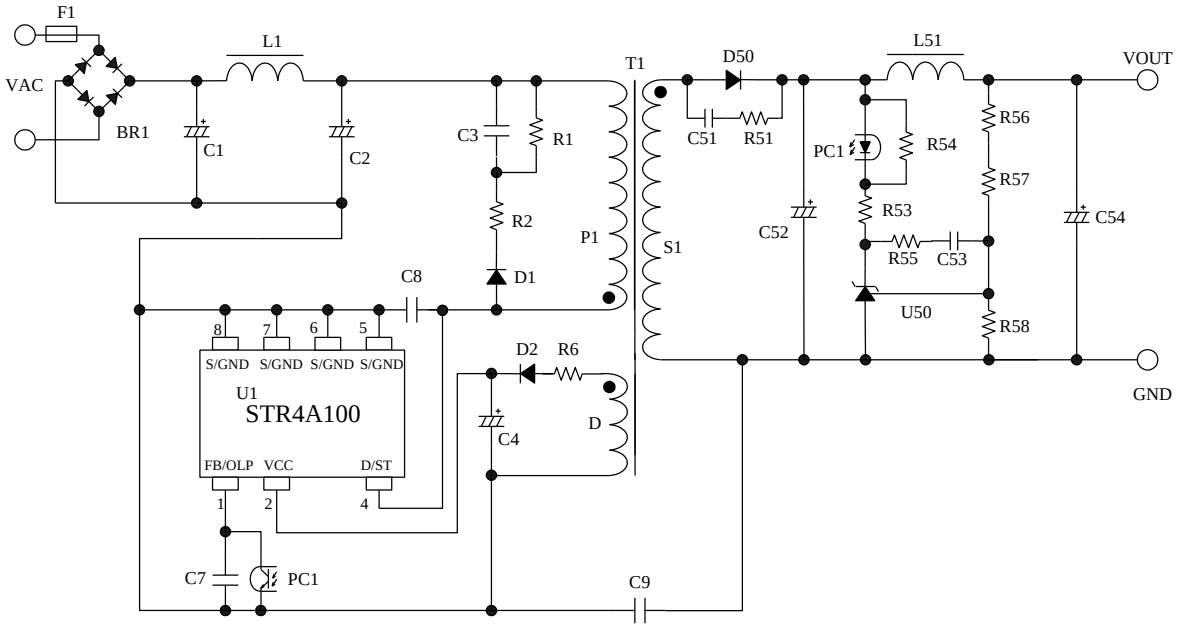
13. Reference Design of Power Supply

As an example, the following show the power supply specification, the circuit schematic, the bill of materials, and the transformer specification.

● Power supply specification

IC	STR4A162D
Input voltage	AC85V to AC265V
Maximum output power	5 W (peak)
Output voltage	5 V
Output current	1 A (max.)

● Circuit schematic



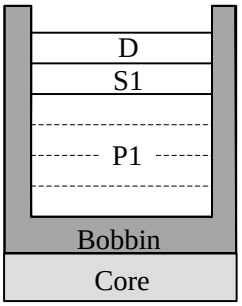
● Bill of materials

Symbol	Part type	Ratings(1)	Recommended Sanken Parts	Symbol	Part type	Ratings(1)	Recommended Sanken Parts
BR1	General, chip	600 V, 1 A	EM01A	T1	Transformer	See the specification	
F1	Fuse	AC 250 V, 1 A		L51	Inductor	5 µH	
L1 (2)	CM inductor	470 µH		D50	Schottky	40 V, 2.5 A	RK34
C1 (2)	Electrolytic	400 V, 10 µF		C51	Ceramic, chip	50 V, 2200 pF	
C2 (2)	Electrolytic	400 V, 10 µF		C52	Electrolytic	10 V, 1000 µF	
C3	Ceramic, chip	2 kV, 1000 pF		C53 (2)	Electrolytic	0.1 µF	
C4	Electrolytic	50 V, 10 µF		C54 (2)	Electrolytic	10 V, 470 µF	
C7	Ceramic, chip	4700 pF		R51	General, chip	22 Ω	
C8	Ceramic, chip	Open		R53	General, chip	220 Ω	
C9	Ceramic, Y1	250 V, 2200 pF		R54	General, chip	1.5 kΩ	
R1 (3)	Metal oxide, chip	470 kΩ		R55 (2)	General, chip	33 kΩ	
R2	General, chip	47 Ω		R56 (2)	General, chip	100 Ω	
R6 (2)	General, chip	2.2 Ω		R57	General, 1%	10 kΩ	
D1	General, chip	SARS01		R58	General, 1%	10 kΩ	
D2	First recovery	200 V, 1 A	AL01Z	U50	Shunt regulator	V_{REF} = 2.5 V TL431 or equiv	
U1	IC		STR4A162D	PC1	Photo-coupler	PC123 or equiv	

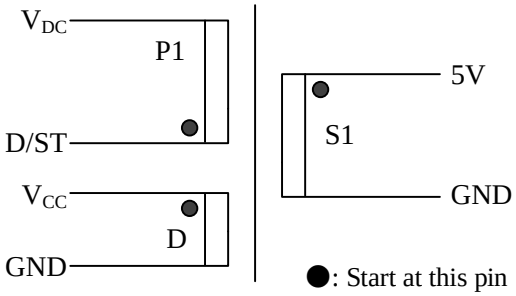
(1) Unless otherwise specified, the voltage rating of capacitor is 50 V or less and the power rating of resistor is 1/8 W or less.
(2) It is necessary to be adjusted based on actual operation in the application.
(3) Resistors applied high DC voltage and of high resistance are recommended to select resistors designed against electromigration or use combinations of resistors in series for that to reduce each applied voltage, according to the requirement of the application.

- Transformer specification
  - Primary inductance, L_P : 2.2 mH
  - Core size : EI-16
  - Al-value : 119 nH/N^2 (Center gap of about 0.3 mm)
  - Winding specification

Winding	Symbol	Number of turns (T)	Wire diameter (mm)	Construction	Wire
Primary winding	P1	136	φ 0.20	Four layers	Enameled Copper Wire
Output winding	S1	8	φ 0.3 × 2	Single-layer	Triple insulated wire
Auxiliary winding	D	21	φ 0.20	Single-layer	Enameled Copper Wire



Cross-section view



OPERATING PRECAUTIONS

In the case that you use Sanken products or design your products by using Sanken products, the reliability largely depends on the degree of derating to be made to the rated values. Derating may be interpreted as a case that an operation range is set by derating the load from each rated value or surge voltage or noise is considered for derating in order to assure or improve the reliability. In general, derating factors include electric stresses such as electric voltage, electric current, electric power etc., environmental stresses such as ambient temperature, humidity etc. and thermal stress caused due to self-heating of semiconductor products. For these stresses, instantaneous values, maximum values and minimum values must be taken into consideration. In addition, it should be noted that since power devices or IC's including power devices have large self-heating value, the degree of derating of junction temperature affects the reliability significantly.

Because reliability can be affected adversely by improper storage environments and handling methods, please observe the following cautions.

Cautions for Storage

- Ensure that storage conditions comply with the standard temperature (5 to 35°C) and the standard relative humidity (around 40 to 75%); avoid storage locations that experience extreme changes in temperature or humidity.
- Avoid locations where dust or harmful gases are present and avoid direct sunlight.
- Reinspect for rust on leads and solderability of the products that have been stored for a long time.

Cautions for Testing and Handling

When tests are carried out during inspection testing and other standard test periods, protect the products from power surges from the testing device, shorts between the product pins, and wrong connections. Ensure all test parameters are within the ratings specified by Sanken for the products.

Remarks About Using Silicone Grease with a Heatsink

- When silicone grease is used in mounting the products on a heatsink, it shall be applied evenly and thinly. If more silicone grease than required is applied, it may produce excess stress.
- Volatile-type silicone greases may crack after long periods of time, resulting in reduced heat radiation effect. Silicone greases with low consistency (hard grease) may cause cracks in the mold resin when screwing the products to a heatsink.
  Our recommended silicone greases for heat radiation purposes, which will not cause any adverse effect on the product life, are indicated below:

Type	Suppliers
G746	Shin-Etsu Chemical Co., Ltd.
YG6260	Momentive Performance Materials Inc.
SC102	Dow Corning Toray Co., Ltd.

Soldering

- When soldering the products, please be sure to minimize the working time, within the following limits:
  - 260 ± 5 °C 10 ± 1 s (Flow, 2 times)
  - 380 ± 10 °C 3.5 ± 0.5 s (Soldering iron, 1 time)
- Soldering should be at a distance of at least 1.5 mm from the body of the products (DIP8).

Electrostatic Discharge

- When handling the products, the operator must be grounded. Grounded wrist straps worn should have at least 1MΩ of resistance from the operator to ground to prevent shock hazard, and it should be placed near the operator.
- Workbenches where the products are handled should be grounded and be provided with conductive table and floor mats.
- When using measuring equipment such as a curve tracer, the equipment should be grounded.
- When soldering the products, the head of soldering irons or the solder bath must be grounded in order to prevent leak voltages generated by them from being applied to the products.
- The products should always be stored and transported in Sanken shipping containers or conductive containers, or be wrapped in aluminum foil.

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