



STS20N3LLH6

N-channel 30 V, 0.004 Ω , 20 A, SO-8
STripFET™ VI DeepGATE™ Power MOSFET

Features

Type	V _{DSS}	R _{DS(on)} max	I _D
STS20N3LLH6	30 V	0.0047 Ω	20 A

- R_{DS(on)} * Q_g industry benchmark
- Extremely low on-resistance R_{DS(on)}
- High avalanche ruggedness
- Low gate drive power losses
- Very low switching gate charge

Application

- Switching applications

Description

This product utilizes the 6th generation of design rules of ST's proprietary STripFET™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest R_{DS(on)} in all packages.

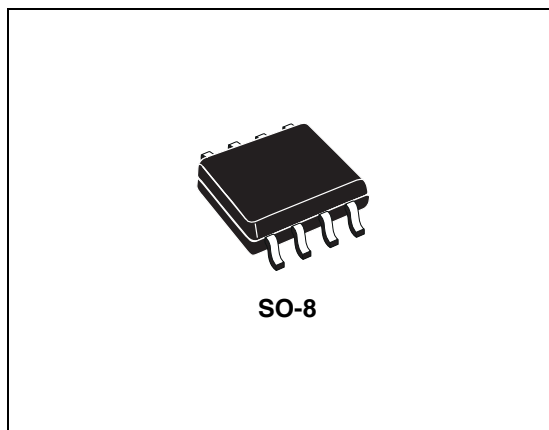


Figure 1. Internal schematic diagram

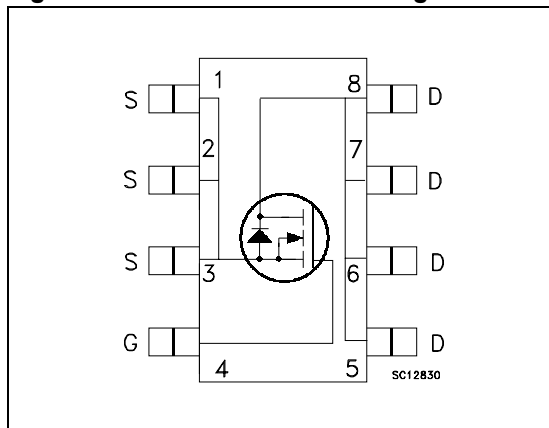


Table 1. Device summary

Order code	Marking	Package	Packaging
STS20N3LLH6	20G3L	SO-8	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	30	V
$V_{GS}^{(1)}$	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	20	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	12.5	A
$I_{DM}^{(2)}$	Drain current (pulsed)	80	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	2.7	W
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	$^{\circ}\text{C}$

1. Continuous mode

2. Pulse width limited by safe operating area

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-amb}^{(1)}$	Thermal resistance junction-ambient	47	$^{\circ}\text{C}/\text{W}$

1. When mounted on FR-4 board of 1inch², 2oz Cu, $t < 10\text{ sec}$

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 250 µA, V _{GS} = 0	30			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = Max rating, V _{DS} = Max rating @ 125 °C			1 10	µA µA
I _{GSS}	Gate body leakage current (V _{DS} = 0)	V _{GS} = ±20 V			±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 µA	1			V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10 V, I _D = 10 A V _{GS} = 4.5 V, I _D = 10 A		0.004 0.0059	0.0047 0.0075	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0	-	1690 290 176	-	pF pF pF
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	V _{DD} = 15 V, I _D = 20 A V _{GS} = 4.5 V <i>Figure 19</i>	-	17 8 6	-	nC nC nC
R _G	Gate Input Resistance	f = 1 MHz Gate DC Bias = 0 Test signal level = 20 mV open drain	-	1.7	-	Ω

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=15\text{ V}$, $I_D=10\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=4.5\text{ V}$ Figure 13	-	9.5	-	ns
t_r	Rise time			30		ns
$t_{d(off)}$	Turn-off delay time			37		ns
t_f	Fall time			12		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		20	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		80	A
$V_{SD}^{(2)}$	Forward on Voltage	$I_{SD}=20\text{ A}$, $V_{GS}=0$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD}=20\text{ A}$, $di/dt=100\text{ A}/\mu\text{s}$, $V_{DD}=20\text{ V}$, $T_j=150\text{ }^\circ\text{C}$ Figure 15	-	14		ns
Q_{rr}	Reverse recovery charge			16.8		nC
I_{RRM}	Reverse recovery current			1.4		A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

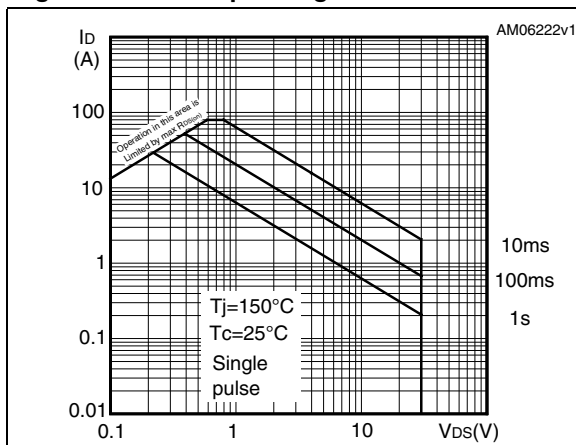


Figure 3. Thermal impedance

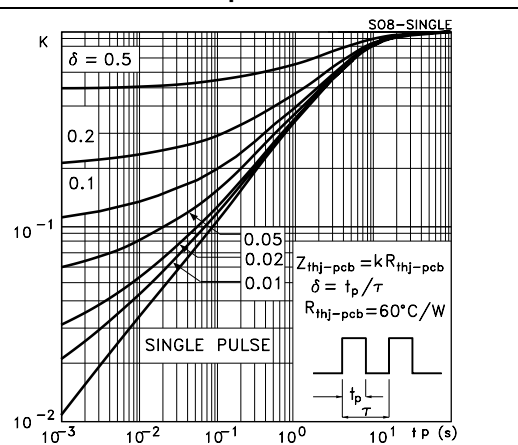


Figure 4. Output characteristics

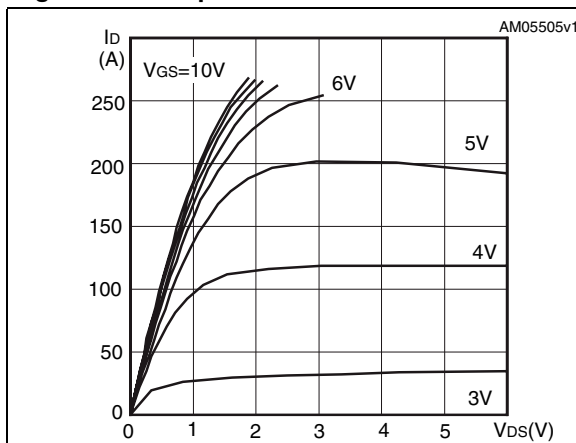


Figure 5. Transfer characteristics

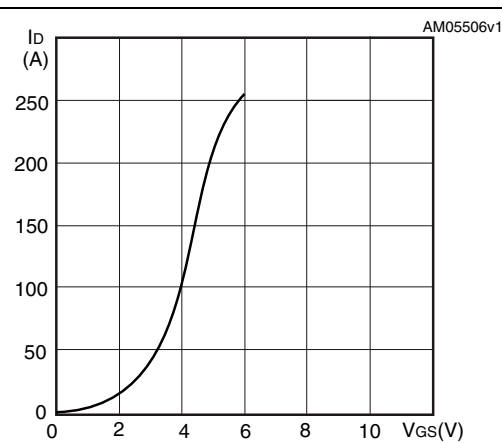


Figure 6. Normalized BVdss vs temperature

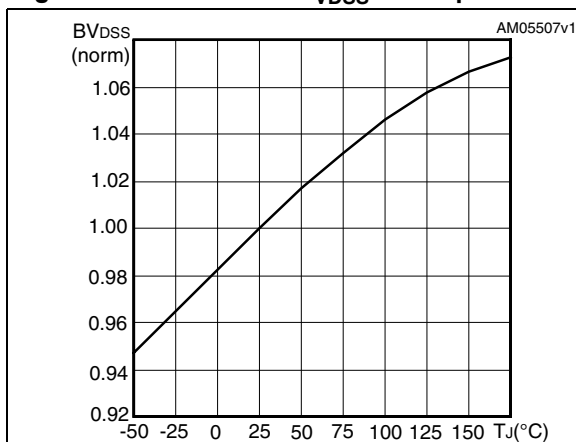


Figure 7. Static drain-source on resistance

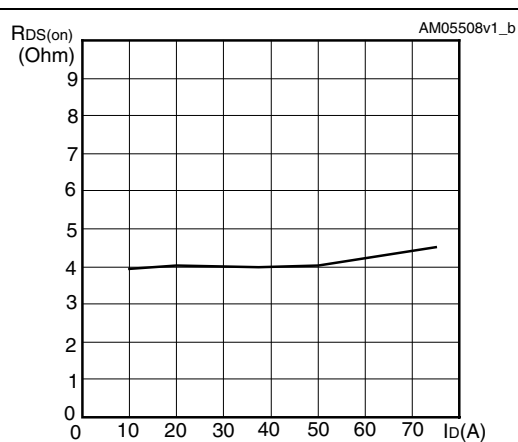
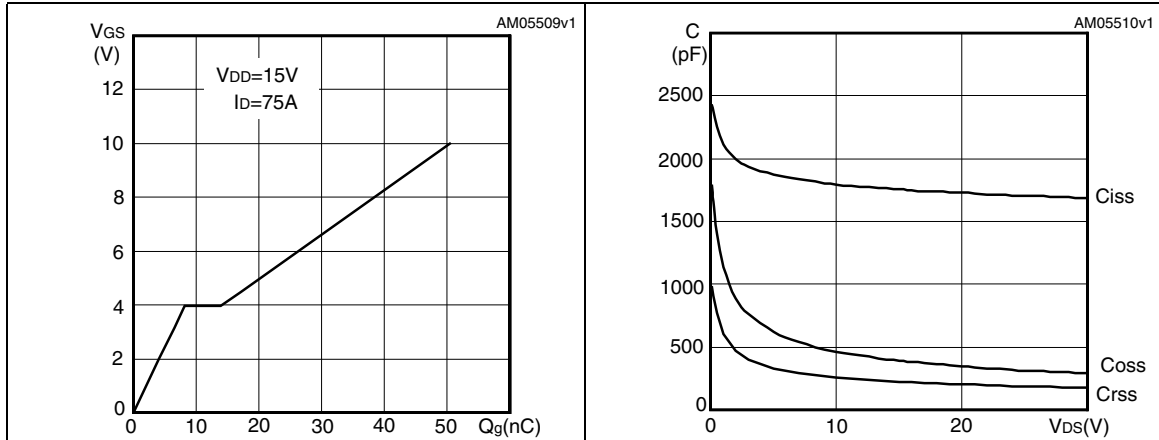
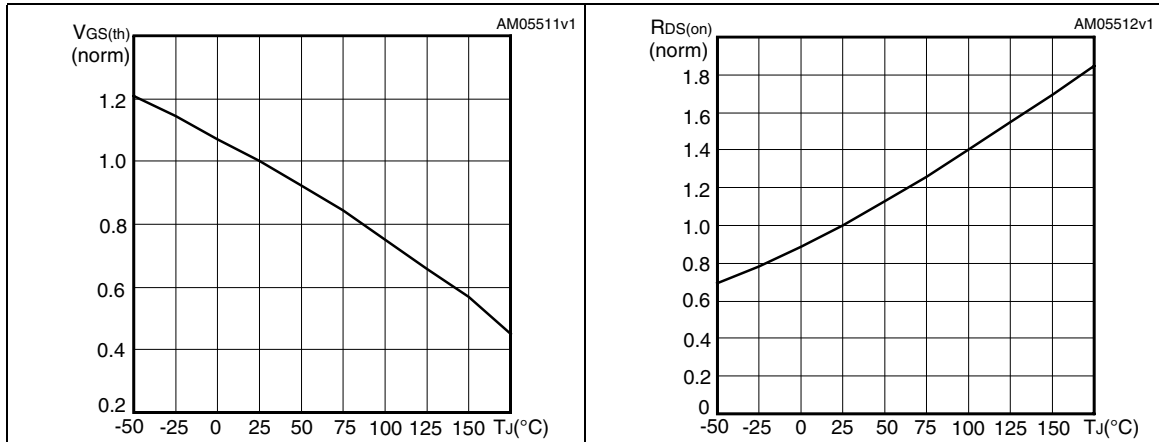
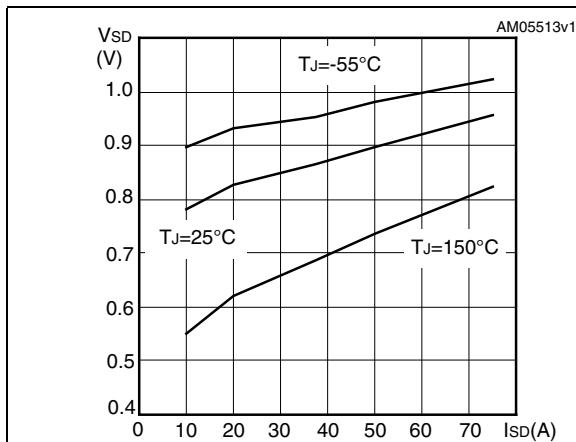


Figure 8. Gate charge vs gate-source voltage **Figure 9. Capacitance variations****Figure 10. Normalized gate threshold voltage vs temperature** **Figure 11. Normalized on resistance vs temperature****Figure 12. Source-drain diode forward characteristics**

3 Test circuits

Figure 13. Switching times test circuit for resistive load

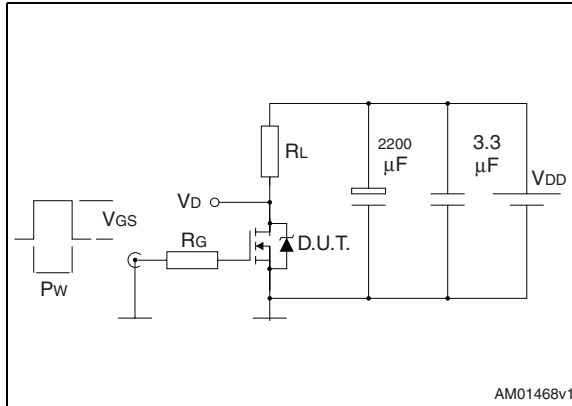


Figure 14. Gate charge test circuit

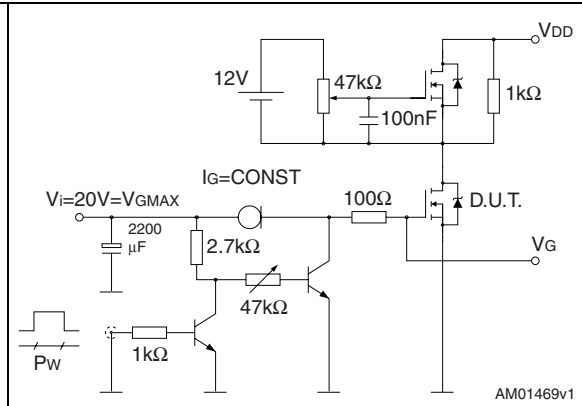


Figure 15. Test circuit for inductive load switching and diode recovery times

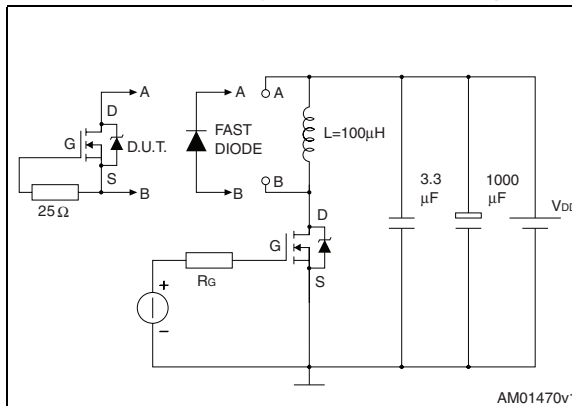


Figure 16. Unclamped inductive load test circuit

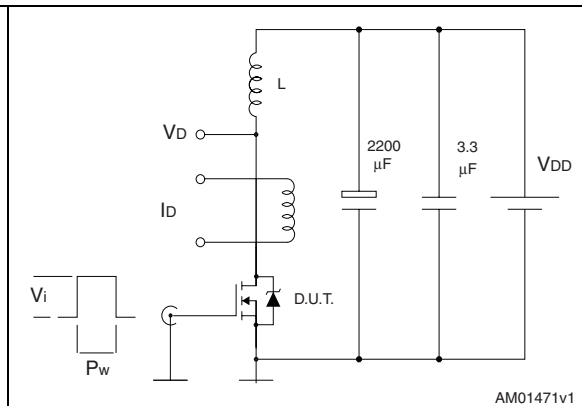


Figure 17. Unclamped inductive waveform

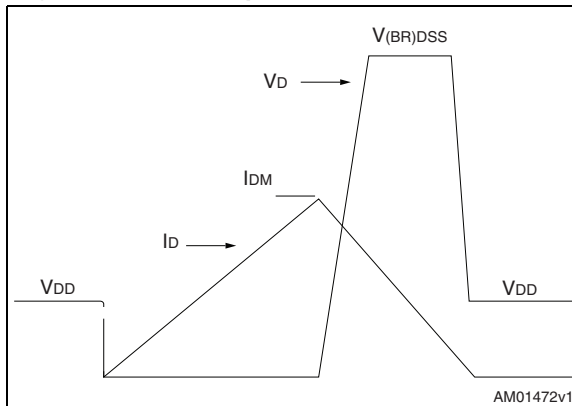


Figure 18. Switching time waveform

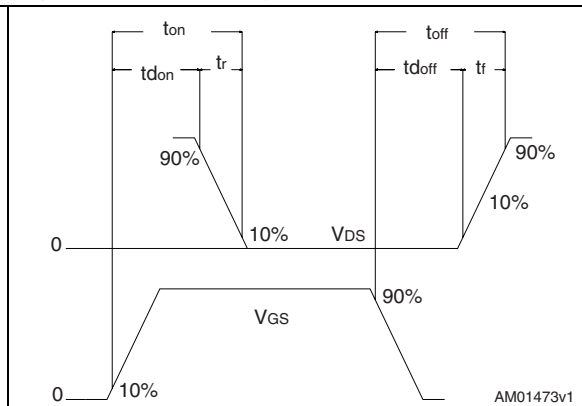
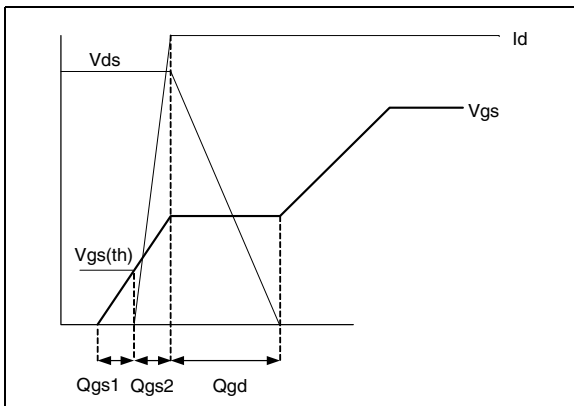


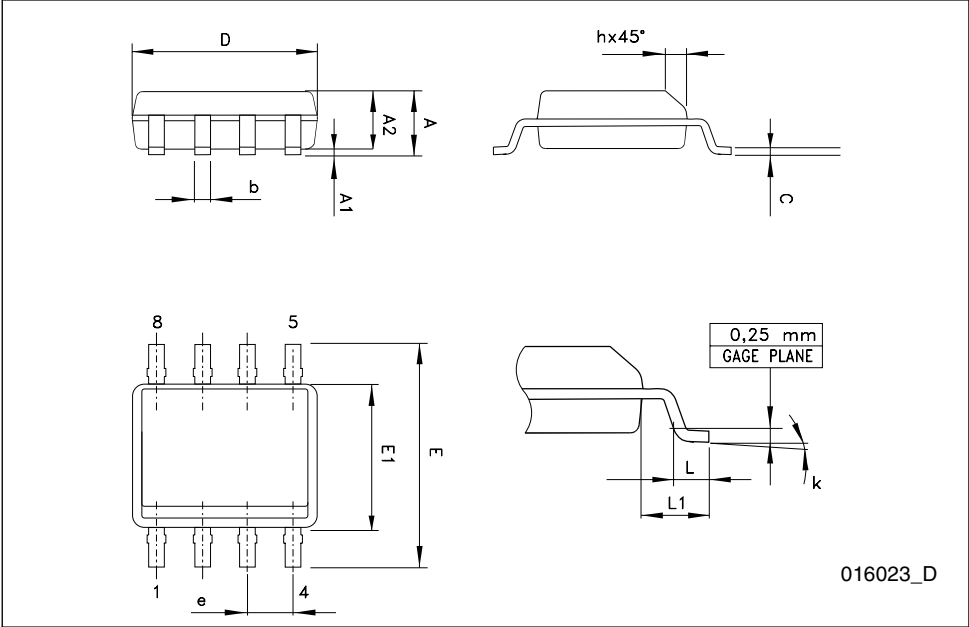
Figure 19. Gate charge waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

SO-8 mechanical data			
DIM.	mm.		
	min.	typ	max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°



5 Revision history

Table 8. Document revision history

Date	Revision	Changes
23-Mar-2009	1	First release
17-Mar-2010	2	Document status promoted from preliminary data to datasheet.

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