



STS7C4F30L

N-CHANNEL 30V - 0.018 Ω - 7A SO-8

P-CHANNEL 30V - 0.070 Ω - 4A SO-8

STripFET™ POWER MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STS7C4F30L(N-Channel)	30 V	<0.022 Ω	7 A
STS7C4F30L(P-Channel)	30 V	<0.080 Ω	4 A

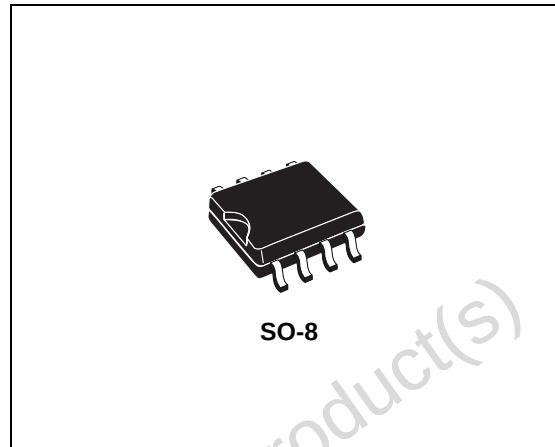
- TYPICAL R_{DS(on)} (N-Channel) = 0.018 Ω
- TYPICAL R_{DS(on)} (P-Channel) = 0.070 Ω
- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLY
- LOW THRESHOLD DRIVE

DESCRIPTION

This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

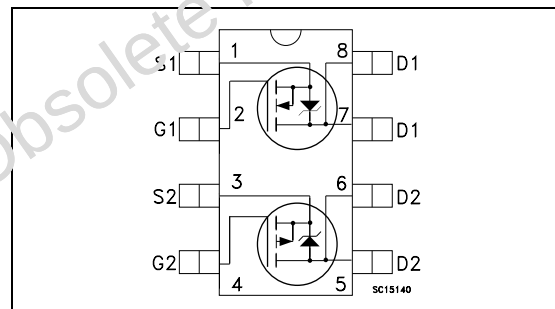
APPLICATIONS

- DC/DC CONVERTERS
- BATTERY MANAGEMENT IN NOMADIC EQUIPMENT
- POWER MANAGEMENT IN CELLULAR PHONES



SO-8

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	N-CHANNEL	P-CHANNEL	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	30	30	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 k Ω)	30	30	V
V _{GS}	Gate- source Voltage	± 20	± 20	V
I _D	Drain Current (continuous) at T _C = 25°C Single Operating	7	4	A
I _D	Drain Current (continuous) at T _C = 100°C Single Operating	4.4	2.5	A
I _{DM} (•)	Drain Current (pulsed)	28	16	A
P _{tot}	Total Dissipation at T _C = 25°C Dual Operating	1.6		W
	Total Dissipation at T _C = 25°C Single Operating	2		W
T _{stg}	Storage Temperature	-60 to 150		°C
T _j	Max. Operating Junction Temperature	150		°C

(•) Pulse width limited by safe operating area.

Note: P-CHANNEL MOSFET actual polarity of voltages and current has to be reversed

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THERMAL DATA

Rthj-amb(1)	Thermal Resistance Junction-ambient	Single Operation	62.5	°C/W
T _l	Maximum Lead Temperature For Soldering Purpose	Dual Operating	78	°C/W
		Purpose	300	°C

(1) when mounted on 0.5 in² pad of 2 oz. copper

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 µA, V _{GS} = 0	n-ch p-ch	30 30			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating T _C = 125°C				1 10	µA µA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20V V _{GS} = ± 20V	n-ch p-ch			±100 ±100	nA nA

ON

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} I _D = 250 µA	n-ch p-ch	1 1	1.6 1.6	2.5 2.5	V V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V I _D = 3.5 A V _{GS} = 10 V I _D = 2 A V _{GS} = 4.5 V I _D = 3.5 A V _{GS} = 4.5 V I _D = 2 A	n-ch p-ch n-ch p-ch		0.018 0.070 0.021 0.085	0.022 0.080 0.026 0.10	Ω Ω Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
g _{fs} (*)	Forward Transconductance	V _{DS} = 15 V I _D = 3.5 A V _{DS} = 15 V I _D = 2 A	n-ch p-ch		10 10		S S
C _{iss}	Input Capacitance		n-ch p-ch		1050 1350		pF pF
C _{oss}	Output Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0	n-ch p-ch		250 490		pF pF
C _{rss}	Reverse Transfer Capacitance		n-ch p-ch		85 130		pF pF

ELECTRICAL CHARACTERISTICS (continued)**SWITCHING ON**

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	N-CHANNEL $V_{DD} = 15\text{ V}$ $I_D = 3.5\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$	n-ch p-ch		22 25		ns ns
t_r	Rise Time	P-CHANNEL $V_{DD} = 15\text{ V}$ $I_D = 2\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$ (Resistive Load, Figure 1)	n-ch p-ch		60 35		ns ns
Qg	Total Gate Charge	N-CHANNEL $V_{DD} = 24\text{ V}$ $I_D = 7\text{ A}$ $V_{GS} = 5\text{ V}$	n-ch p-ch		17.5 12.5	23 16	nC nC
Qgs	Gate-Source Charge	P-CHANNEL $V_{DD} = 24\text{ V}$ $I_D = 4\text{ A}$ $V_{GS} = 5\text{ V}$ (see test circuit, Figure 2)	n-ch p-ch		4 5		nC nC
Qgd	Gate-Drain Charge		n-ch p-ch		7 3		nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off Delay Time	N-CHANNEL $V_{DD} = 15\text{ V}$ $I_D = 3.5\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$	n-ch p-ch		42 125		ns ns
t_f	Fall Time	P-CHANNEL $V_{DD} = 15\text{ V}$ $I_D = 2\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$ (Resistive Load, Figure 1)	n-ch p-ch		10 35		ns ns

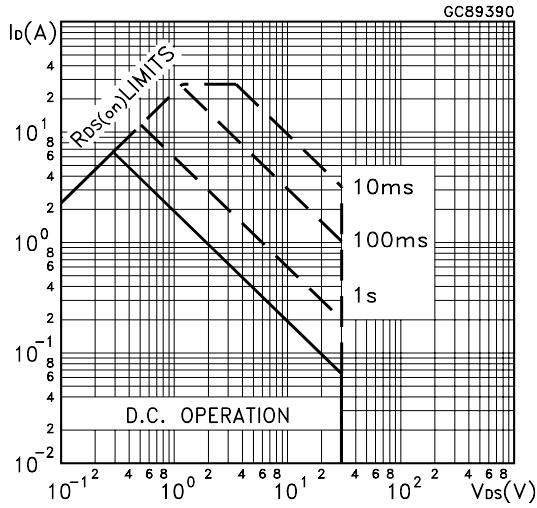
SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current		n-ch p-ch			7 4	A A
$I_{SDM}(\bullet)$	Source-drain Current (pulsed)		n-ch p-ch			28 16	A A
$V_{SD}(\ast)$	Forward On Voltage	$I_{SD} = 7\text{ A}$ $V_{GS} = 0$ $I_{SD} = 4\text{ A}$ $V_{GS} = 0$	n-ch p-ch			1.2 1.2	V V
t_{rr}	Reverse Recovery Time	N-CHANNEL $I_{SD} = 7\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 15\text{ V}$ $T_J = 150\text{ }^\circ\text{C}$	n-ch p-ch		50 45		ns ns
Q_{rr}	Reverse Recovery Charge	P-CHANNEL $I_{SD} = 4\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 15\text{ V}$ $T_J = 150\text{ }^\circ\text{C}$ (see test circuit, Figure 3)	n-ch p-ch		40 36		nC nC
I_{RRM}	Reverse Recovery Current		n-ch p-ch		1.6 1.6		A A

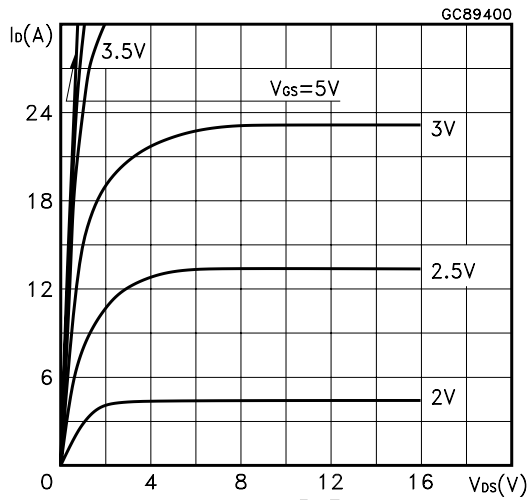
(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

(•) Pulse width limited by safe operating area.

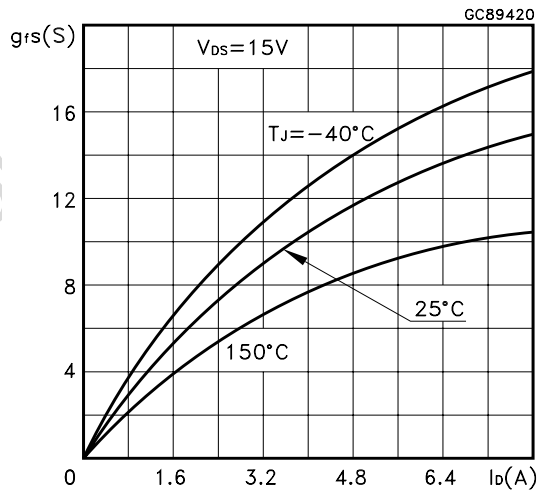
Safe Operating Area **n-ch**



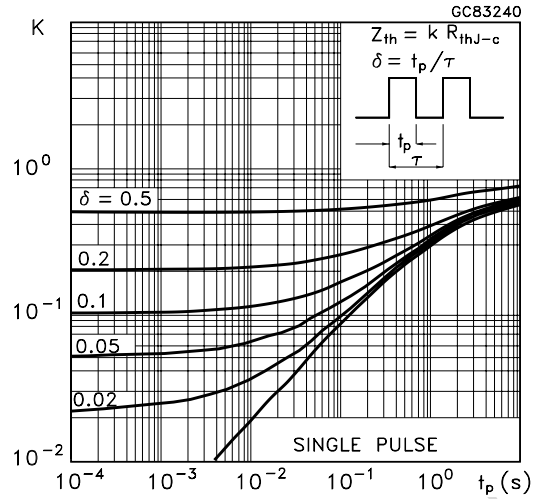
Output Characteristics **n-ch**



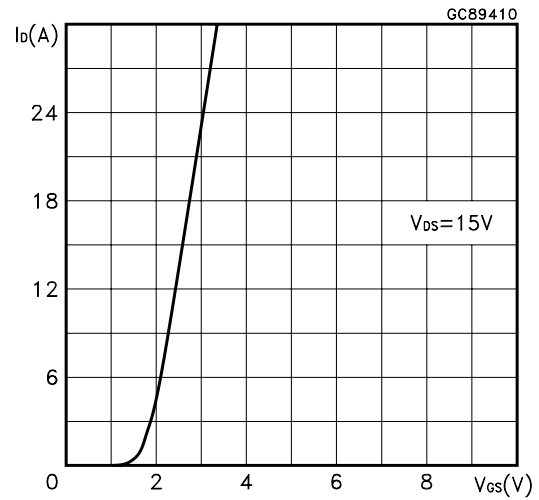
Transconductance **n-ch**



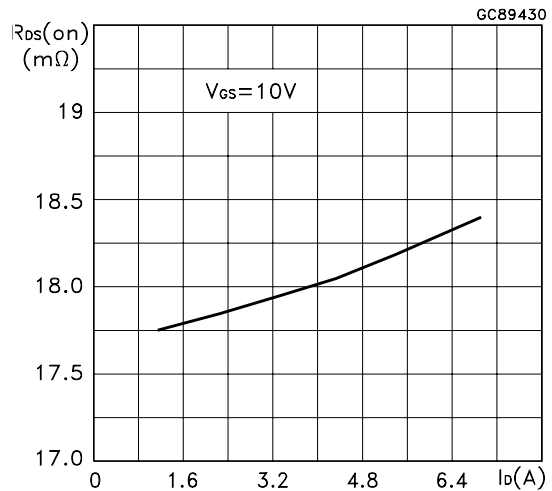
Thermal Impedance **n-ch**



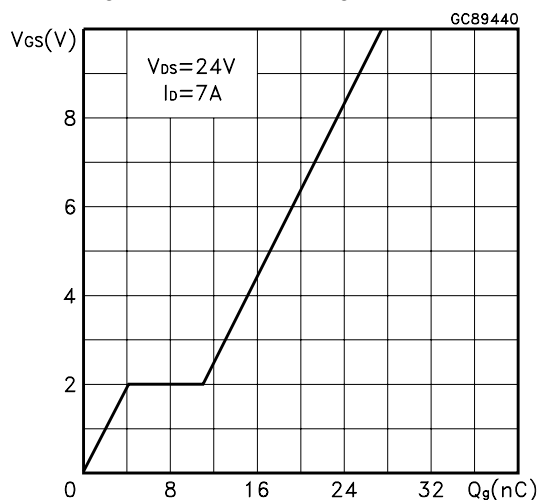
Transfer Characteristics **n-ch**



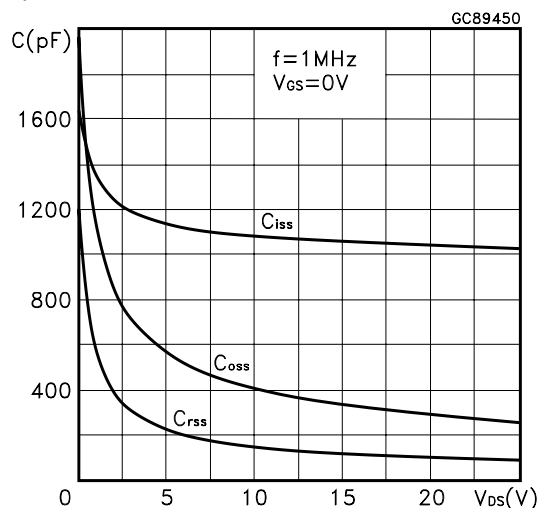
Static Drain-source On Resistance **n-ch**



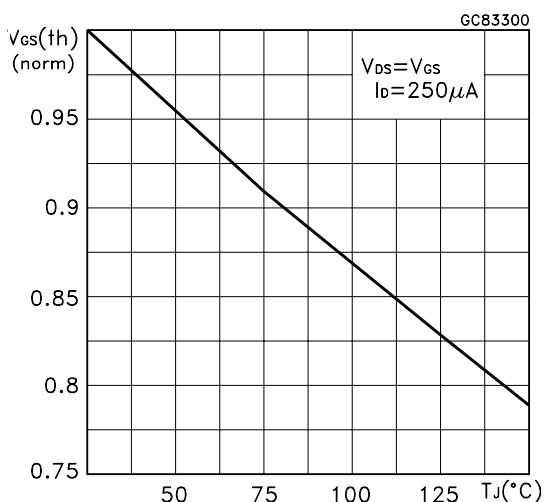
Gate Charge vs Gate-source Voltage **n-ch**



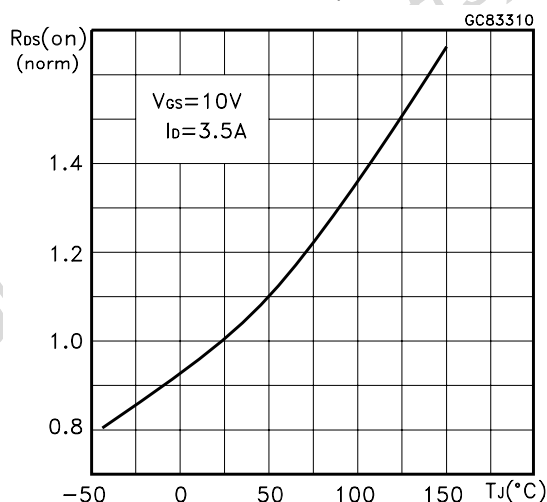
Capacitance Variations **n-ch**



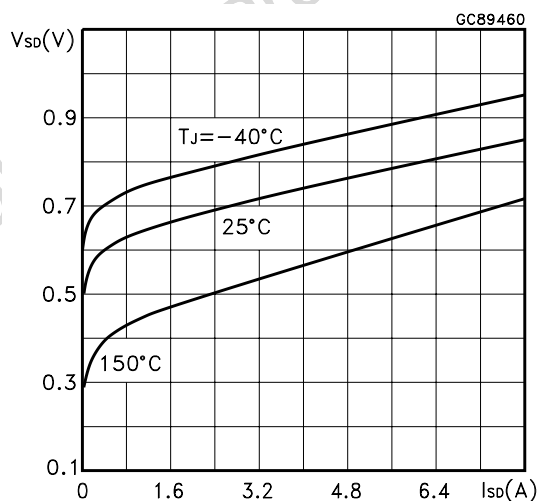
Normalized Gate Threshold Voltage vs Temperature **n-ch**



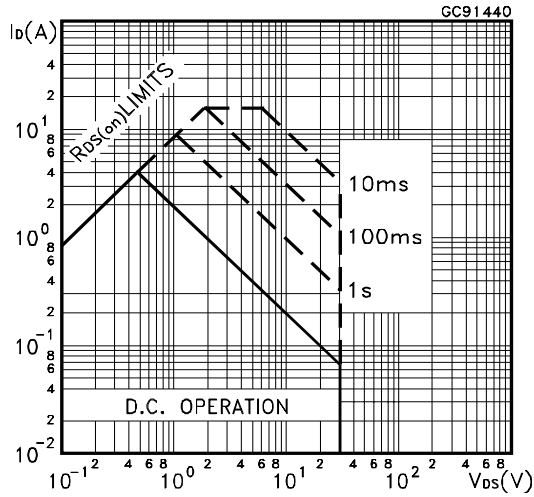
Normalized on Resistance vs Temperature **n-ch**



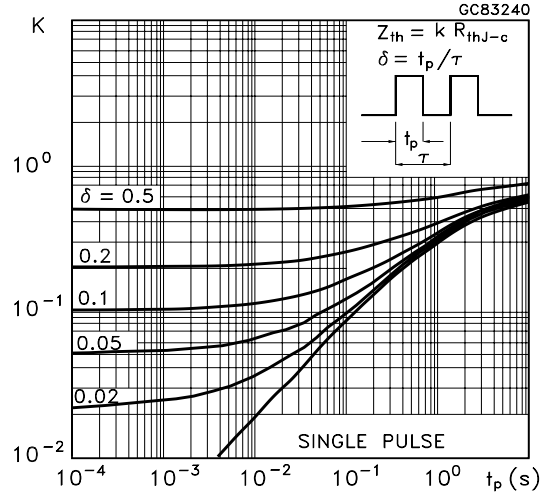
Source-drain Diode Forward Characteristics **n-ch**



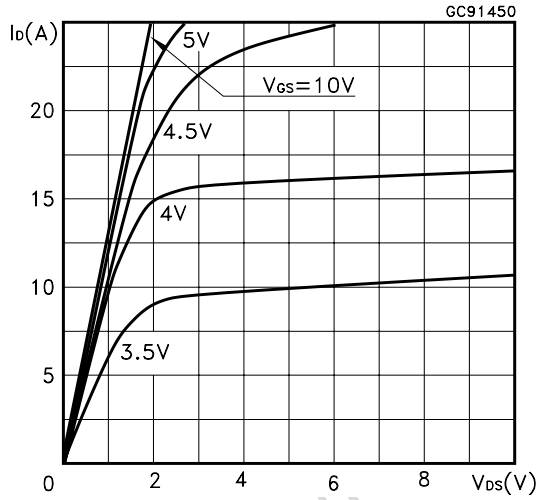
Safe Operating Area **p-ch**



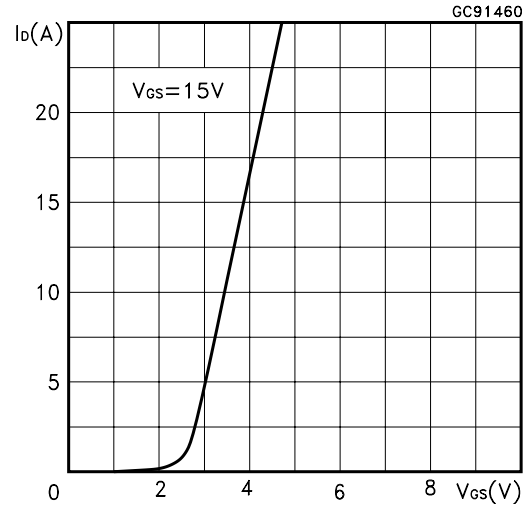
Thermal Impedance **p-ch**



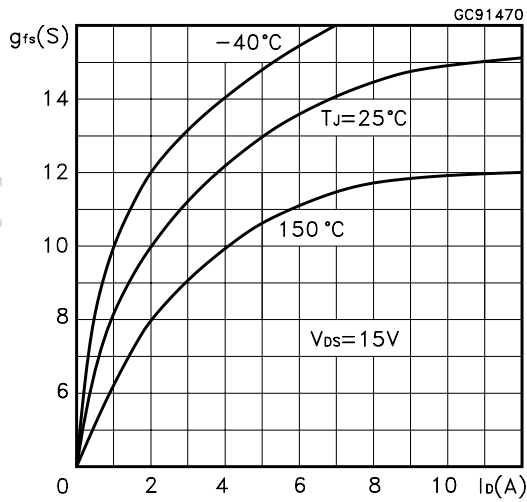
Output Characteristics **p-ch**



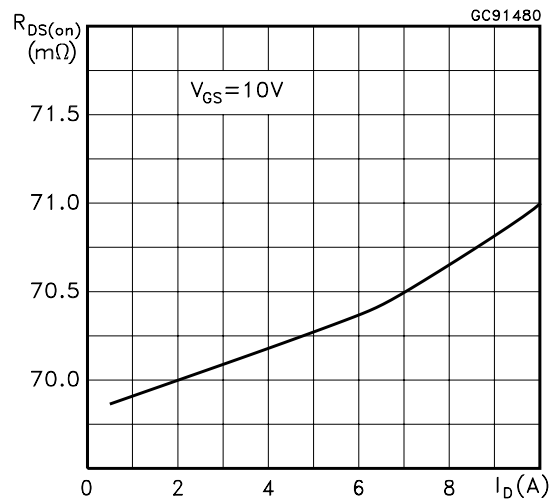
Transfer Characteristics **p-ch**



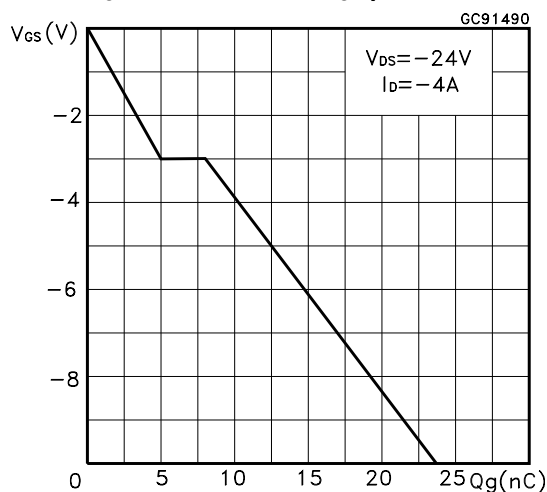
Transconductance **p-ch**



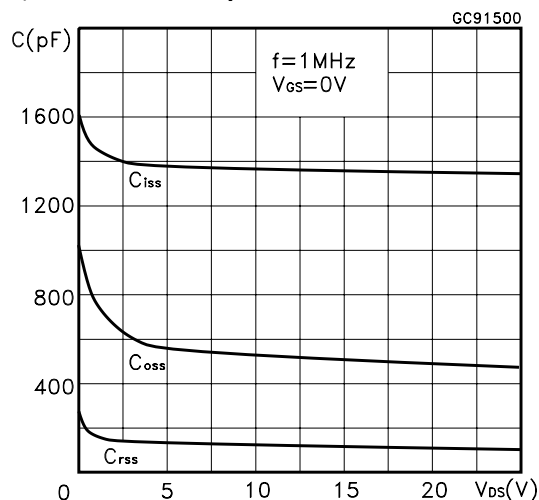
Static Drain-source On Resistance **p-ch**



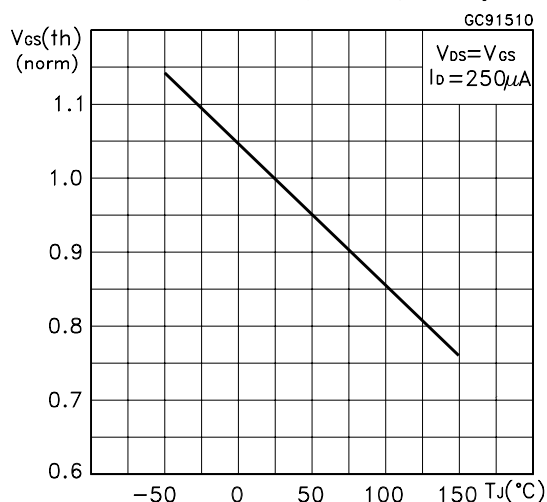
Gate Charge vs Gate-source Voltage **p-ch**



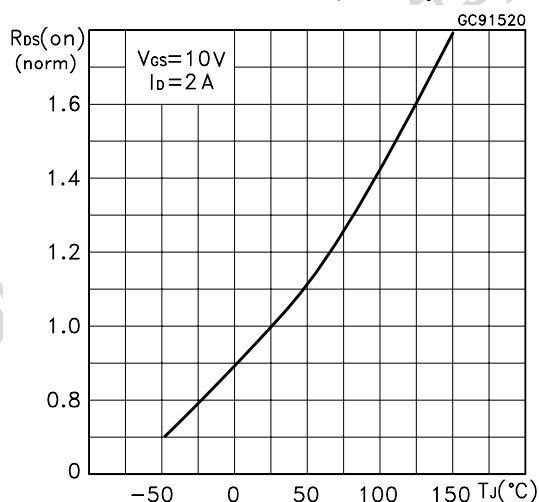
Capacitance Variations **p-ch**



Normalized Gate Threshold Voltage vs Temperature **p-ch**



Normalized on Resistance vs Temperature **p-ch**



Source-drain Diode Forward Characteristics **p-ch**

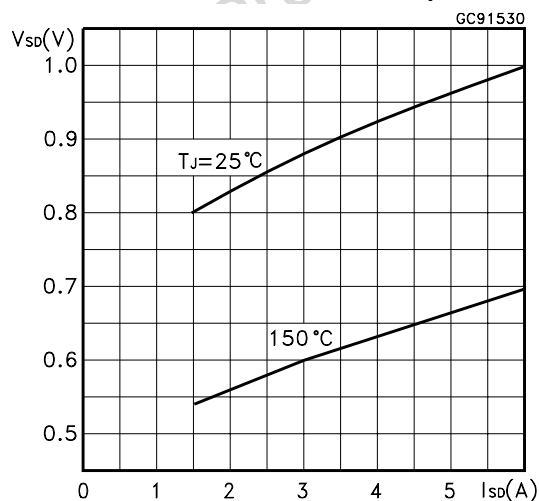


Fig. 1: Switching Times Test Circuits For Resistive Load

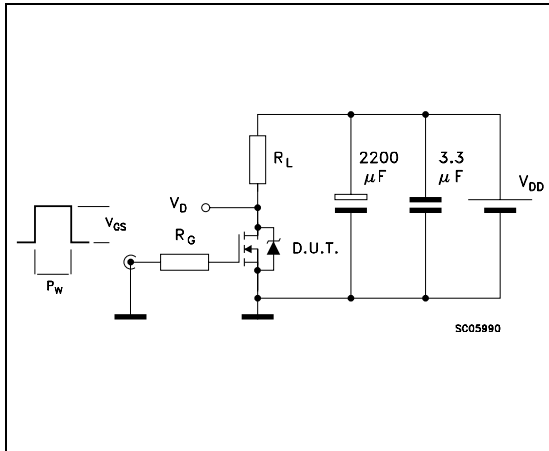


Fig. 2: Gate Charge test Circuit

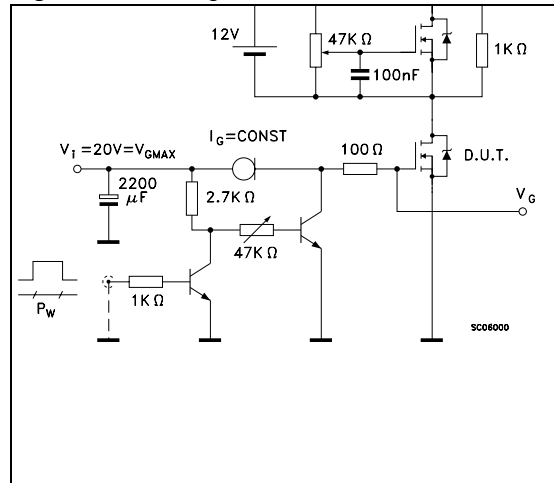
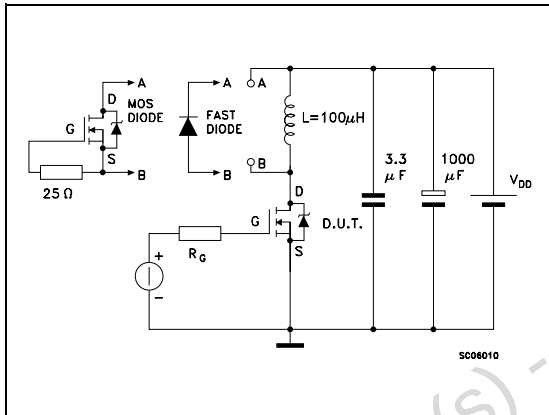
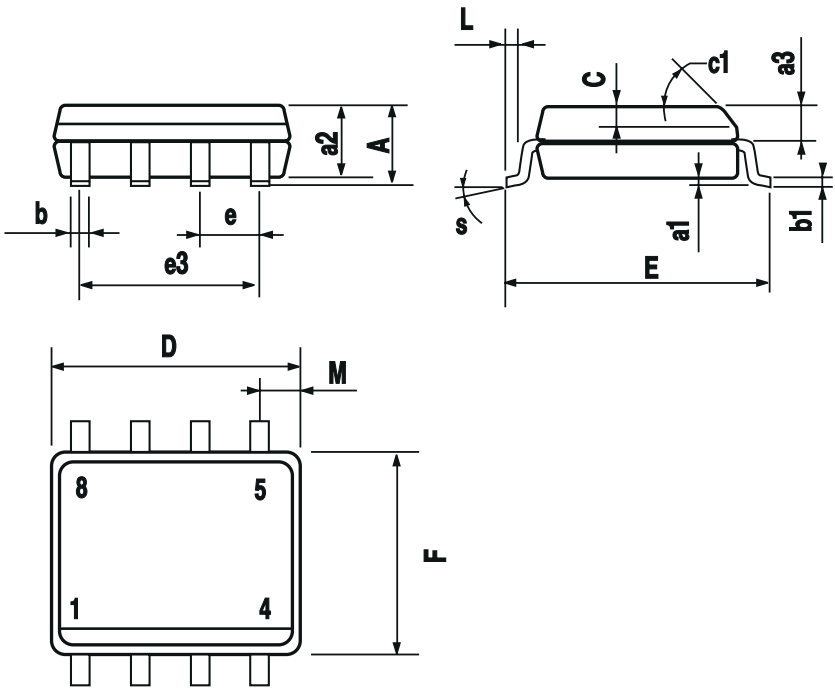


Fig. 3: Test Circuit For Diode Recovery Behaviour



SO-8 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



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