AN5088
Application note

Rectifiers thermal management, handling and mounting recommendations

Introduction

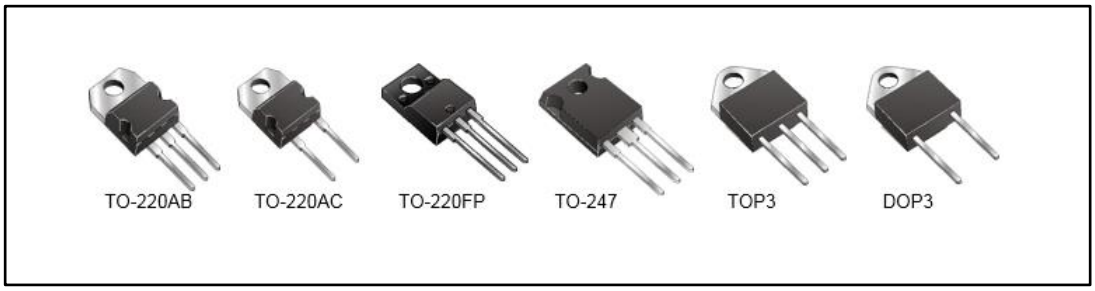
The behavior of a semiconductor device depends on the temperature of its silicon chip. This is the reason why electrical parameters are given at a specified temperature. To sustain the performance of a component and avoid failure, temperature must be limited by controlling the heat transfer between the chip and the ambient atmosphere. The aim of this application note is to provide guidelines on package mounting, handling and soldering, taking into account thermal requirements (heatsink for through-hole packages, PCB design for surface mount packages components).

Contents

1 Through-hole packages

Some through-hole packages pictures used by ST Microelectronics (non-exhaustive list) are shown here below (pictures not in scale).

Figure 1: Through-hole packages



1.1 Thermal resistance

The thermal resistance of a semiconductor assembly is the parameter which characterizes its resistance to the heat flow generated by junction during operation. If temperature exceeds the maximum junction temperature limit, the electrical performance can be curtailed and the device may be damaged.

The maximum dissipated power capability is:

$$P_{max} = \frac{T_j \max - T_a}{R_{th(j-a)}}$$

Where:

- T_j max is the maximum junction temperature of the semiconductor in degrees (°C)
- T_a is the ambient air temperature in degrees (°C)
- $R_{th(j-a)}$ is the thermal resistance between junction and ambient air in °C/W. The $R_{th(j-a)}$ takes into account all materials between the junction and ambient air.

1.1.1 Product without external heatsink

Depending on the power dissipated in the component, two types of assembly are possible:

- In the air without external heatsink
- With heatsink

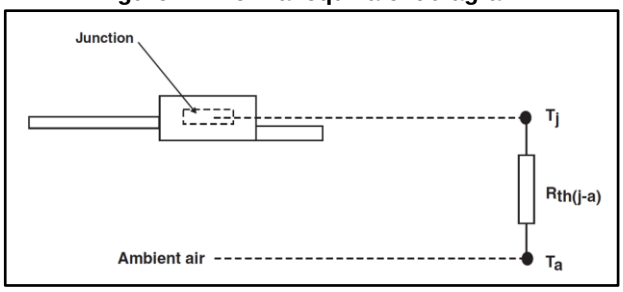
Below figure shows the thermal equivalent diagram for a diode without external heatsink. The given parameters are the following:

- T_a: ambient air temperature where the diode is located
- $R_{th(j-a)}$: thermal resistance between junction and ambient air given in the datasheet
- P: dissipated power in the diode depending on the load current

The following equation defines the junction temperature depending on these parameters

$$T_j = PxR_{th(j-a)} + T_a$$

Figure 2: Thermal equivalent diagram



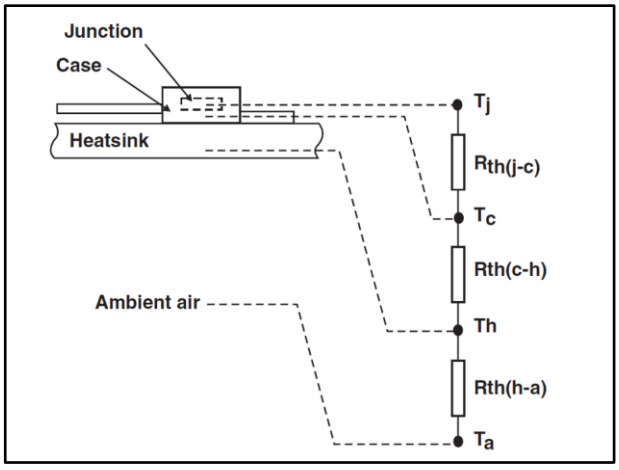
1.1.2 Product with external heatsink

If the T_j temperature is higher than the maximum junction temperature specified in the datasheet, a heatsink has to be used.

Recommendation: this calculation has to be made in the worst case scenario, meaning with the maximum dissipated power, load and line voltage dispersions. The maximum ambient temperature must be considered around the component i.e. inside the box where the component is located.

The same approach as presented in the previous section allows a suitable heatsink to be defined. The following figure shows the thermal diagram.

Figure 3: Thermal equivalent diagram with external heatsink



The thermal resistance between the heatsink and ambient air can be calculated using the following formula: $R_{th(h-a)} = \frac{T_j - T_a}{P} - R_{th(j-c)} - R_{th(c-h)}$

Where:

- T_j is the junction temperature in °C
- P is the maximum dissipated power in W
- $R_{th(j-c)}$ is the thermal resistance between junction and case in °C/W
- $R_{th(c-h)}$ is the thermal resistance between case and heatsink in °C/W, depending on the contact case/heatsink

Table 1: "Rth(c-h) for different materials for TO-220 package" is an example of $R_{th(c-h)}$ that can be used for the calculation.

1.1.3 Choice of heatsink

The selection of a heatsink depends on several parameters: the thermal characteristics, the shape and the cost.

In some applications a flat heatsink can be sufficient. The below figure shows the $R_{th(h-a)}$ curve versus the length of a flat square heatsink for different materials and thickness. Some applications may require the use of heatsinks with an optimized shape when the thermal resistances are not known.

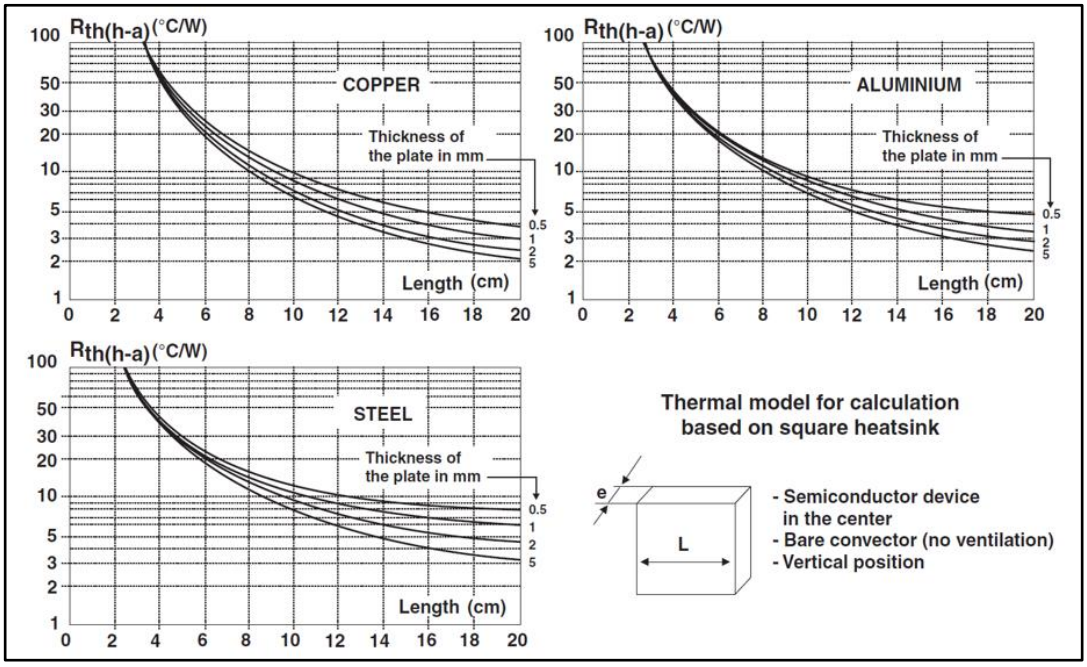
In such case the best solution is to measure the case temperature of the component in the worst case scenario and remain within the limits of the following equation:

$$T_c < T_{jmax} - P \times R_{th(j-c)}$$

Where:

- T_c is the case temperature
- T_j max is the maximum junction temperature
- P is the dissipated power in the component
- $R_{th(j-c)}$ is the thermal resistance between junction and case

Figure 4: $R_{th(h-a)}$ versus the length of a flat square heatsink



1.1.4 Forced cooling

For high-power or very high-power applications, an air-forced or liquid cooling heatsink may be required. Heatsink manufacturers provide a coefficient depending on the air or liquid flow.

In this case it is necessary to measure the case temperature in the worst case scenario and verify its compliance with the following formula:

$$T_c < T_j max - P \times R_{th(j-c)}$$

1.2 Insulating materials

We can classify them in 3 types as following:

1. **Mica insulators**
   These have been the most commonly used insulators for many years. They are defined by good insulating quality, but are rigid, which leads to a poor thermal interface and needs contact grease on each side. Because of their rigidity they can be easily broken.
2. **Ceramic insulators**
   Ceramic insulators are more expensive than the mica ones, with a lower thermal resistance. Because of their rigidity they also need contact grease. Being less fragile than mica insulators they still can break easily.
3. **Silicon pad insulators**
   These materials are not rigid and therefore do not need contact grease. They adjust themselves to the shape of the component and to the heatsink if enough pressure is applied. The problems previously explained disappear. According to manufacturers, the stability in time is much better with contact grease. Moreover the thermal resistance is higher than the combination of mica and grease.

The following table shows the thermal resistance for different TO-220 insulators and for a given pressure (F = 30 N).

Table 1: $R_{th(c-h)}$ for different materials for TO-220 package

Symbol	Contact grease	Mica + grease e = 80 µm	Mica dry e = 80 µm	Silicon insulator	Unit
$R_{th(c-h)}$	0.5	1.7	4	2.6	°C/W

The following table shows the thermal resistance for different TO-220 insulators and for a given pressure (F = 30 N).

1.3 Insulated components

The rectifier diodes manufactured by STMicroelectronics are available in insulated and non-insulated packages.

For insulated packages, insulation can be achieved in two different ways, either with a ceramic between the die pad and the heatsink of the component (TO-220 / TOP3 / ISOTOP packages), or with the rear/bottom side resin encapsulation (TO220-FP package). All insulated packages delivered by STMicroelectronics are compliant with UL1557 recognition applicable for "electrically isolated semiconductors". The added material increases the thermal resistance between the junction and the case, but the total thermal resistance (R_{thj-c}) is lower than the one when using a non-insulated component with an external insulating material. In addition, it simplifies the assembly and reduces the cost.

1.4 Handling and mounting techniques

The use of inappropriate techniques or unsuitable tools during handling and mounting can affect the long term reliability of the device, or even damage it.

1.4.1 Bending and cutting leads

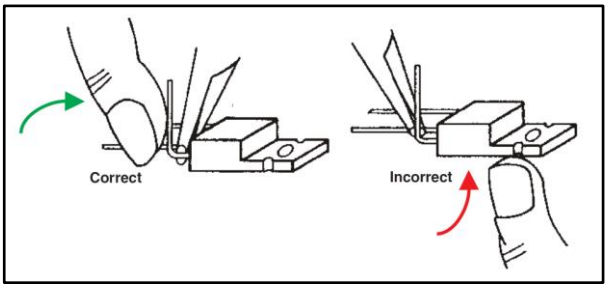
Lead bending must be done carefully. The lead must be firmly held between the plastic package and the bending point during lead operation. If the package / lead interface is

strained, the resistance to humidity may be impaired and in addition mechanical stress is inflicted on the die. This damage can affect the long term reliability of the device.

There are six basic rules to keep in mind:

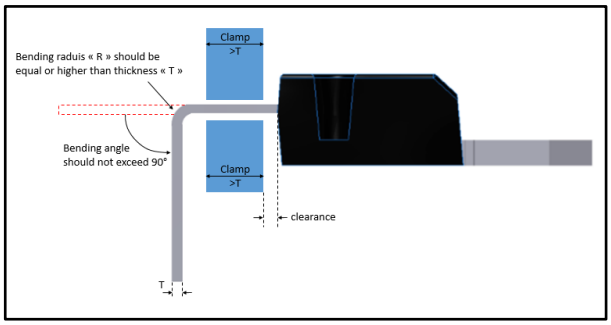
- Never apply clamping or holding force to the plastic package during the bending operation

Figure 5: Correct lead bending



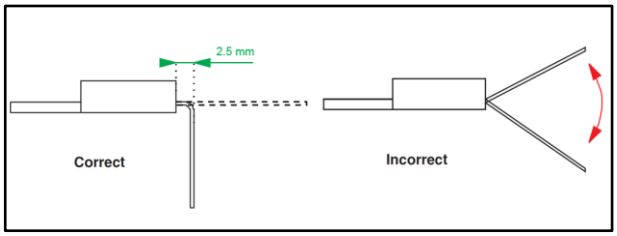
- Clamp the leads firmly between the plastic package and the bend / cut point

Figure 6: Lead bending recommendation



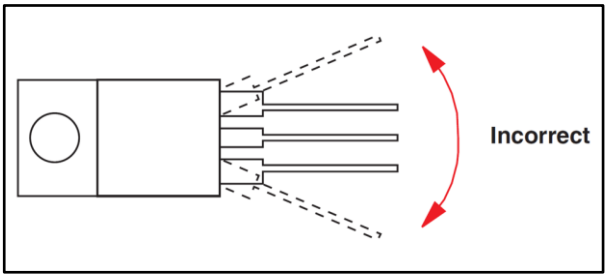
- Bend the leads at least 2.5mm away from the plastic package

Figure 7: Minimum distance between package and lead



- Never bend the leads laterally

Figure 8: Incorrect lead bending



- Never bend the leads more than 90° and never bend more than once
- Make sure that the bending / cutting tool does not damage the leads

1.4.2 Using a heatsink

Mounting surface preparation:

- The mounting surface should be flat, clean and free of burns and scratches.
- The use of a thin layer of thermal silicon grease ensures a very low contact thermal resistance between the component and the heatsink. An excessively thick layer or an excessively viscous silicon grease may have the opposite effect and cause the deformation of the tab
- The planarity of the contact surface between device and heatsink must be better than 50 µm for TO-220

Insertion:

If the heatsink is mounted on the printed circuit board, it should be attached to the component before the soldering process of the leads.

Mounting techniques:

Mounting must be done carefully. Excessive stress may induce distortion of the tab and as a consequence mechanical damage on the die.

1.4.2.1 Tab soldering

It is not recommended for through-hole packages

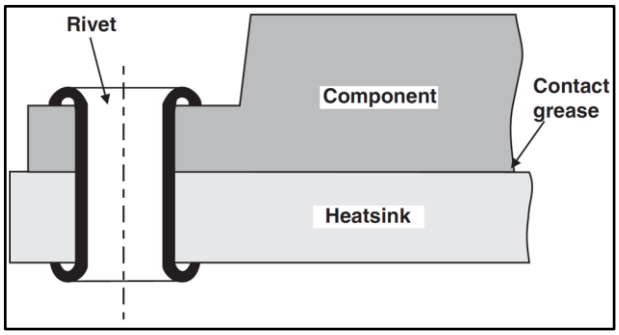
1.4.2.2 Tab attachment with rivets

Pop rivets should never be used for the following reasons:

- Any excessive expansion of the metal can lead to a distortion of the heatsink hole and induce mechanical stresses on the die.
- High crimping shock can damage the die.

Press rivets can be used with caution providing they are of a soft metal like aluminium. The crimping force must be applied slowly and carefully in order to avoid shock and deformation of the heatsink.

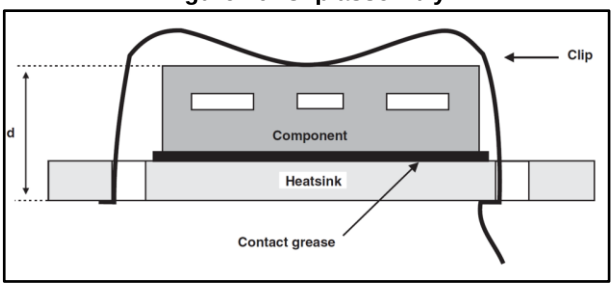
Figure 9: Assembly with rivet



1.4.2.3 Clip assembly

Care should be taken with the contact area between the plastic case and the clip: the maximum pressure allowed on plastic is 150 N/mm2. Over this value, cracks may be induced in the package. Therefore, the clips have to be round or smooth in the contact area to avoid any force concentration on the plastic body. The force applied on the component depends on the heatsink and on the component thickness. The clips must therefore be designed to take these dimensions into account.

Figure 10: Clip assembly

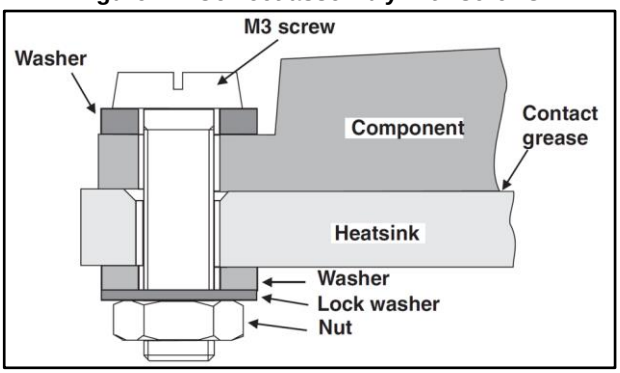


1.4.2.4 Assembly with screws

The following precautionary measures should be taken:

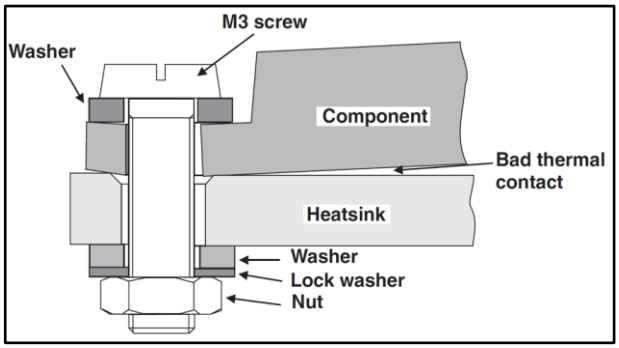
- In order to avoid tab distortion, a washer must be put between the screw head and the tab, and a compression washer must be put between the tab and the nut.

Figure 11: Correct assembly with screws



- Take care to avoid mechanical shock during screwing step
- Keep the screw straight
- Appropriate screwing torque should be used, excessive screwing torque may cause the distortion of the tab and induce bad thermal contact, and it could also generate die cracks.

Figure 12: Incorrect assembly with screws



The thermal contact resistance depends on the force generated by the torque applied on the screw:

$$F = \frac{2xTx\pi}{P+rxDx\pi}$$

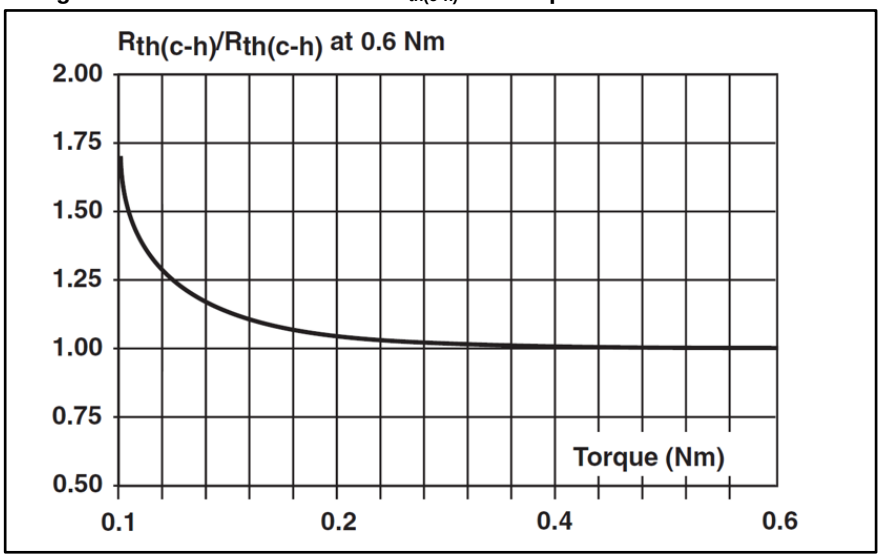
Where:

- **T:** torque applied on the screw in N.m

- **P:** pitch in m
- **D:** screw diameter in m
- **r:** rubbing factor: # 0.12 for steel-steel with grease and # 0.2 for steel-aluminum

The relative variation of the $R_{th(c-h)}$ versus the torque for M3 screw used for the TO-220 is given on *Figure 13: "Relative variation of Rth(c-h) versus pressure force for TO-220"*.

Figure 13: Relative variation of $R_{th(c-h)}$ versus pressure force for TO-220



The following table provides the recommended torque and the thermal contact resistance

Table 2: Torque values and thermal contact resistance

Package	Recommended torque (N.m)	Max torque (N.m)	Thermal contact resistance (°C/W) (typical values)
TO-220	0.55	0.7	0.5
TO-220SG		0.6	
TO-220FP		0.7	
TOP3	1.05	1.2	0.1
ISOTOP™	1.3	1.5	0.05
TO247/TO3-P/TO3-PF	0.8	1.0	0.1

1.5 Through-hole package wave soldering

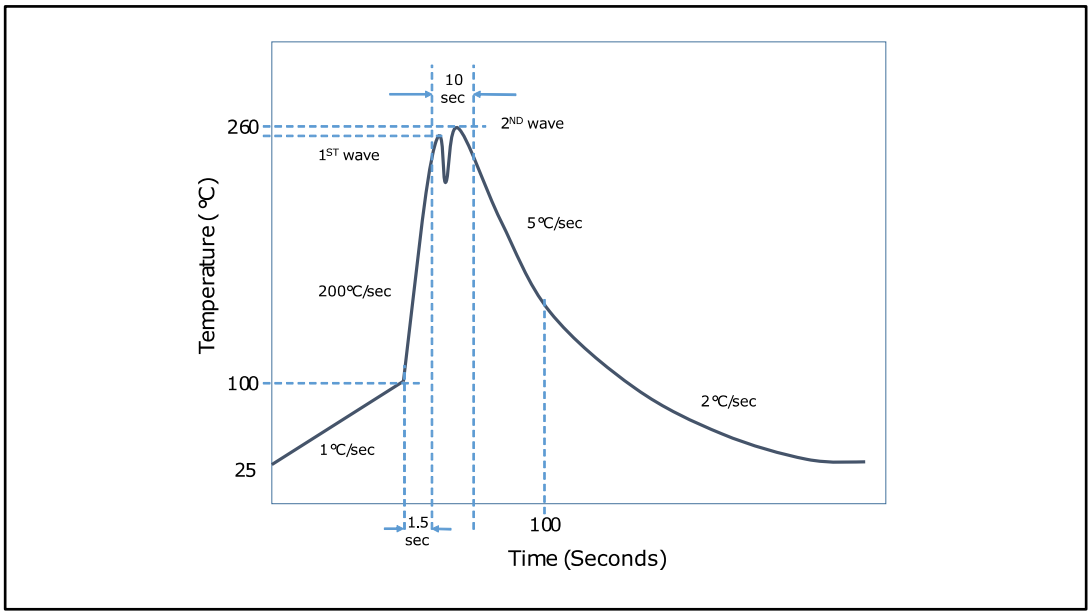
The insertion components for lead-free devices are solderable with lead-free solder pastes or alloys (Sn-Ag-Cu based alloys). The typical soldering temperature is 260 °C. They can be also soldered using SnPb based solder pastes or solder alloys. The soldering temperature is then typically around 220 °C.

Interface adherences on through-hole packages structure are qualified to sustain 3 consecutive dips of their leads in a solder pot at 260 °C (0 °C / +5 °C).

- Immersion duration: 10 seconds each
- Duration between 2 dippings : 5 minutes
- Minimum distance solder to package plastic body: according to packages, by default 1 mm

Wave soldering temperature profile recommendations are mentioned in *Figure 14: "Recommended wave soldering profile"*. These recommendations are only indicative, solder process engineers should always optimize the thermal profile for each circuit assembly based on its specific requirements.

Figure 14: Recommended wave soldering profile



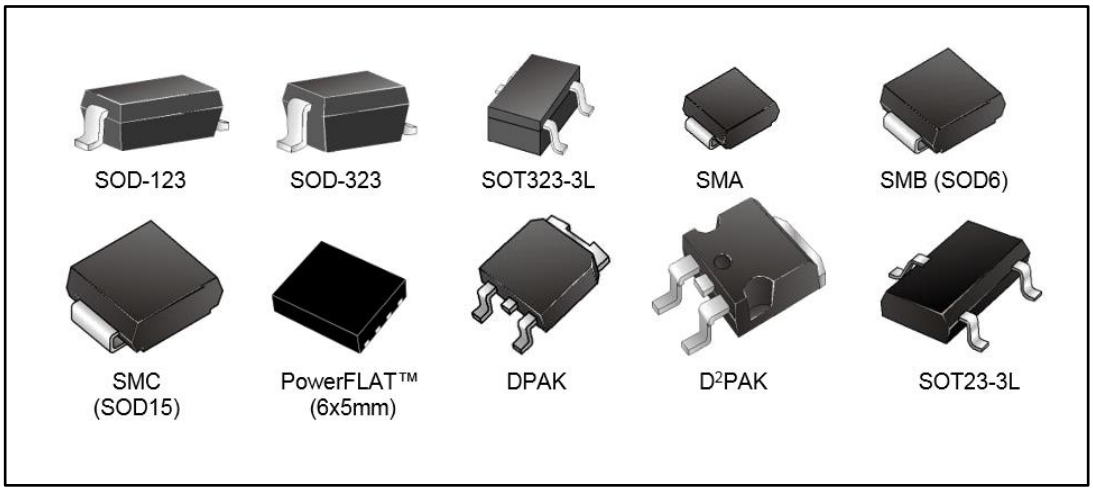
Profile feature	Pb-free system
Average ramp-up rate	~200 °C/second
Heating rate during preheat	Typ. 1-2 °C/sec., max. 4 °C/sec.
Final preheat temperature	Within 125 °C of solder temp.
Peak temperature	260 °C
Time within +0 -5 °C of actual peak	10 seconds
Ramp-down rate	5 °C/second max.

Lead-free devices are described in an internal specification. This specification is available for ST customers upon request (Title: ECOPACK Components Definition & Characteristics). Please consult it for further information.

2 Surface mount packages

Following surface mount packages are used for rectifier diodes products : POWERFLAT, DPAK, D²PAK, PSMC, SMA, SMA Flat, SMB, SMB Flat, SMC, SOD123, SOD123 Flat, SOD523, SOD128 Flat, SOT23 and SOT323, some packages pictures are shown here below (pictures not in scale).

Figure 15: Surface mount packages



2.1 Thermal characteristics

2.1.1 Thermal resistance

The thermal resistance of a semiconductor device characterizes the device capability to dissipate the heat generated by the chip during operation. This parameter allows us to calculate the junction temperature, taking into account the device environment (load current, ambient temperature, mounting conditions etc...).

For surface mount packages, the thermal resistance between junction and ambient, called $R_{th(j-a)}$, depends on the copper surface used under the tab. The following figures (from *Figure 16: "Rth(j-a) versus copper area on PCB for DPAK"* to *Figure 18: "Rth(j-a) versus copper area on PCB for SMB"*) provide the relationship between $R_{th(j-a)}$ and the copper surface under the tab for a FR4 board (35 µm copper thickness) for various surface mount packages.

Figure 16: $R_{th(j-a)}$ versus copper area on PCB for DPAK

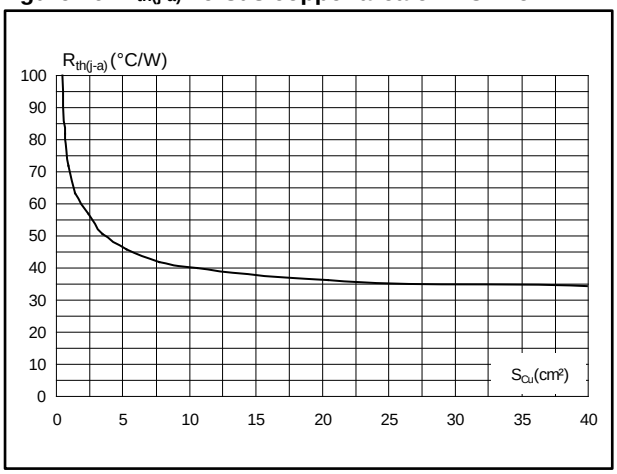


Figure 17: $R_{th(j-a)}$ versus copper area on PCB for D²PAK

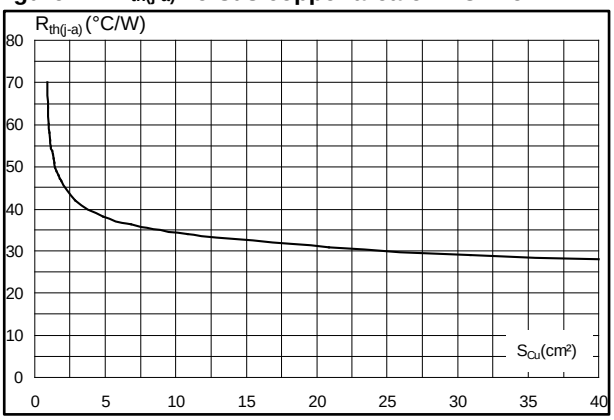
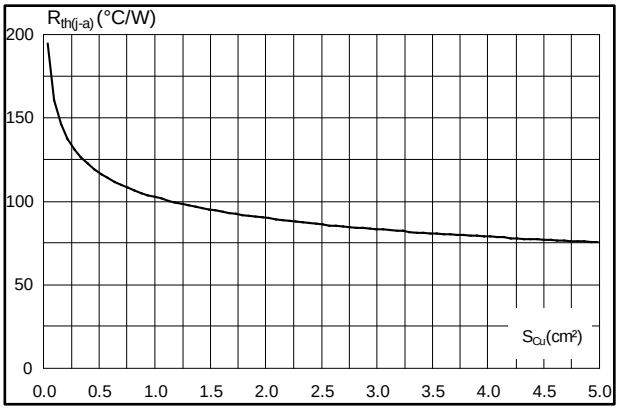


Figure 18: $R_{th(j-a)}$ versus copper area on PCB for SMB



2.1.2 Thermal impedance

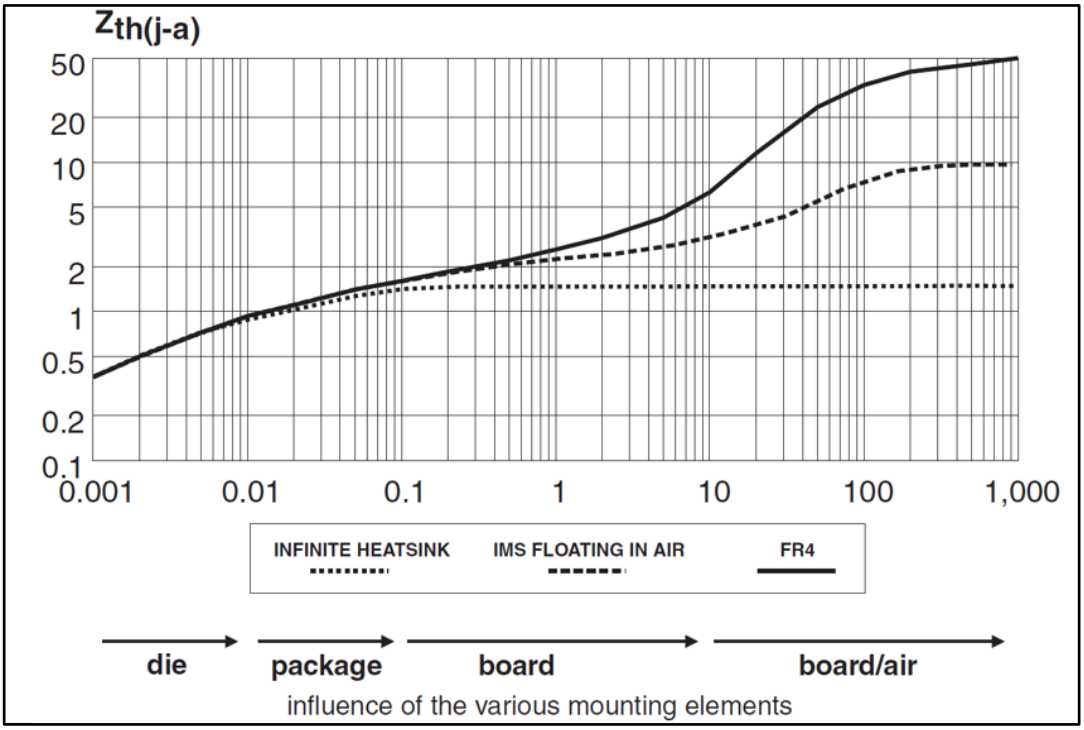
When dealing with short duration pulses, the thermal impedance must be taken into consideration to calculate the junction temperature. Depending on the time scale, the following elements are thermally prevalent:

- t_p < 10 ms: die influence
- t_p < 0.1 s: package influence
- t_p < 10 s: PCB influence

- above 10s : thermal exchange board-air (example: with / without force cooling)

The next figure shows the Z_{th} / R_{th} ratio for surface mount packages

Figure 19: Relative variation of thermal impedance junction to ambient versus pulse duration typical $Z_{th(j-a)}$ for DPAK and D²PAK

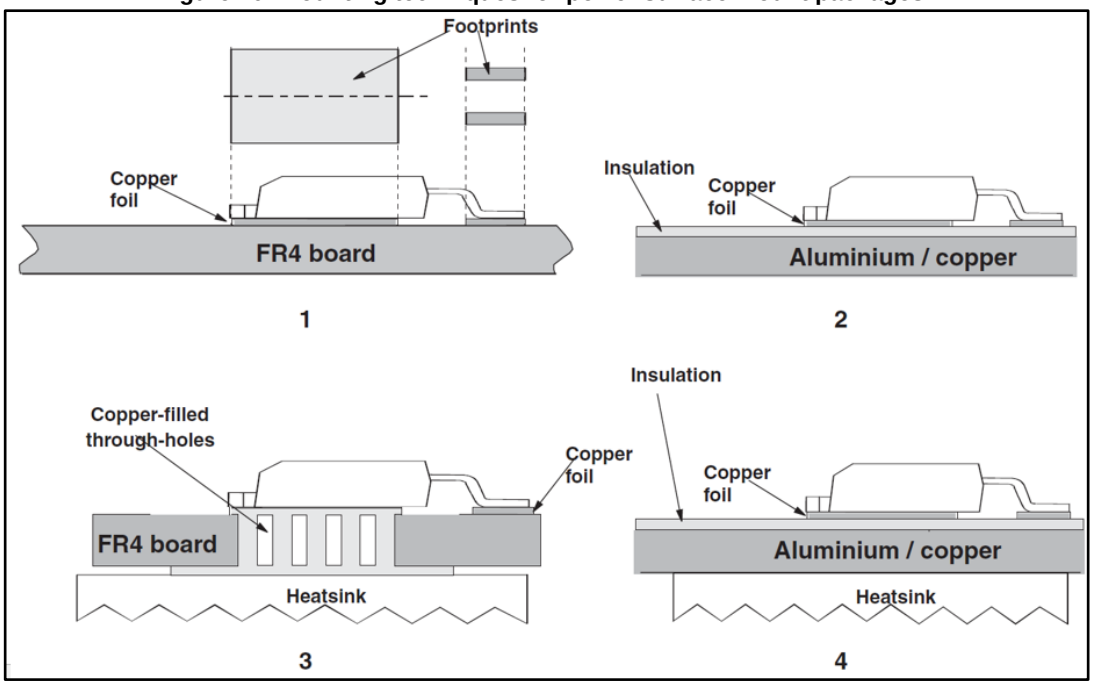


2.1.3 Mounting techniques and $R_{th(j-a)}$

$R_{th(j-a)}$ varies based on the printed circuit board technology employed. Several technologies can be used depending on the performance required in the design. Four techniques are commonly used:

1. FR4 - copper
2. IMS (insulated metal substrate)
3. FR4 board with copper-filled through-holes + heatsink
4. IMS + heatsink

Figure 20: Mounting techniques for power surface mount packages



As the FR4 board is commonly used in surface mounting techniques, there are several ways of overcoming its low thermal performance:

- The use of large heat spreader areas (heatsink) at the copper layer of the PCB
- The use of copper-filled through-holes in addition to an external heatsink for even better thermal management

However, due to its power dissipation limitation, using the FR4 board with these techniques is only advisable for currents up to 8 A max.

Another technology available today is IMS - Insulated Metal Substrate. This offers greatly enhanced thermal characteristics for surface mount components. IMS consists of three different layers:

1. Base material which is available as an aluminum or copper plate
2. Thermal conductive dielectric layer
3. Copper foil, which can be etched as a circuit layer

If a higher power must be dissipated, an external heatsink can be applied, which allows a significant reduction of $R_{th(j-a)}$.

The designer should carefully examine the appropriate mounting method to be used based on the power dissipation requirements. The board type will influence the thermal performance of the system.

Table 3: "Rth(j-a) for DPAK" is an example of the $R_{th(j-a)}$ depending on the mounting techniques for DPAK and D²PAK.

Table 3: $R_{th(j-a)}$ for DPAK

Mounting method	$R_{th(j-a)}$	
	DPAK	D²PAK
FR4	70 °C/W	50 °C/W
FR4 with 10 cm² heatsink on board	40 °C/W	35 °C/W
FR4 with copper filled holes and external heatsink	13 °C/W	12 °C/W
IMS (40 cm²) floating in air	9 °C/W	8 °C/W
IMS with external heatsink	4.5 °C/W	3.5 °C/W

2.2 Reflow soldering information

The surface mount assembly is a 5-step process:

1. Solder paste printing
2. Component placement on the board
3. Reflow soldering
4. Cleaning (optional)
5. Final solder joint inspection

Recommendations for these processes are proposed here below.

Proposed footprint and stencil openings for each surface mount packages used by Rectifier products (POWERFLAT5x6 and 3.3x3.3, DPAK, D²PAK, D³PAK, PSMC, SMA, SMA Flat, SMB, SMB Flat, SMC, SOD123, SOD123 Flat, SOD523, SOD128 Flat, SOT23, SOT323, STMite, STMite flat, SOD323 Flat, as well as Wafer level Chip Scale Packages) are included at the end of the document.

2.3 Printed circuit board recommendations

2.3.1 PCB solderable metallization

There are two common plated solderable metallization finishes which are used for PCB surface mount devices. In either case, it is required that the plating is uniform, conforming, and free of impurities to ensure consistent solderability.

The first metallization finish consists of an organic solderable preservative (OSP) coating over the copper pad. The organic coating assists in reducing oxidation to preserve the copper metallization for soldering.

The second metallization is NiAu (electroless nickel plating over the copper pad, followed by immersion gold). The thickness of the nickel layer is determined by the allowable internal material stresses and the temperature excursions the board will be subjected to throughout its lifetime. For the immersion gold process, the gold thickness is self-limited, but should be thick enough to prevent Ni oxidation (typically above 0.05 µm) and thin enough to represent more than 5% of the overall solder volume. Having excessive gold in the solder joint can create gold embitterment, which may affect the reliability of the solder joint.

2.3.2 PCB design

We recommend closed vias in the design, in order to control the amount of solder paste during screen printing.

The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

2.3.3 PCB pad design

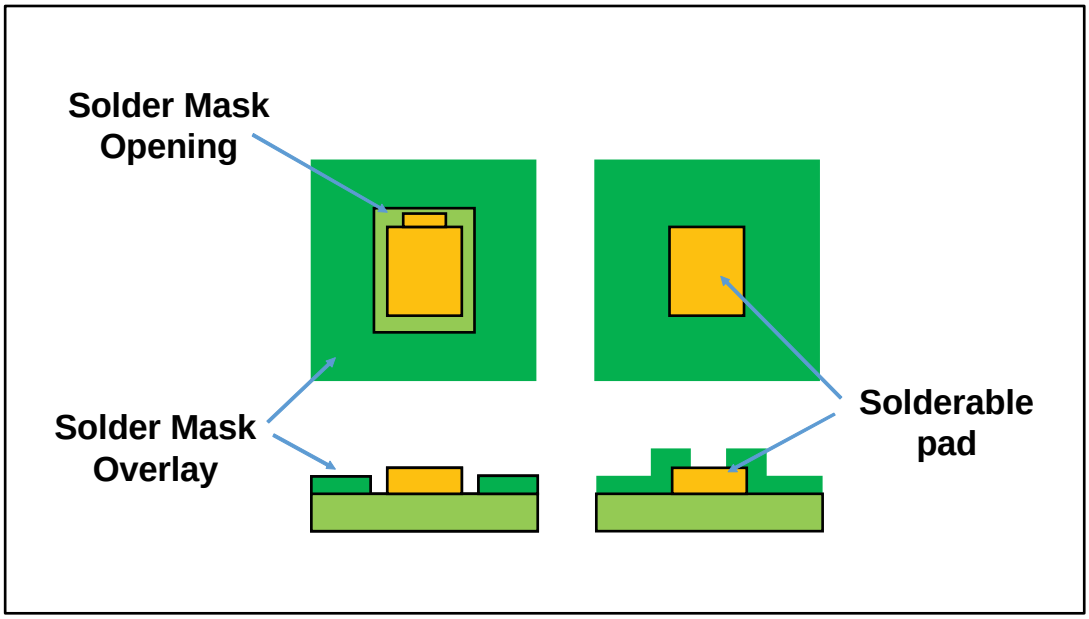
There are 2 different types of PCB pad configurations commonly used for surface mount packages:

- Non-solder mask defined (NSMD)
- Solder mask defined (SMD)

As their title indicates, NSMD contact pads have the solder mask pulled away from the solderable metallization, while the SMD pads have the solder mask over the edge of the metallization, as shown in *Figure 21: "Comparison between SMD and NSMD pads"*.

With SMD pads, the solder mask restricts the flow of solder paste to the top of the metallization, preventing the solder from flowing along the sides of the metal pad. This is different from the NSMD pads, where the solder will flow around both the top and the sides of the metallization.

Figure 21: Comparison between SMD and NSMD pads



Both configurations can be used.

Typically, NSMD pads are preferred since defining the location and size of the copper pad is easier to control than the solder mask. This is based on the fact that the copper etching process is capable of tighter tolerance than the solder masking process.

2.4 Solder paste printing

2.4.1 Solder type

It is recommended the use of solder paste with fine particles (type 3 or type 4, meaning particle dimensions from 20 to 45 µm), as well as solder paste containing halide-free flux ROL0 in accordance with ANSI/J-STD-004. For lead-free solders Sn-Ag-Cu, alloy SnAg1.0Cu0.5 is preferred, but any SnAgCu alloys with 1 to 4% Ag and <1% Cu should be suitable.

2.4.2 Solder screening on the PCB

Stencil screening the solder on the PCB is commonly used in the industry. Recommended stencil thicknesses are 0.075 mm to 0.127 mm (0.003 inch to 0.005 inch) and the sidewalls of the stencil openings should be tapered to approximately 5° to ease the release of the paste when the stencil is removed from the PCB.

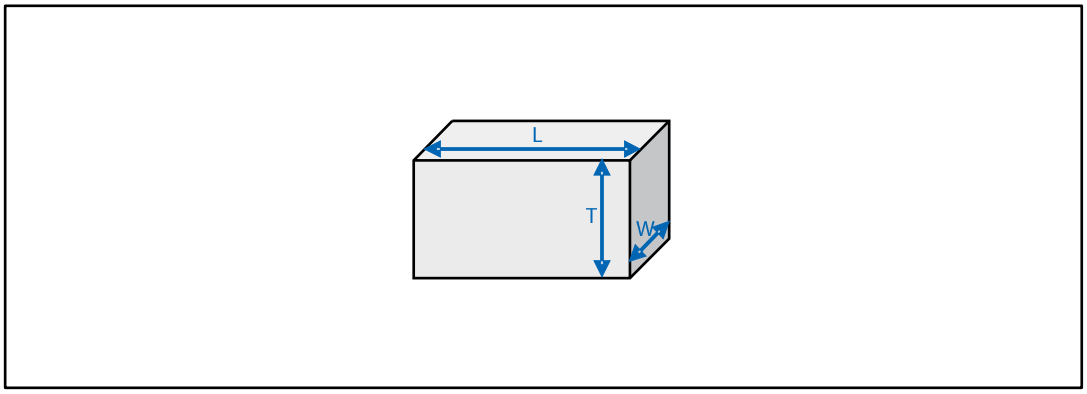
For a typical lead PCB terminal, a stencil opening to footprint ratio of 90% is recommended. For central exposed pad, it may vary depending on package dimensions, but solder coverage should vary from 50 to 80%.

For big packages (DPAK, D²PAK, POWERFLAT), the stencil opening under the package's exposed pad must be divided into smaller openings. This reduces the risk of solder voiding, and allows the solder joint for the leads to be at the same height as the exposed pad.

To ensure a safe and repeatable stencil printing process, some generic design rules for stencil design should be followed, as described here below.

- General design rule
  - Stencil thickness (T) = 75 ~ 125 µm
  - Aspect ratio = $\frac{W}{T} \geq 1.5$
  - Aspect area = $\frac{L \times W}{2T(L+W)} \geq 0.66$

Figure 22: Stencil opening dimensions



2.5 Component placement

Manual placement is not recommended.

We recommend to use pick-and-place equipment with the standard tolerance of +/- 0.05 mm or better. The package will tend to center itself and correct for slight placement errors during the reflow process due to surface tension of the solder joint.

Adequate placement force should be used (3.5 N for example for most of packages). Too strong a placement force can lead to squeezed-out solder paste and cause solder joint to short. Too low a placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or non-centered packages.

2.6 Reflow profile recommendation

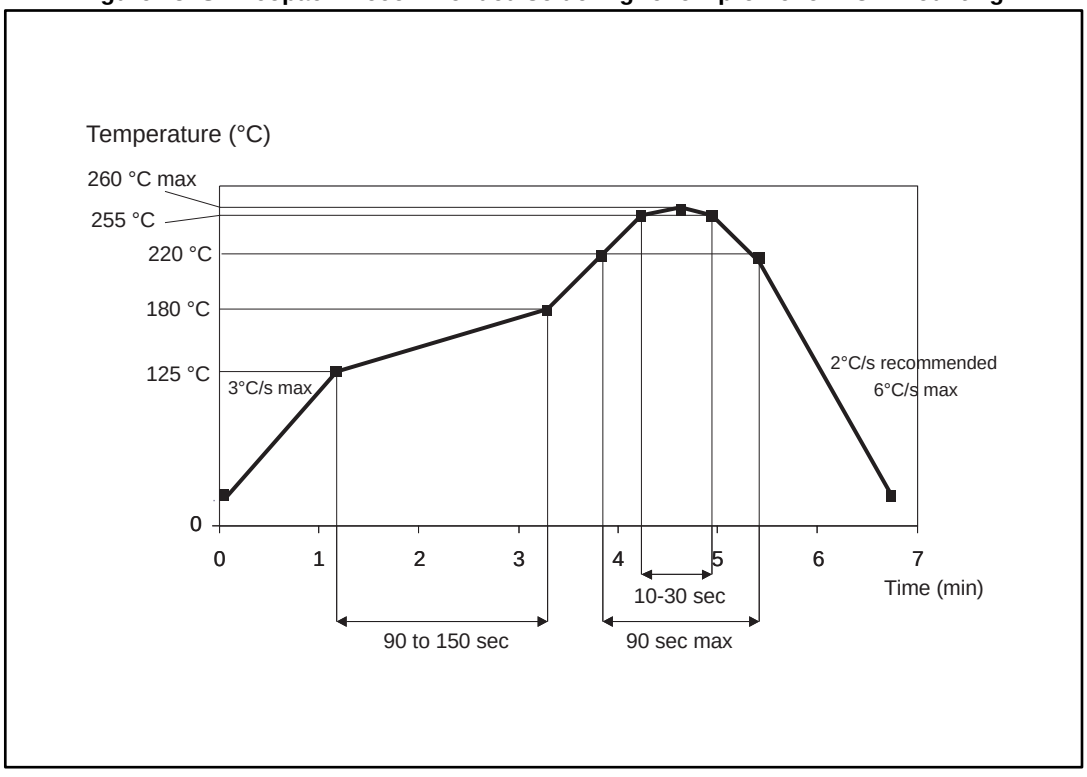
The soldering process causes significant thermal stress to a semiconductor component. This has to be minimized to assure a reliable and extended lifetime of the device.

All packages used by rectifier products (POWERFLAT5x6 and 3.3x3.3, DPAK, D²PAK, D3PAK, PSMC, SMA, SMA Flat, SMB, SMB Flat, SMC, SOD123, SOD123 Flat, SOD523, SOD128 Flat, SOT23, SOT323, STMite, STMite flat, SOD323 Flat, as well as wafer level chip scale packages) are following IPC/JEDEC J-STD-020E requirements, and thus can be exposed to a maximum temperature of 260 °C for 10 seconds (except for packages with body thickness > 2.5mm, like D²PAK and D3PAK for which peak body temperature should be 245 °C). Overheating during the reflow soldering process may damage the device, therefore any solder temperature profile should be within these limits. As reflow techniques are most common in surface mounting, typical heating profiles for lead-free solder (ST Ecopack®) are given in the following figure for small packages, either for mounting on an FR4 or on metal-backed boards (IMS). Please refer to the IPC / JEDEC J-STD-020E standard for further information about “small” and “large” component definitions.

The soldering profile defined in the JEDEC J-STD-020E standard are used for reliability assessment and typically describe the warmest profiles used for component mounting, not the necessary temperatures to achieve good soldering.

Wave soldering is not advisable for SMD power packages (and thus for PowerFLAT) because it is almost impossible to contact the whole package slug during the process.

Figure 23: ST Ecopack® recommended soldering reflow profile for PCB mounting



For each individual board, the appropriate heat profile has to be adjusted experimentally. The current proposal is just a starting point. In every case, the following precautions have to be considered:

- Always preheat the device. The purpose of this step is to minimize the rate of temperature rise to less than 3 °C per second (recommended 2 °C/s) in order to minimize the thermal shock on the component.
- Dry out section, after preheating, to ensure that the solder paste is fully dried before starting the reflow step. Also, this step allows the temperature gradient on the board to be evened out.
- Peak temperature should be at least 30 °C higher than the melting point of the solder alloy chosen to ensure reflow quality. In any case the peak temperature should not exceed 260 °C.

Lead-free devices are described in an internal specification defining:

- Their characteristics: lead-free connection coating, solderability and identification features
- Their reliability, such as soldering resistance, reliability, whisker risk prevention

This specification is available for ST customers upon request (title: ECOPACK components definition and characteristics). Please consult this specification for further reflow and wave soldering information.

Voids represent a difficult reliability problem for large surface mount devices. Voids under the package result in poor thermal contact and the high thermal resistance can lead to component failure.

Coplanarity between the substrate and the package can be easily verified. The quality of the solder joints is very important for two reasons:

1. Poor quality solder joints directly result in poor reliability
2. Solder thickness affects the thermal resistance significantly

Thus, this parameter should be kept under control in order to obtain efficient thermal and reliable solder joints.

2.7 Footprints and stencil opening recommendations

The recommended footprints and stencil opening designs for following packages are listed: POWERFLAT5x6 and 3.3x3.3, DPAK, D²PAK, D³PAK, PSMC, SMA, SMA Flat, SMB, SMB Flat, SMC, SOD123, SOD123 Flat, SOD523, SOD128 Flat, SOT23, SOT323, STMite, STMite flat, SOD323 Flat, as well as wafer level chip scale packages.

In the following figures stencil opening dimensions are shown as blue lines.

Figure 24: DPAK footprint (mm)

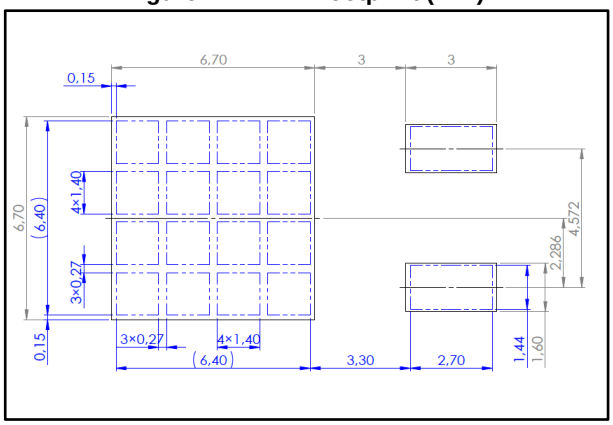


Figure 25: D²PAK footprint (mm)

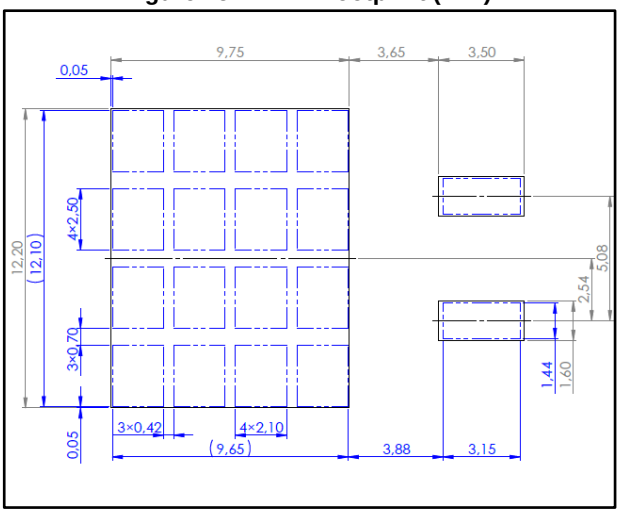


Figure 26: POWERFLAT 5x6 single pad (mm)

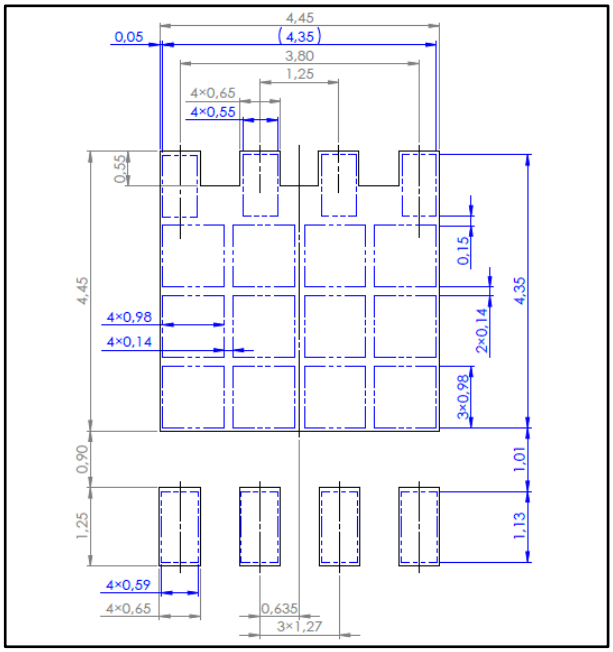


Figure 27: POWERFLAT 5x6 high voltage (mm)

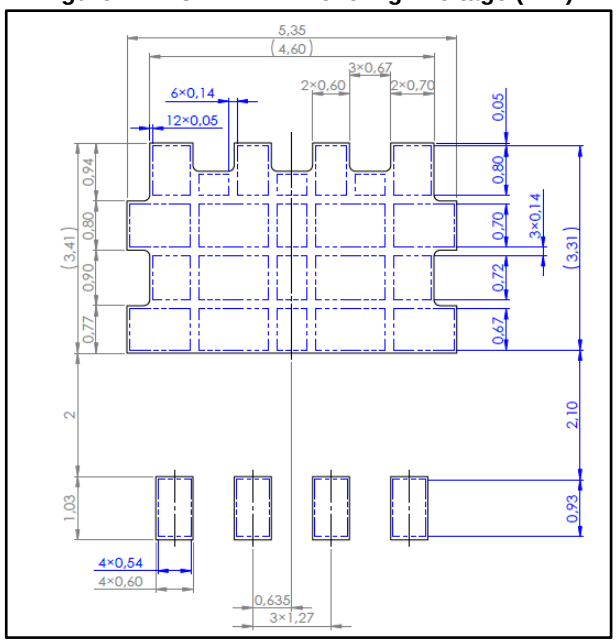


Figure 28: POWERFLAT 5x6 dual pad (mm)

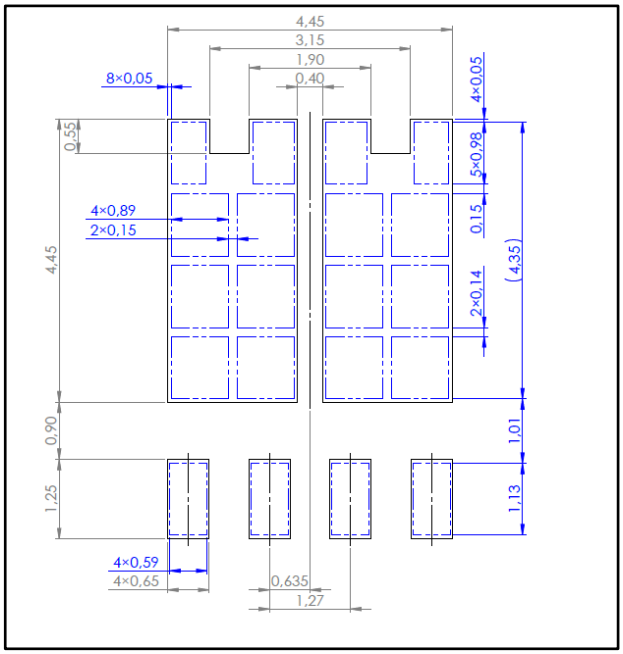


Figure 29: POWERLAT 3.3x3.3 high voltage and standard footprint and stencil opening (mm)

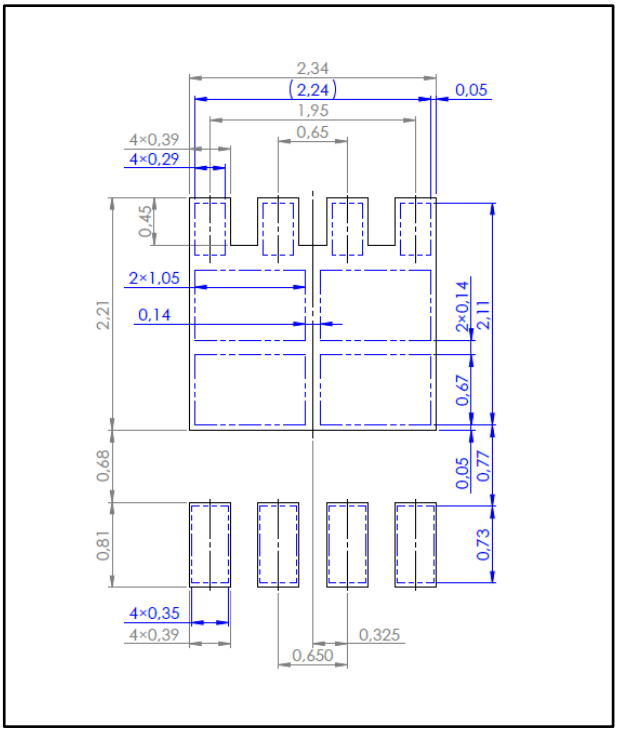


Figure 30: D3PAK footprint and stencil opening (mm)

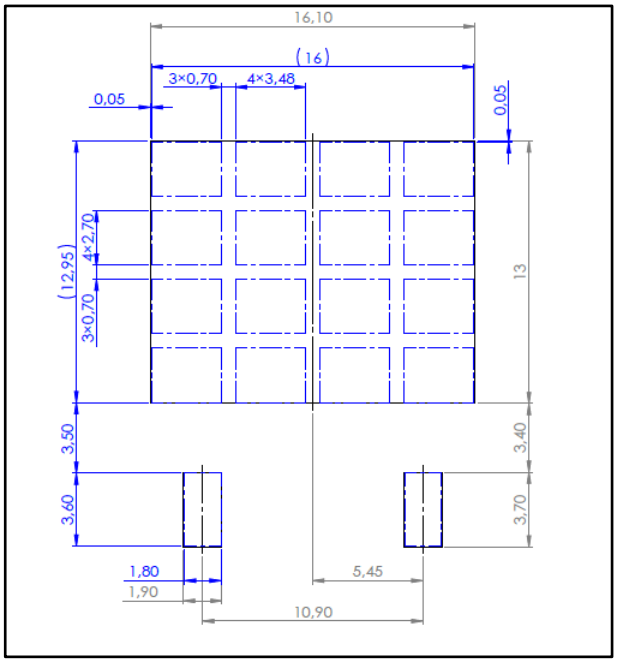


Figure 31: SOD123 footprint and stencil opening (mm)

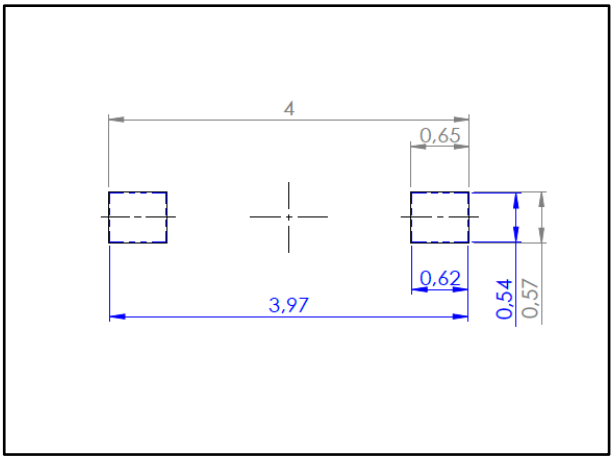


Figure 32: SOD323 footprint and stencil opening (mm)

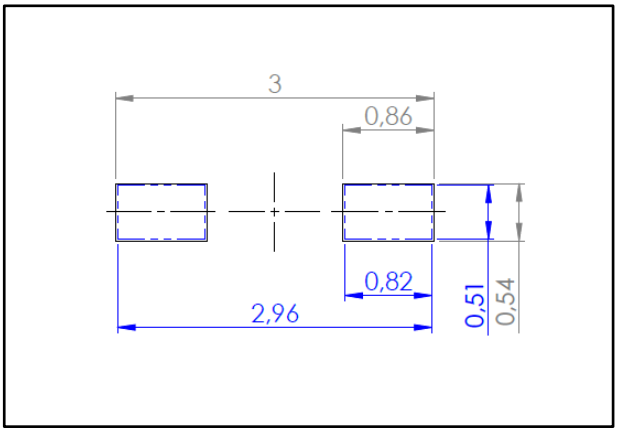


Figure 33: SOD523 footprint and stencil opening (mm)

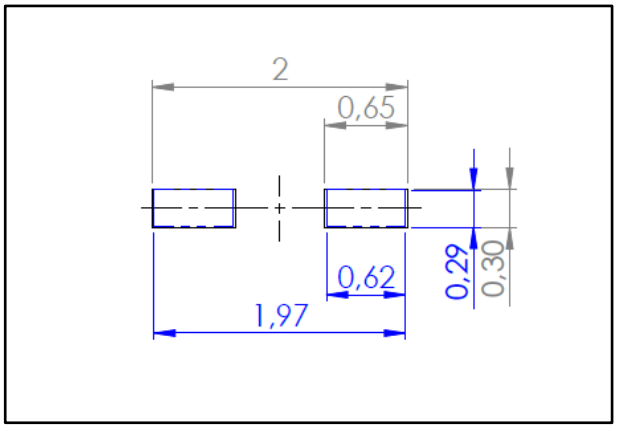


Figure 34: SOT23-3L footprint and stencil opening (mm)

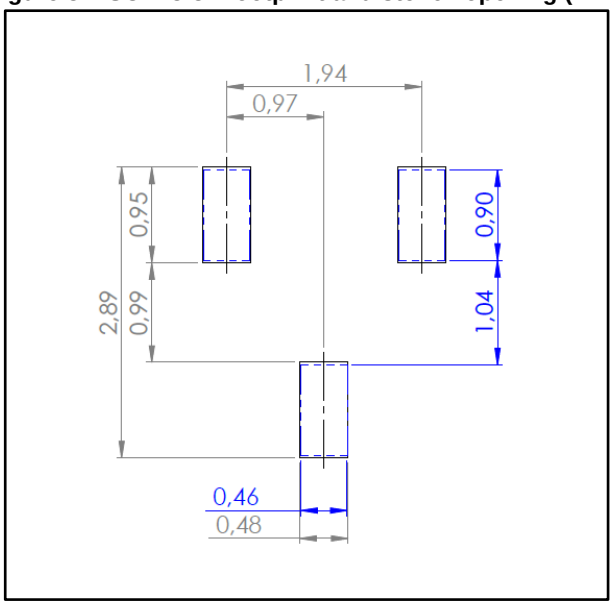


Figure 35: SOT323 footprint and stencil opening (mm)

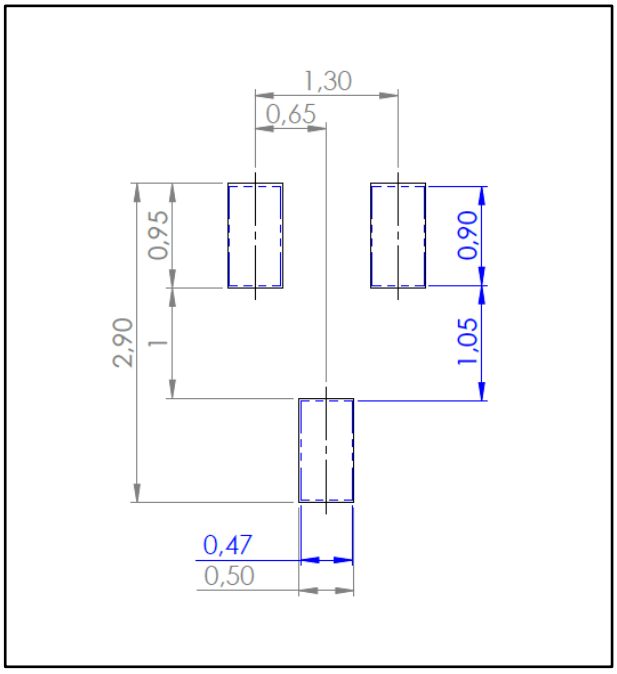


Figure 36: SOD123 Flat footprint and stencil opening (mm)

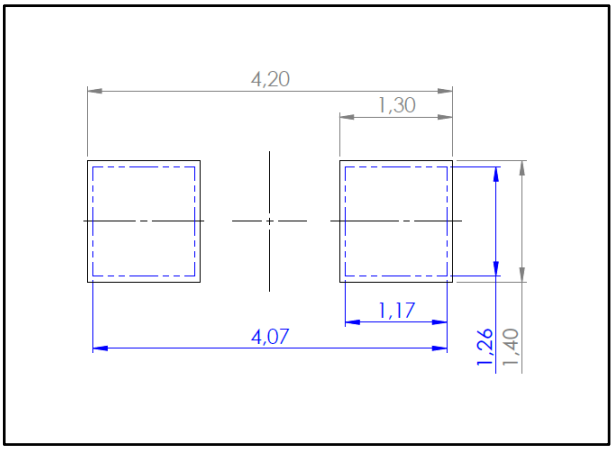


Figure 37: SOD128 footprint and stencil opening (mm)

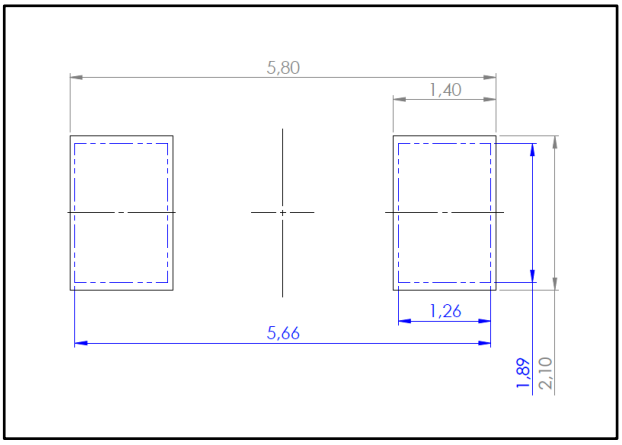


Figure 38: SMA footprint and stencil opening (mm)

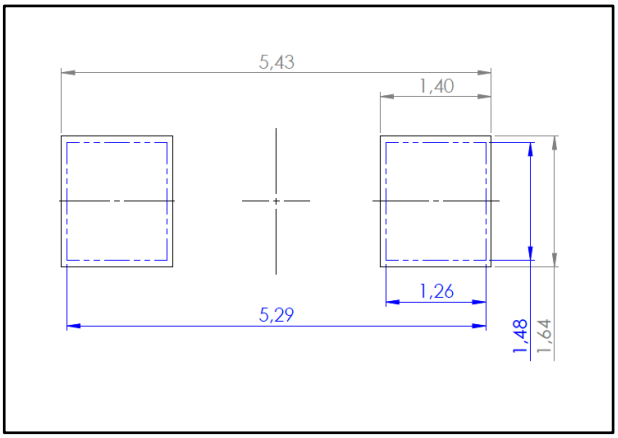


Figure 39: SMB footprint and stencil opening (mm)

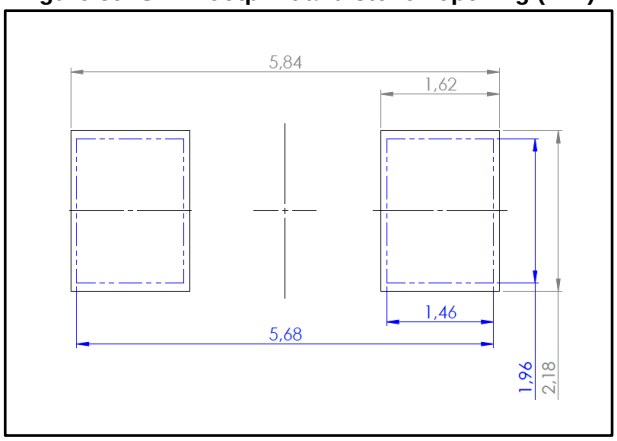


Figure 40: SMA Flat footprint and stencil opening (mm)

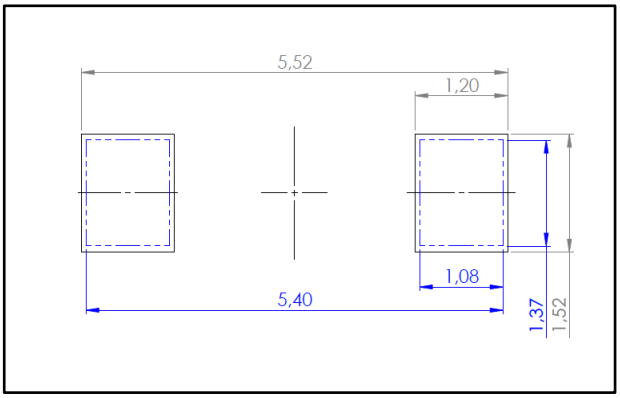


Figure 41: SMB Flat footprint and stencil opening (mm)

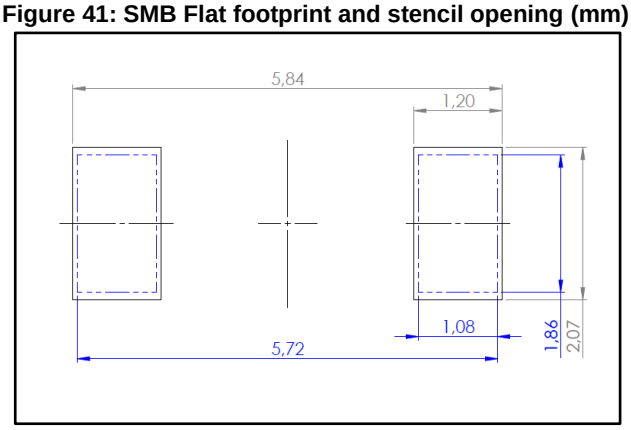


Figure 42: SMC footprint and stencil opening (mm)

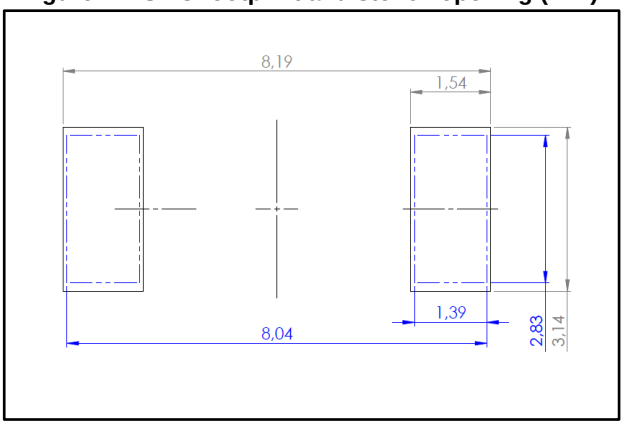


Figure 43: PSMC footprint and stencil opening (mm)

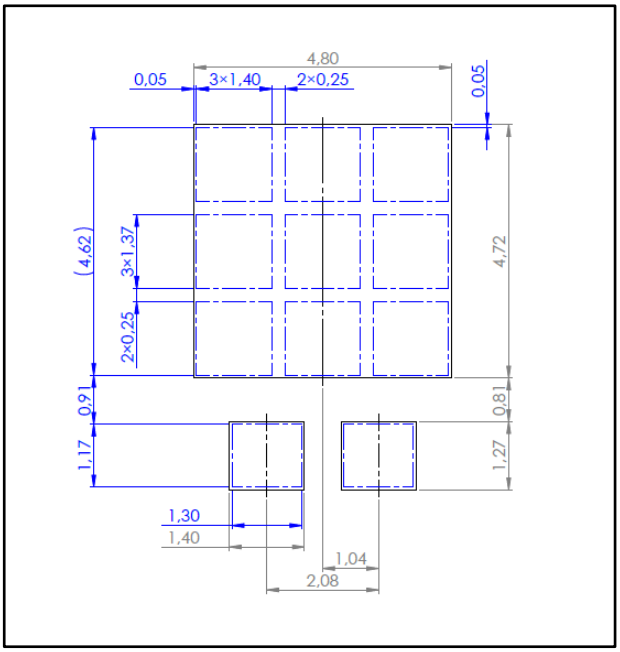


Figure 44: DO-216AA footprint and stencil opening (mm)

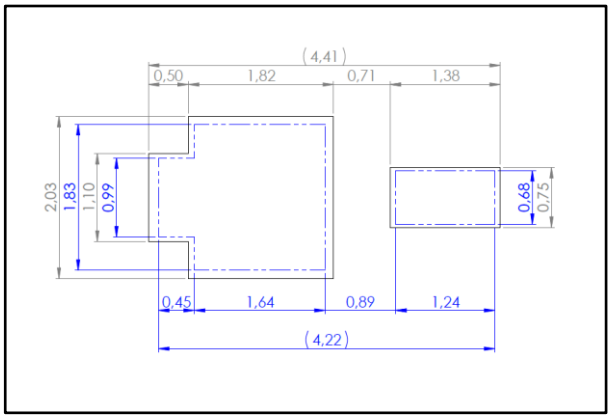


Figure 45: STMite FLAT footprint and stencil opening (mm)

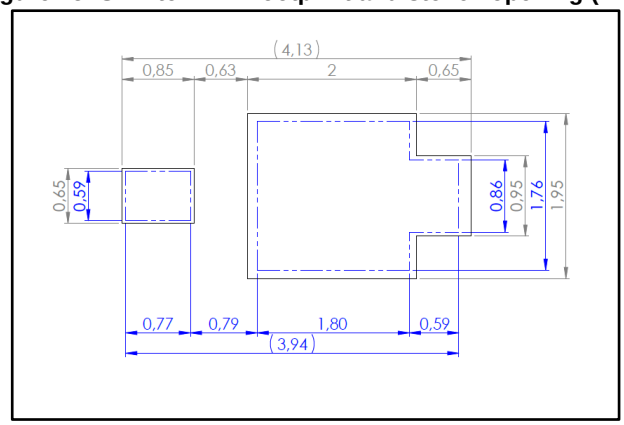


Figure 46: SOD323 Flat footprint and stencil opening (mm)

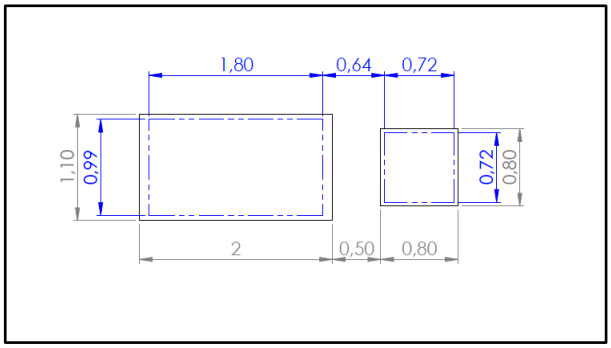


Figure 47: BAT30F3 footprint and stencil opening (mm)

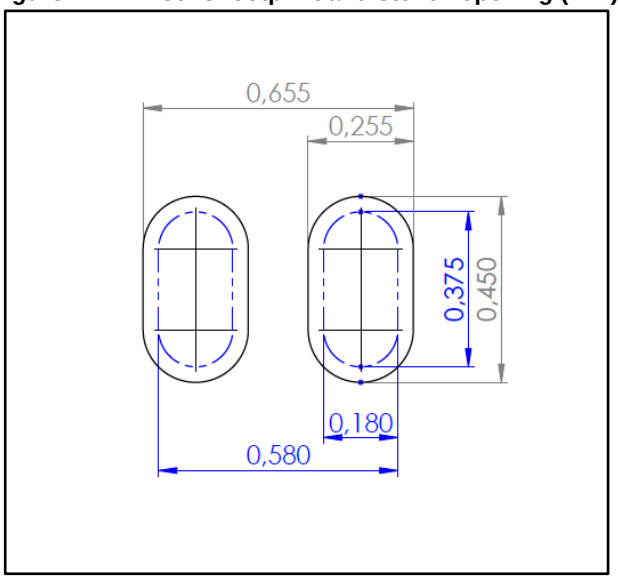
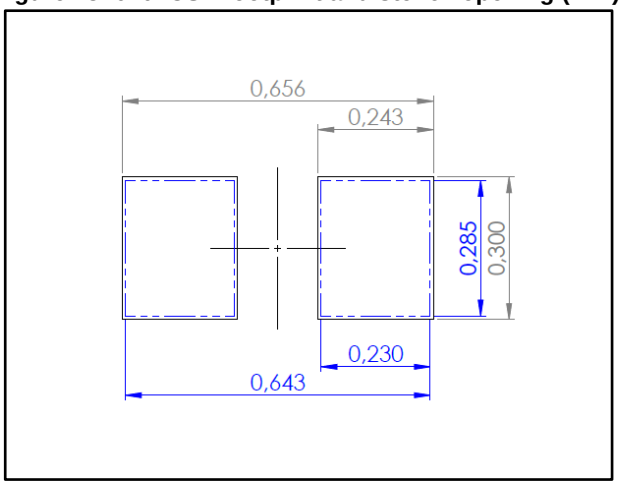


Figure 48: 0201CSP footprint and stencil opening (mm)



3 Conclusion

This application note provides mounting and soldering requirement for through-hole and surface mount devices. A correct mounting and soldering process provides an additional guarantee of good thermal performance without affecting the common reliability performance.

4 Revision history

Table 4: Document revision history

Date	Revision	Changes
09-Nov-2017	1	Initial release.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.