



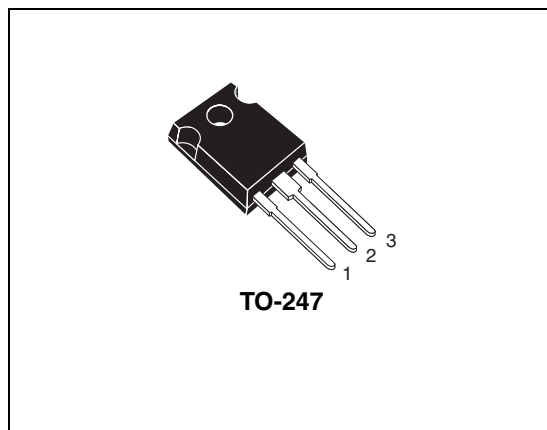
# STW54NM65ND

N-channel 650 V, 0.055  $\Omega$  49 A TO-247  
FDmesh™ II Power MOSFET (with fast diode)

## Features

Order code	V <sub>DSS</sub> (@T <sub>jmax</sub> )	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STW54NM65ND	710 V	< 0.065 $\Omega$	49 A

- The worldwide best R<sub>DS(on)</sub> \* area amongst the fast recovery diode devices
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance
- Extremely high dv/dt and avalanche capabilities



## Application

Switching applications

## Description

The device is an N-channel FDmesh™ II Power MOSFET that belongs to the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a new vertical structure to the company's strip layout and associates all advantages of reduced on-resistance and fast switching with an intrinsic fast-recovery body diode. It is therefore strongly recommended for bridge topologies, in particular ZVS phase-shift converters.

Figure 1. Internal schematic diagram

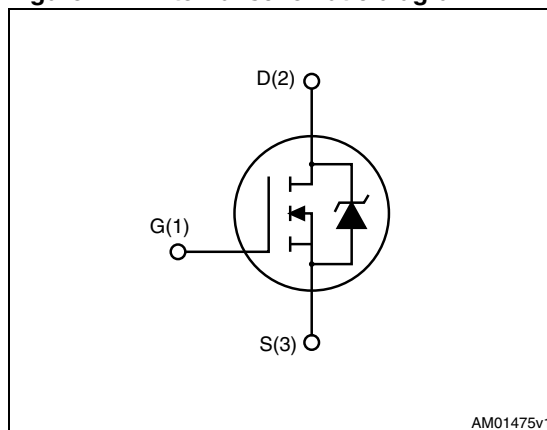


Table 1. Device summary

Order code	Marking	Package	Packaging
STW54NM65ND	54NM65ND	TO-247	Tube

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	650	V
$V_{GS}$	Gate- source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	49	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	31	A
$I_{DM}^{(1)}$	Drain current (pulsed)	196	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	350	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	40	V/ns
$T_{stg}$	Storage temperature	- 55 to 150	$^{\circ}\text{C}$
$T_j$	Max. operating junction temperature	150	$^{\circ}\text{C}$

1. Pulse width limited by safe operating area

2.  $I_{SD} \leq 49\text{ A}$ ,  $di/dt \leq 600\text{ A}/\mu\text{s}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.36	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	50	$^{\circ}\text{C}/\text{W}$
$T_I$	Maximum lead temperature for soldering purpose	300	$^{\circ}\text{C}$

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AS}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ max)	15	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^{\circ}\text{C}$ , $I_D = I_{AS}$ , $V_{DD} = 50\text{ V}$ )	850	mJ

## 2 Electrical characteristics

(T<sub>CASE</sub> = 25 °C unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0	650			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max rating V <sub>DS</sub> = Max rating, @ 125 °C			10 100	μA μA
I <sub>GSS</sub>	Gate-body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20 V			100	nA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	3	4	5	V
R <sub>DS(on)</sub>	Static drain-source on resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 24.5 A		0.055	0.065	Ω

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input capacitance Output capacitance Reverse transfer capacitance	V <sub>DS</sub> = 50 V, f = 1 MHz, V <sub>GS</sub> = 0	-	6200 218 10	-	pF pF pF
C <sub>oss eq.</sub> <sup>(1)</sup>	Output equivalent capacitance	V <sub>DS</sub> =0 to 200 V V <sub>GS</sub> =0	-	850	-	pF
Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	Total gate charge Gate-source charge Gate-drain charge	V <sub>DD</sub> = 520 V, I <sub>D</sub> = 49 A, V <sub>GS</sub> = 10 V, (see <a href="#">Figure 14</a> )	-	188 32 100	-	nC nC nC
t <sub>c</sub> t <sub>r</sub> t <sub>d(off)</sub> t <sub>f</sub>	Crossing time Rise time Turn-off delay time Fall time	V <sub>DD</sub> = 520 V, I <sub>D</sub> = 49 A, R <sub>G</sub> = 4.7 Ω, V <sub>GS</sub> = 10 V (see <a href="#">Figure 17</a> ), (see <a href="#">Figure 13</a> )	-	33 59 152 98	-	ns ns ns ns
R <sub>g</sub>	Gate input resistance	f=1 MHz gate DC bias=0 Test signal level = 20 mV open drain	-	1.9	-	Ω

1. C<sub>oss eq.</sub> is defined as a constant equivalent capacitance giving the same charging time as C<sub>oss</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DS</sub>.

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current		-		49	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		196	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 49\text{ A}$ , $V_{GS} = 0$	-		1.3	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 49\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$	-	212		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60\text{ V}$	-	2		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	<a href="#">Figure 15</a>	-	19		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 49\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$	-	296		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$	-	4		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	<a href="#">Figure 15</a>	-	28		A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

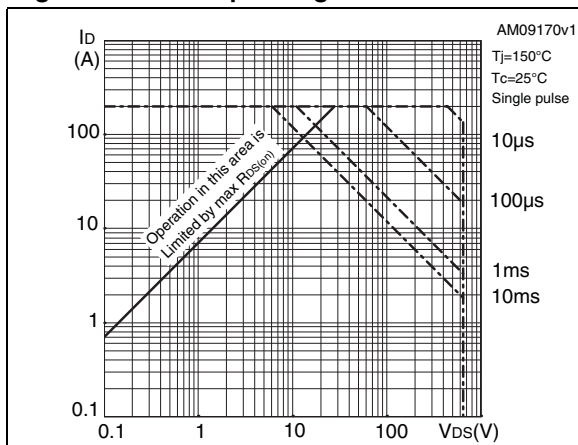


Figure 3. Thermal impedance

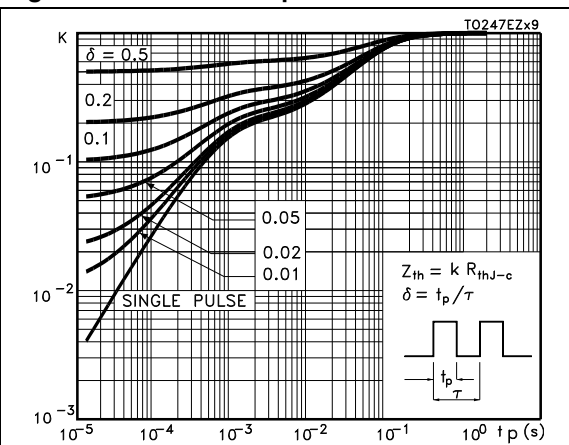


Figure 4. Output characteristics

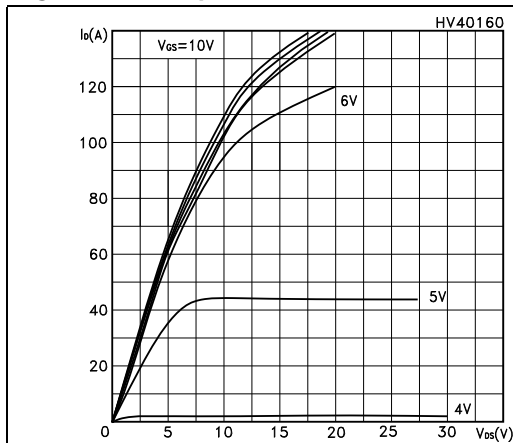


Figure 5. Transfer characteristics

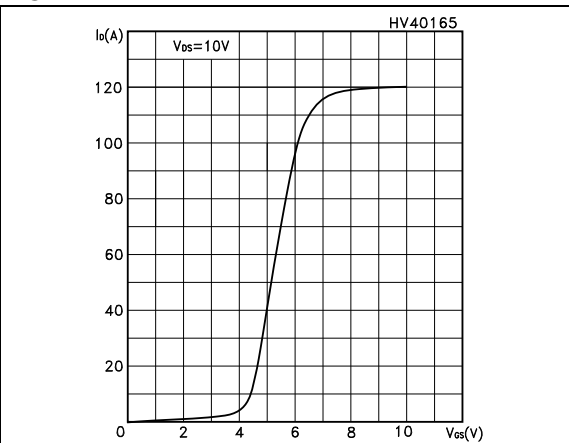


Figure 6. Normalized BVDSS vs temperature

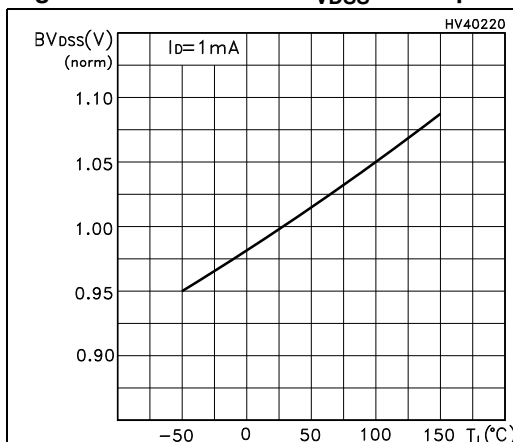


Figure 7. Static drain-source on resistance

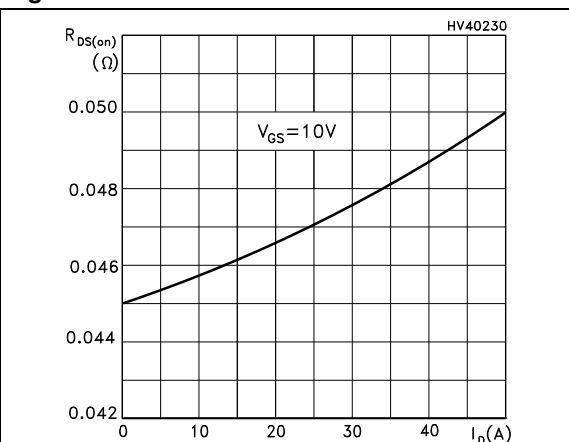


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

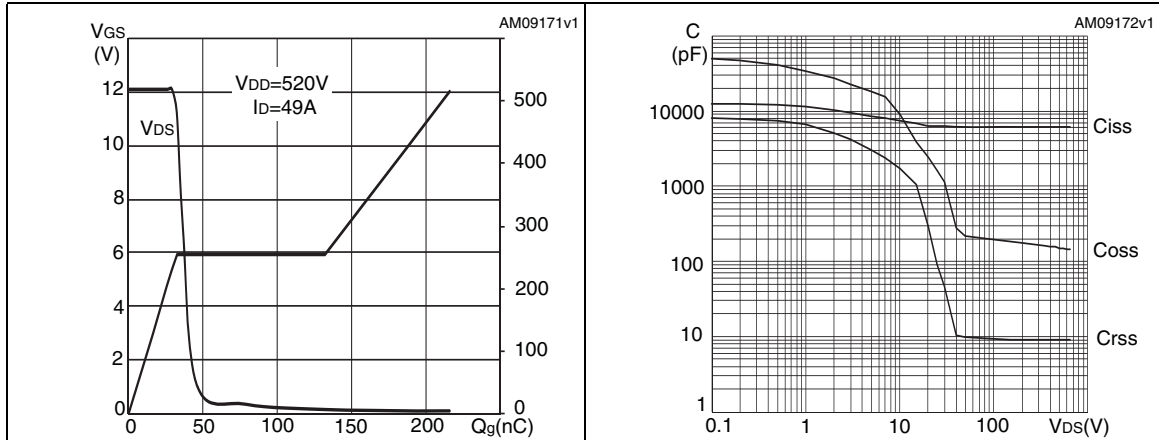


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

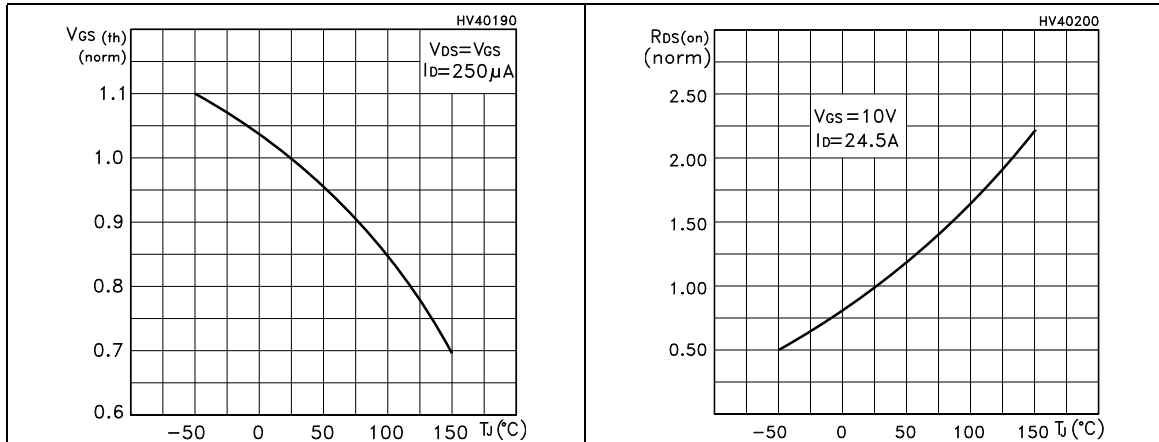
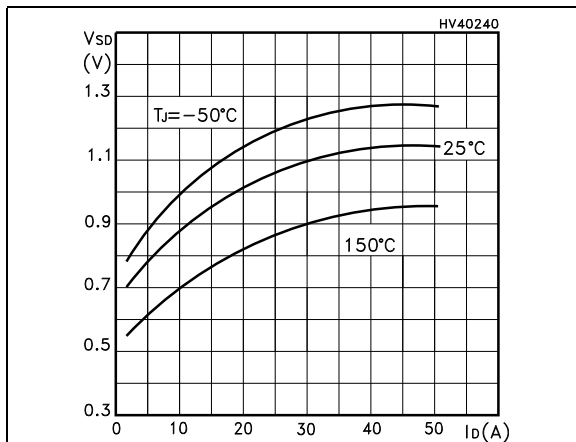
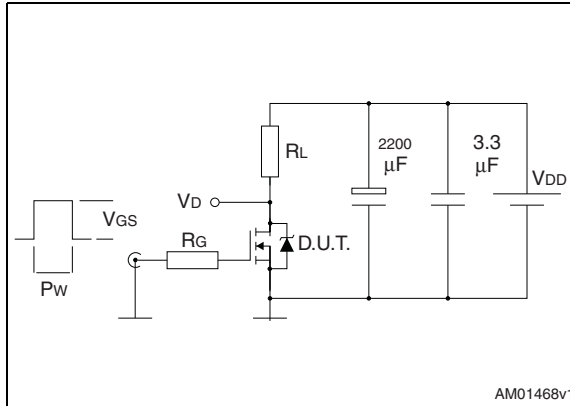


Figure 12. Source-drain diode forward characteristics

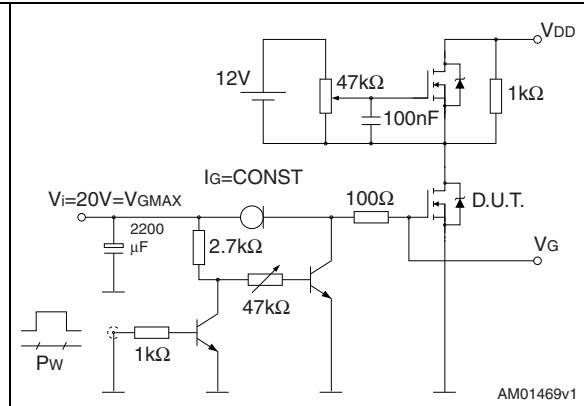


### 3 Test circuits

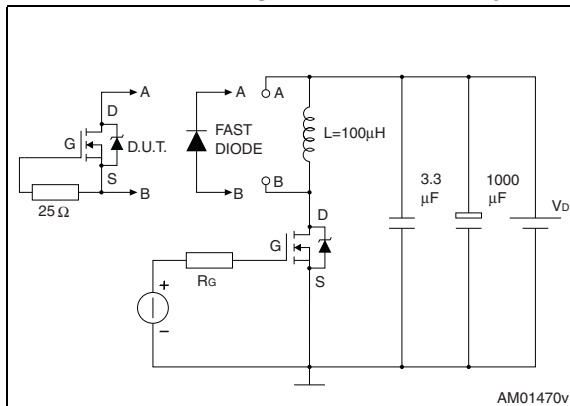
**Figure 13. Switching times test circuit for resistive load**



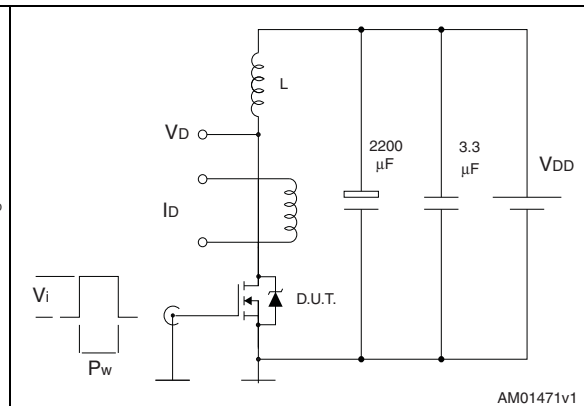
**Figure 14. Gate charge test circuit**



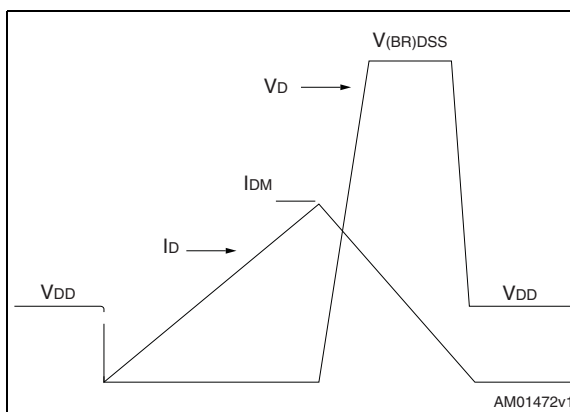
**Figure 15. Test circuit for inductive load switching and diode recovery times**



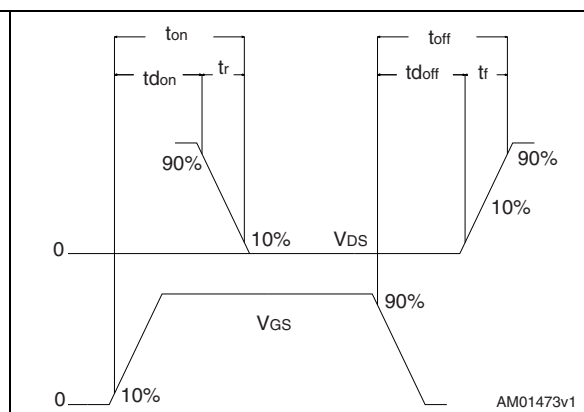
**Figure 16. Unclamped inductive load test circuit**



**Figure 17. Unclamped inductive waveform**



**Figure 18. Switching time waveform**





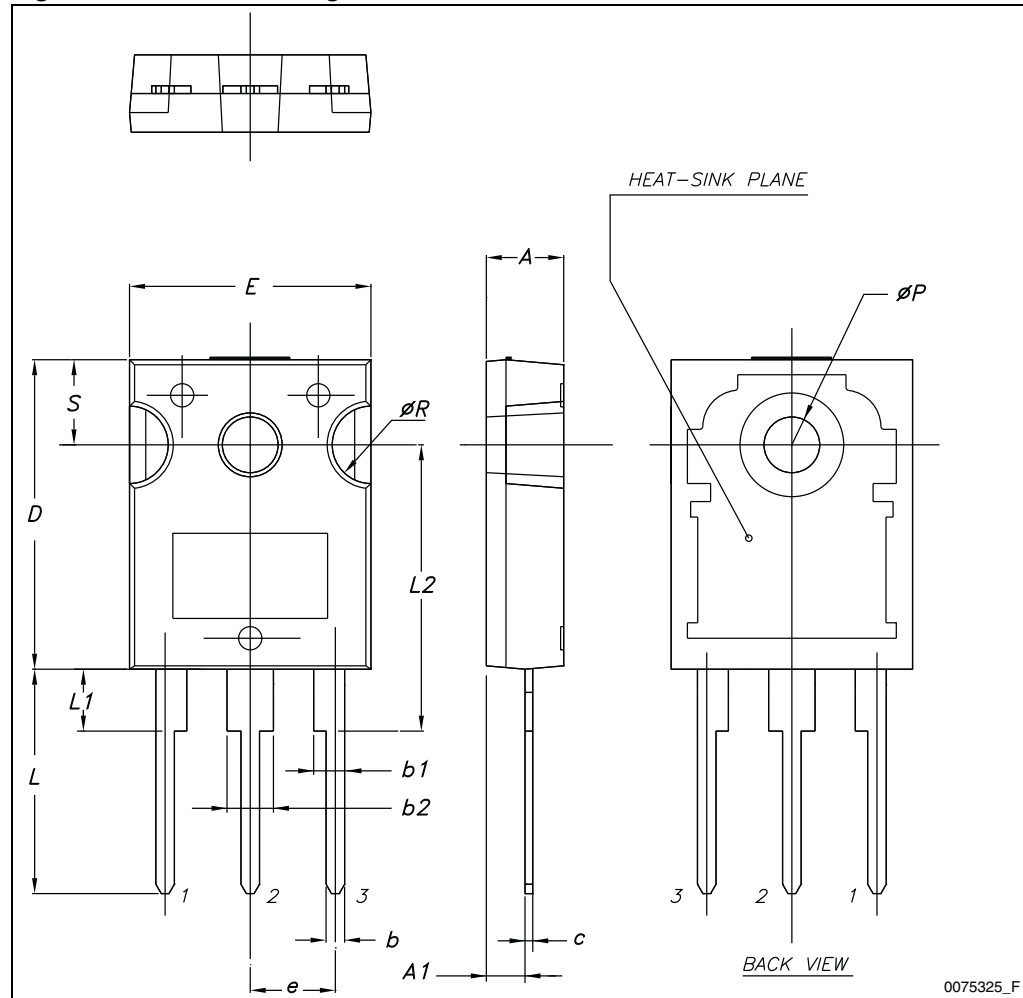
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

Table 8. TO-247 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S		5.50	

Figure 19. TO-247 drawing



## 5 Revision history

Table 9. Document revision history

Date	Revision	Changes
03-Jun-2011	1	Initial release

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