

N-Channel 250-V (D-S) 175 °C MOSFET

PRODUCT SUMMARY

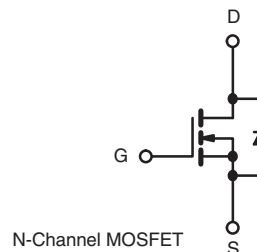
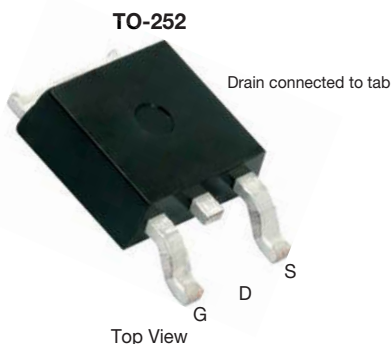
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)
250	0.165 at V _{GS} = 10 V	17

FEATURES

- TrenchFET® power MOSFET
- 175 °C junction temperature
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912



RoHS
COMPLIANT



Ordering Information:

SUD17N25-165-E3 (lead (Pb)-free)

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	250	V
Gate-Source Voltage	V _{GS}	± 20	V
Continuous Drain Current (T _J = 175 °C) ^b	I _D	T _C = 25 °C	17
		T _C = 125 °C	9.8
Pulsed Drain Current	I _{DM}	20	A
Continuous Source Current (Diode Conduction)	I _S	17	A
Single Pulse Avalanche Current	I _{AS}	4	A
Single Pulse Avalanche Energy	E _{AS}	2.4	mJ
Maximum Power Dissipation	P _D	T _C = 25 °C	136 ^b
		T _A = 25 °C	3 ^a
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +175	°C

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Ambient ^a	R _{thJA}	t ≤ 10 s	15	°C/W
		Steady State	40	
Junction-to-Case (Drain)	R _{thJC}	0.85	1.1	

Notes

- Surface mounted on 1" x 1" FR4 board.
- See SOA curve for voltage derating.



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP. ^a	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	250	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2.5	-	4	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 250 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 250 V, V _{GS} = 0 V, T _J = 125 °C	-	-	50	
		V _{DS} = 250 V, V _{GS} = 0 V, T _J = 175 °C	-	-	250	
On-State Drain Current ^b	I _{D(on)}	V _{DS} = 15 V, V _{GS} = 10 V	17	-	-	A
Drain-Source On-State Resistance ^b	R _{DS(on)}	V _{GS} = 10 V, I _D = 14 A	-	0.131	0.165	Ω
		V _{GS} = 10 V, I _D = 14 A, T _J = 125 °C	-	-	0.347	
		V _{GS} = 10 V, I _D = 14 A, T _J = 175 °C	-	-	0.462	
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 17 A	-	36	-	S
Dynamic ^a						
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1 MHz	-	1950	-	pF
Output Capacitance	C _{oss}		-	160	-	
Reverse Transfer Capacitance	C _{rss}		-	70	-	
Total Gate Charge ^c	Q _g	V _{DS} = 125 V, V _{GS} = 10 V, I _D = 17 A	-	30	42	nC
Gate-Source Charge ^c	Q _{gs}		-	10	-	
Gate-Drain Charge ^c	Q _{gd}		-	10	-	
Gate Resistance	R _g		-	1.6	-	Ω
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = 125 V, R _L = 7.35 Ω I _D ≅ 17 A, V _{GEN} = 10 V, R _g = 2.5 Ω	-	15	25	ns
Rise Time ^c	t _r		-	130	195	
Turn-Off Delay Time ^c	t _{d(off)}		-	30	45	
Fall Time ^c	t _f		-	100	150	
Source-Drain Diode Ratings and Characteristics (T _C = 25 °C)						
Pulsed Current	I _{SM}		-	-	20	A
Diode Forward Voltage ^b	V _{SD}	I _F = 17 A, V _{GS} = 0 V	-	0.9	1.5	V
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 17 A, dI/dt = 100 A/μs	-	115	175	ns

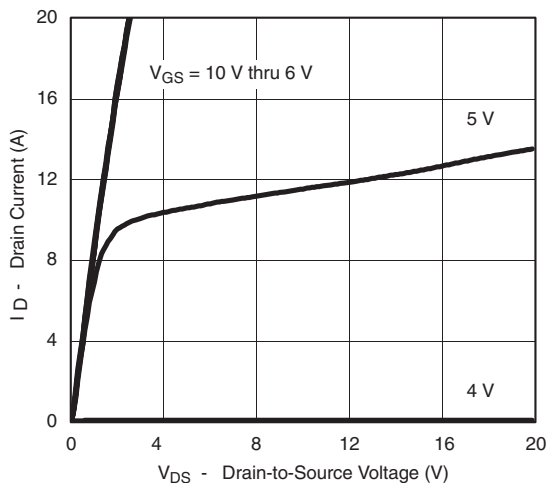
Notes

- a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
c. Independent of operating temperature.

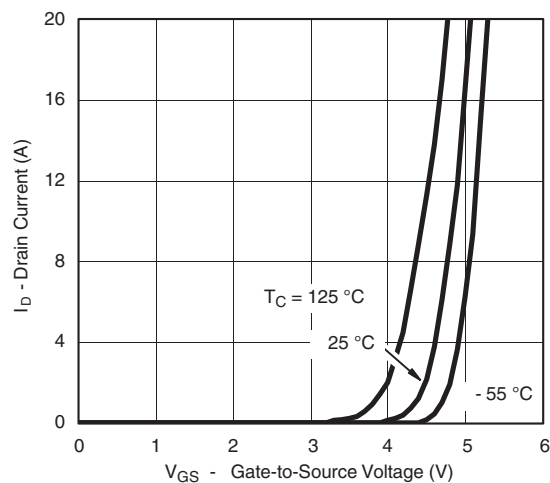
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



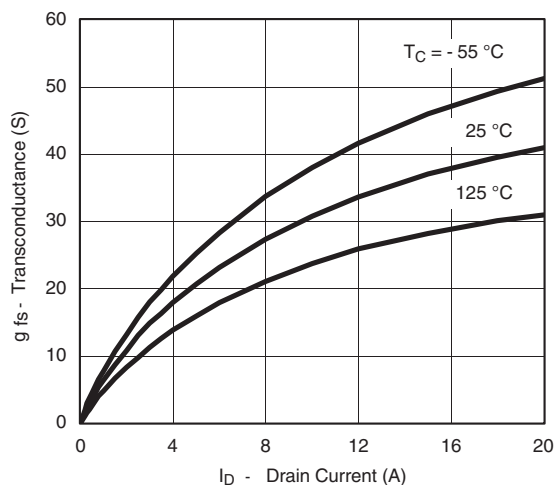
TYPICAL CHARACTERISTICS (25 °C unless otherwise noted)



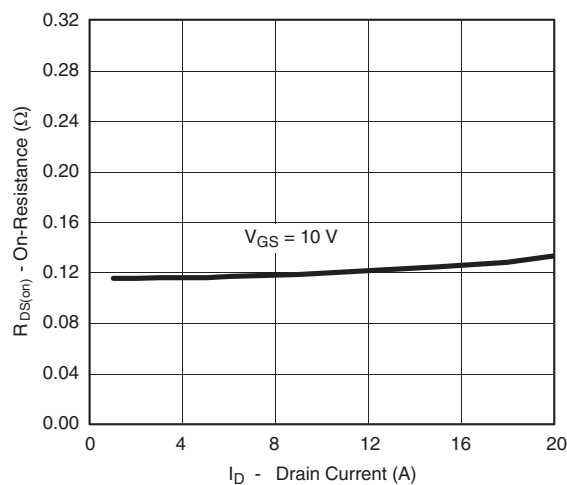
Output Characteristics



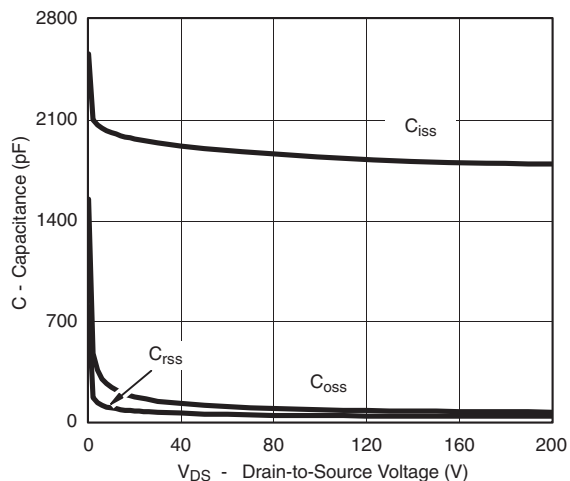
Transfer Characteristics



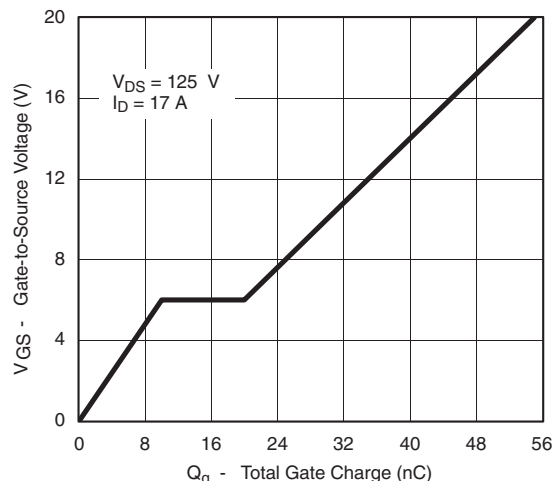
Transconductance



On-Resistance vs. Drain Current



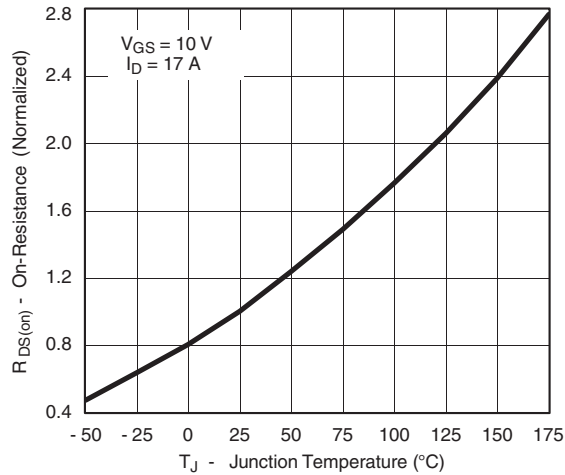
Capacitance



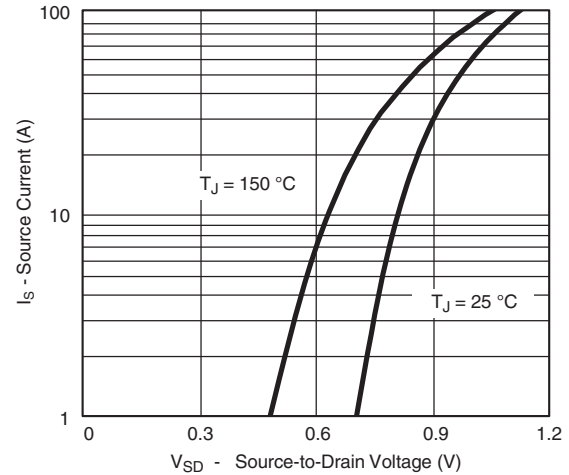
Gate Charge



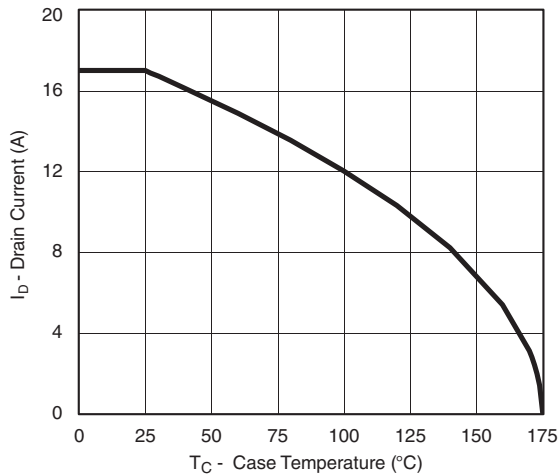
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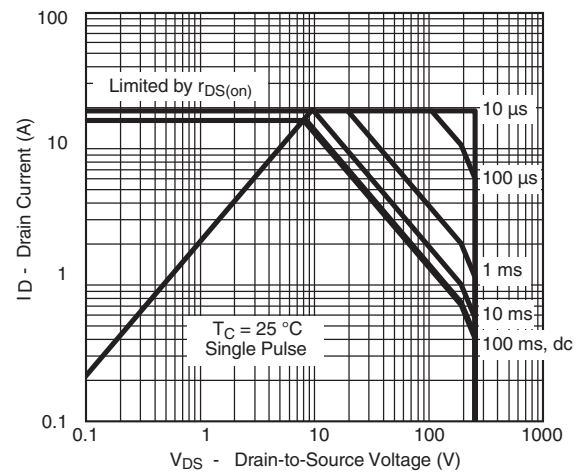
On-Resistance vs. Junction Temperature



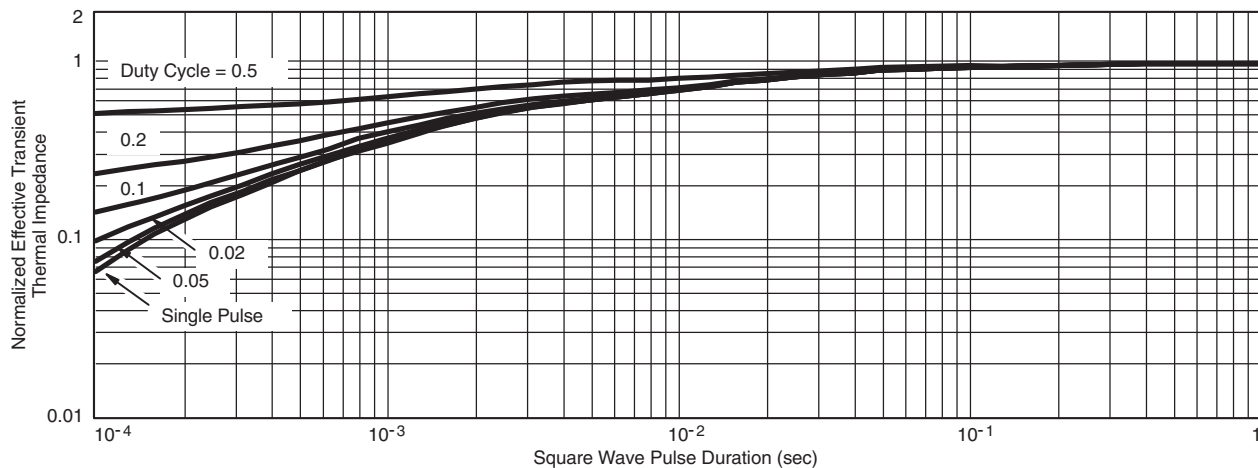
Source-Drain Diode Forward Voltage



Max. Avalanche Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?72851.



TO-252AA Case Outline

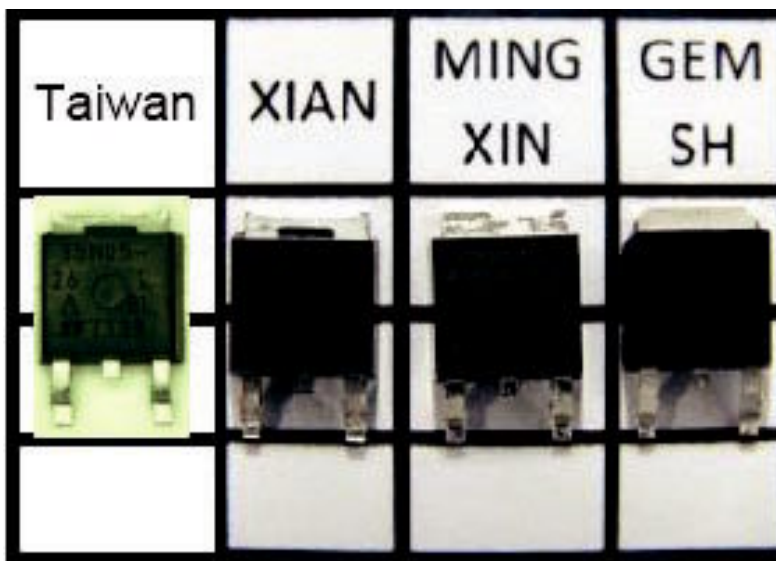


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060

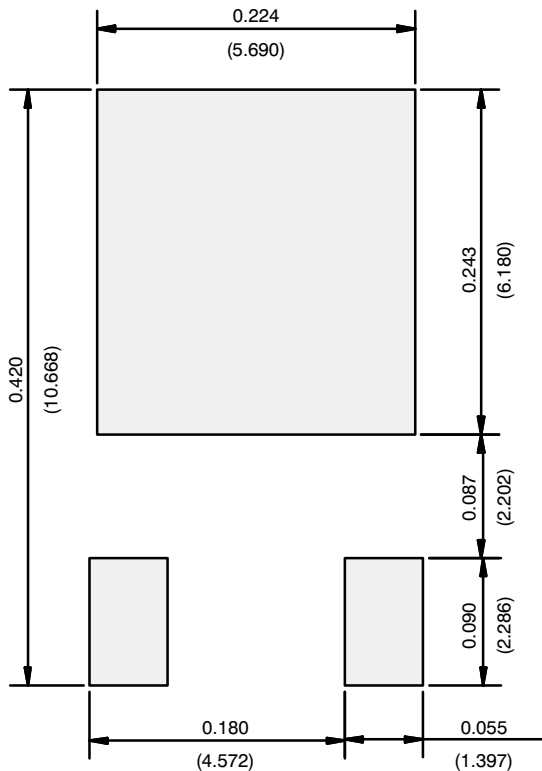
ECN: T13-0359-Rev. O, 03-Jun-13
DWG: 5347

Notes

- Dimension L3 is for reference only.
- Xi'an, Mingxin, and GEM SH actual photo.



RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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