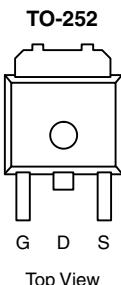


N-Channel 200 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
200	0.090 at $V_{GS} = 10$ V	19
	0.105 at $V_{GS} = 6$ V	17.5

FEATURES

- TrenchFET® Power MOSFET
- 175 °C Junction Temperature
- PWM Optimized
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC

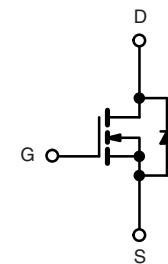


Drain Connected to Tab

Top View

Ordering Information:

SUD19N20-90-E3 (Lead (Pb)-free)



N-Channel MOSFET

APPLICATIONS

- Primary Side Switch

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)				
Parameter	Symbol		Limit	Unit
Drain-Source Voltage	V_{DS}		200	V
Gate-Source Voltage	V_{GS}		± 20	
Continuous Drain Current ($T_J = 175$ °C) ^b	I_D		19	A
	$T_C = 25$ °C		11	
Pulsed Drain Current	I_{DM}		40	
Continuous Source Current (Diode Conduction)	I_S		19	
Avalanche Current	I_{AS}		19	mJ
Single Pulse Avalanche Energy	E_{AS}		18	
Maximum Power Dissipation	P_D		136 ^b	
	$T_A = 25$ °C		3 ^a	
Operating Junction and Storage Temperature Range	T_J, T_{stg}		- 55 to 175	°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Junction-to-Ambient ^a	$t \leq 10$ s	R_{thJA}	15	18	°C/W
	Steady State		40	50	
Junction-to-Case (Drain)		R_{thJC}	0.85	1.1	

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b. See SOA curve for voltage derating.

SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ. ^a	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$	200			V
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	2		4	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}$, $V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 200 \text{ V}$, $V_{GS} = 0 \text{ V}$		1		μA
		$V_{DS} = 200 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 125^\circ\text{C}$		50		
		$V_{DS} = 200 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 175^\circ\text{C}$		250		
On-State Drain Current ^b	$I_{D(\text{on})}$	$V_{DS} = 5 \text{ V}$, $V_{GS} = 10 \text{ V}$	40			A
Drain-Source On-State Resistance ^b	$R_{DS(\text{on})}$	$V_{GS} = 10 \text{ V}$, $I_D = 5 \text{ A}$		0.075	0.090	Ω
		$V_{GS} = 10 \text{ V}$, $I_D = 5 \text{ A}$, $T_J = 125^\circ\text{C}$			0.190	
		$V_{GS} = 10 \text{ V}$, $I_D = 5 \text{ A}$, $T_J = 175^\circ\text{C}$			0.260	
		$V_{GS} = 6 \text{ V}$, $I_D = 5 \text{ A}$		0.082	0.105	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15 \text{ V}$, $I_D = 19 \text{ A}$		35		S
Dynamic^a						
Input Capacitance	C_{iss}	$V_{GS} = 0 \text{ V}$, $V_{DS} = 25 \text{ V}$, $F = 1 \text{ MHz}$		1800		pF
Output Capacitance	C_{oss}			180		
Reverse Transfer Capacitance	C_{rss}			80		
Total Gate Charge ^c	Q_g	$V_{DS} = 100 \text{ V}$, $V_{GS} = 10 \text{ V}$, $I_D = 19 \text{ A}$		34	51	nC
Gate-Source Charge ^c	Q_{gs}			8		
Gate-Drain Charge ^c	Q_{gd}			12		
Gate Resistance	R_g	$V_{DD} = 100 \text{ V}$, $R_L = 5.2 \Omega$ $I_D \approx 19 \text{ A}$, $V_{GEN} = 10 \text{ V}$, $R_g = 2.5 \Omega$	0.5		2.9	Ω
Turn-On Delay Time ^c	$t_{d(\text{on})}$			15	25	ns
Rise Time ^c	t_r			50	75	
Turn-Off Delay Time ^c	$t_{d(\text{off})}$			30	45	
Fall Time ^c	t_f			60	90	
Source-Drain Diode Ratings and Characteristics ($T_C = 25^\circ\text{C}$)						
Pulsed Current	I_{SM}				50	A
Diode Forward Voltage ^b	V_{SD}	$I_F = 19 \text{ A}$, $V_{GS} = 0 \text{ V}$		0.9	1.5	V
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 19 \text{ A}$, $dl/dt = 100 \text{ A}/\mu\text{s}$		180	250	ns

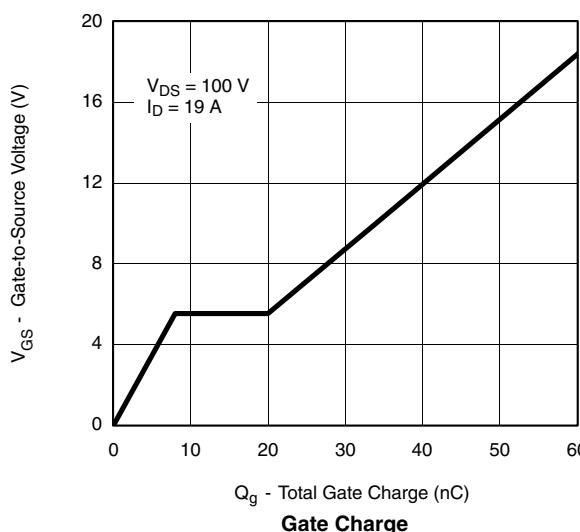
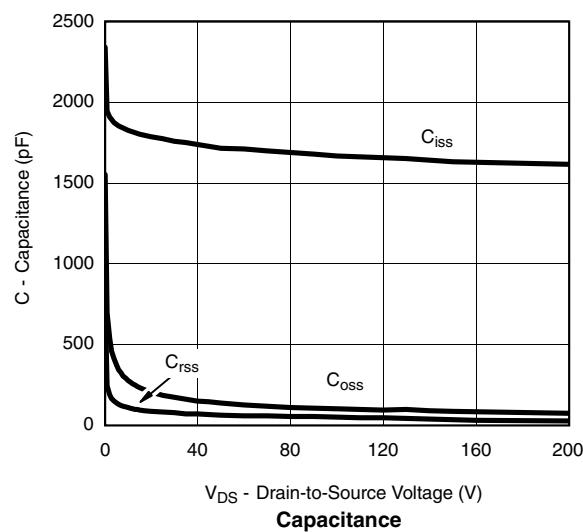
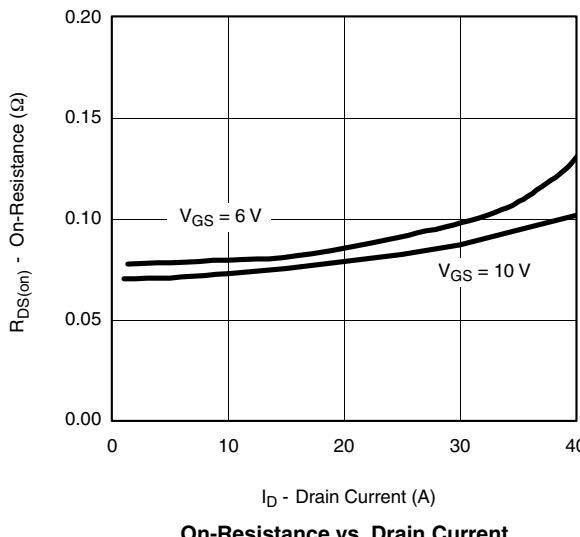
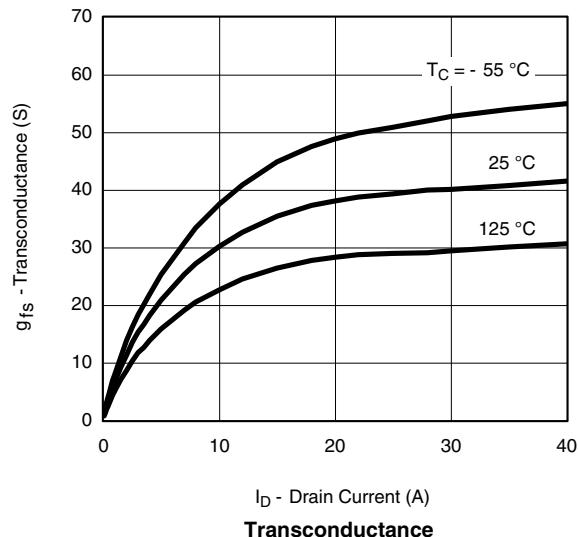
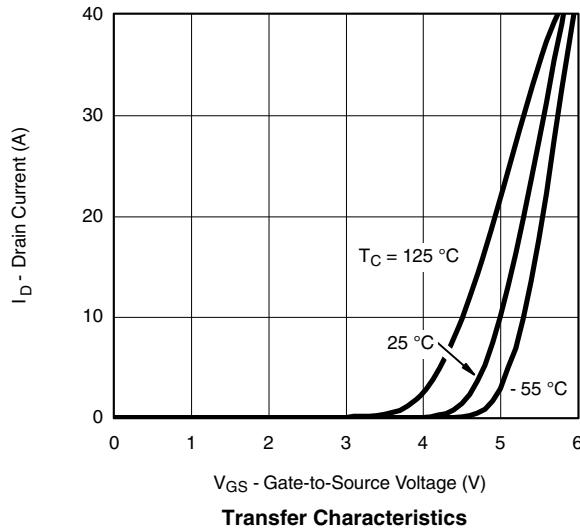
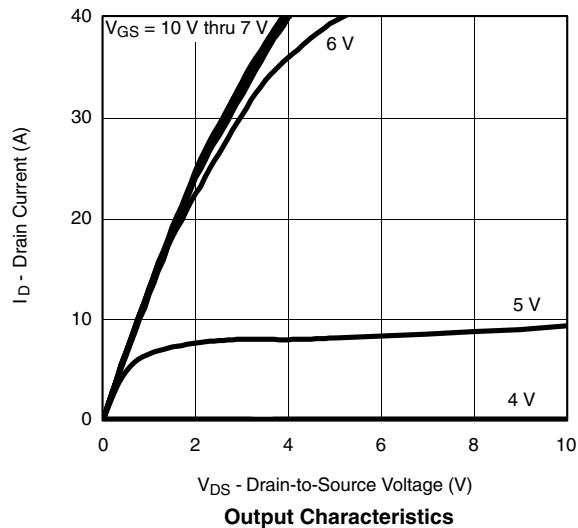
Notes:

a. Guaranteed by design, not subject to production testing.

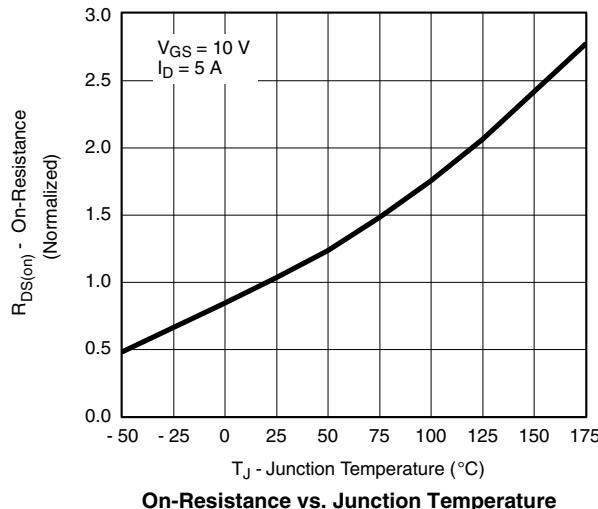
b. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.

c. Independent of operating temperature.

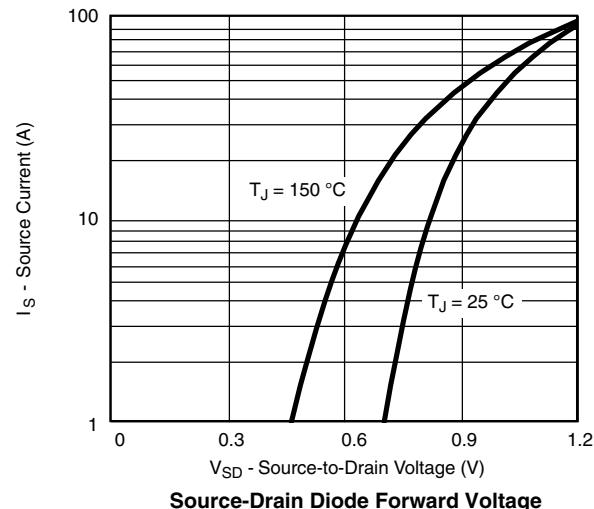
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

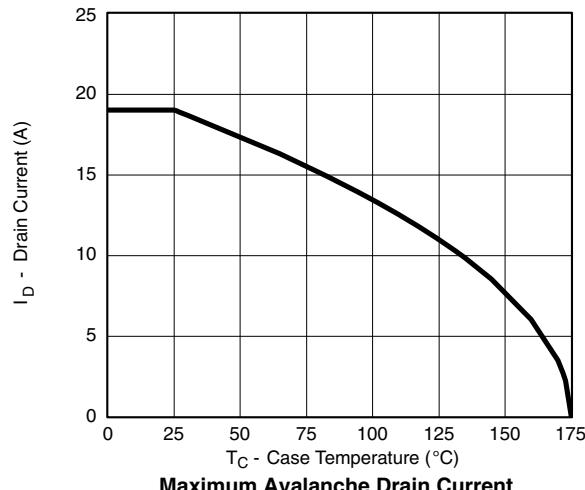


On-Resistance vs. Junction Temperature

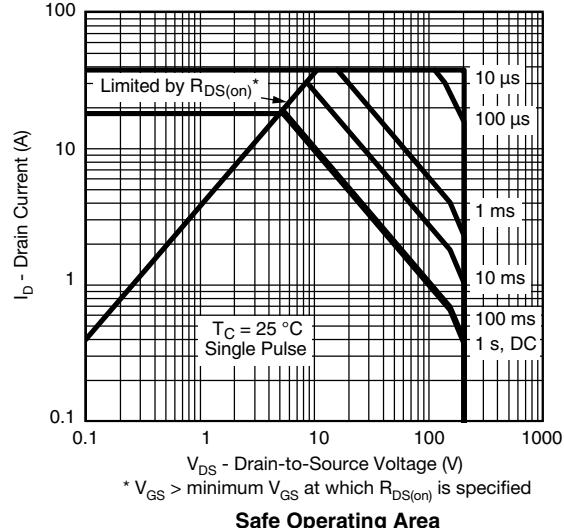


Source-Drain Diode Forward Voltage

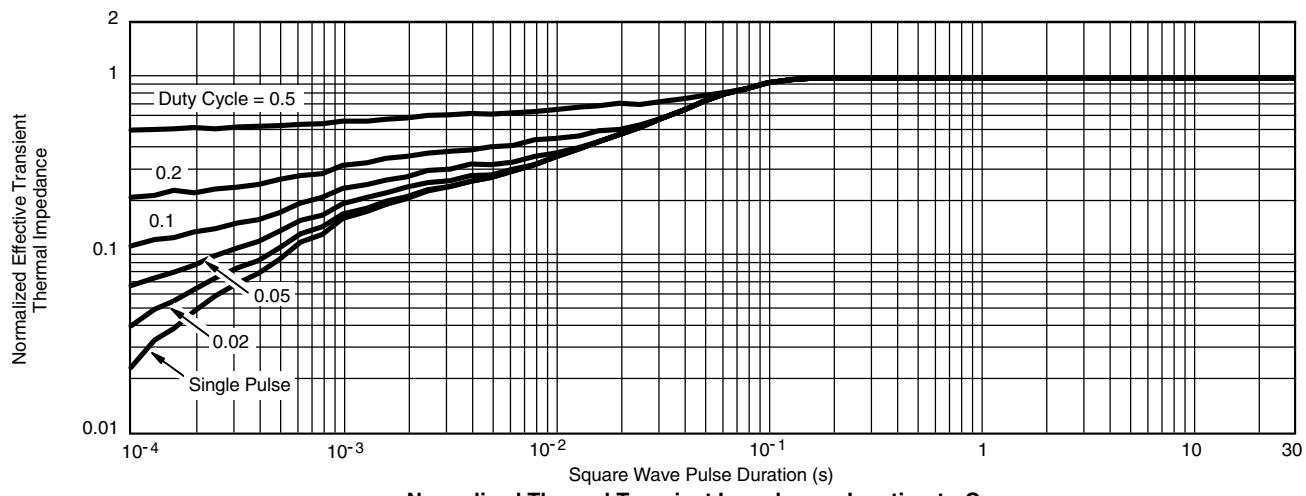
THERMAL RATINGS



Maximum Avalanche Drain Current
vs. Case Temperature



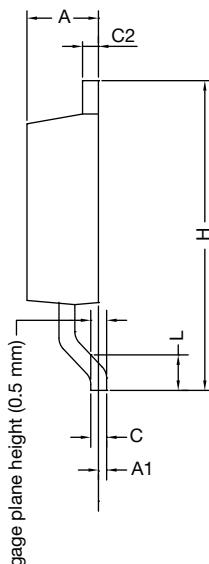
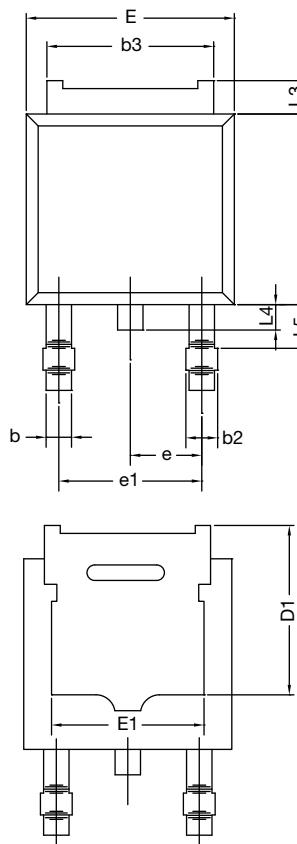
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71767.

TO-252AA Case Outline



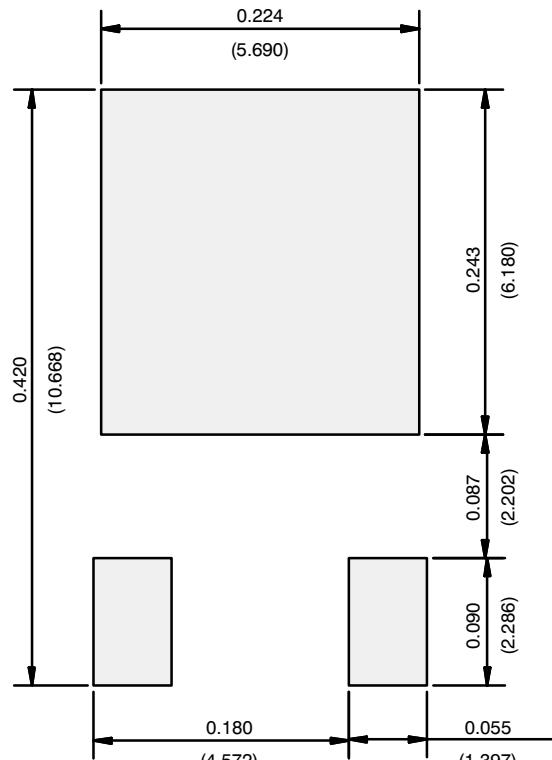
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060

ECN: T16-0236-Rev. P, 16-May-16
DWG: 5347

Notes

- Dimension L3 is for reference only.

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



**Recommended Minimum Pads
Dimensions in Inches/(mm)**

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