



## N-Channel 20-V (D-S), 175 °C MOSFET

## PRODUCT SUMMARY

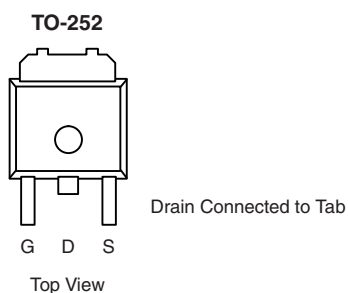
$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A) <sup>a</sup>	$Q_g$ (Typ)
20	0.0033 at $V_{GS} = 10$ V	40	30 nC
	0.0044 at $V_{GS} = 4.5$ V	40	

## FEATURES

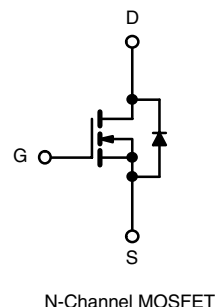
- TrenchFET<sup>®</sup> Power MOSFET
- 100 %  $R_g$  Tested

## APPLICATIONS

- Server

RoHS  
COMPLIANT

Order Number:  
SUD40N02-3m3P-E3 (Lead (Pb)-free)



ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		$V_{DS}$	20	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 150$ °C)	$T_C = 25$ °C	$I_D$	40 <sup>a</sup>	A
	$T_C = 100$ °C		40 <sup>a</sup>	
	$T_A = 25$ °C		24.4 <sup>b</sup>	
	$T_A = 100$ °C		17.2 <sup>b</sup>	
Pulsed Drain Current		$I_{DM}$	100	
Continuous Source-Drain Diode Current	$T_C = 25$ °C	$I_S$	40 <sup>a</sup>	
	$T_A = 25$ °C		2.8 <sup>b</sup>	
Maximum Power Dissipation	$T_C = 25$ °C	$P_D$	79	W
	$T_C = 100$ °C		39.5	
	$T_A = 25$ °C		3.3 <sup>b</sup>	
	$T_A = 100$ °C		1.6 <sup>b</sup>	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	- 55 to 175	°C

## THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b</sup>	Steady State	$R_{thJA}$	37	45	°C/W
Maximum Junction-to-Case	Steady State	$R_{thJC}$	1.5	1.9	

Notes:

a. Package limited.

b. Surface Mounted on 1" x 1" FR4 board.

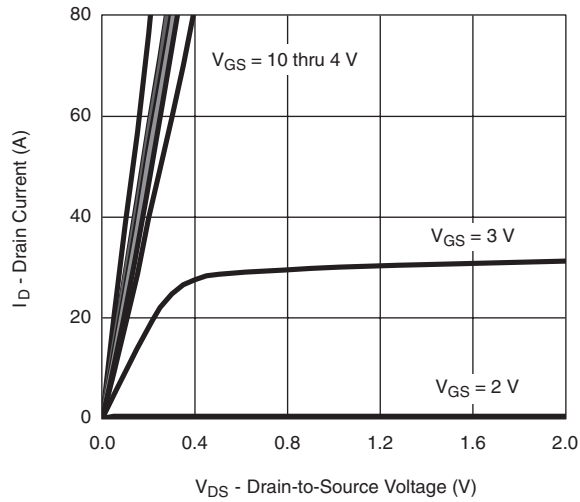
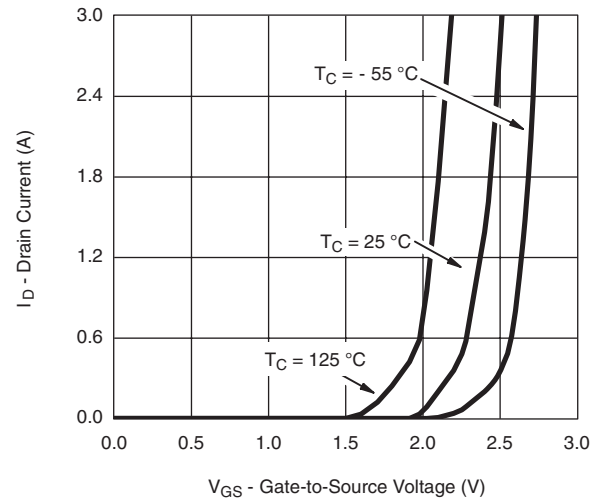
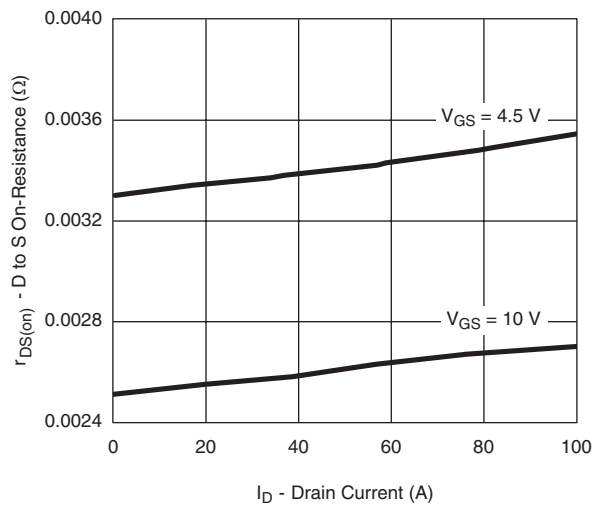
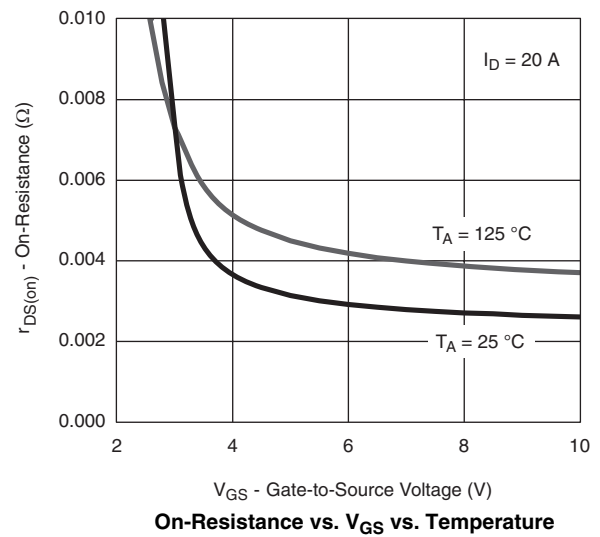
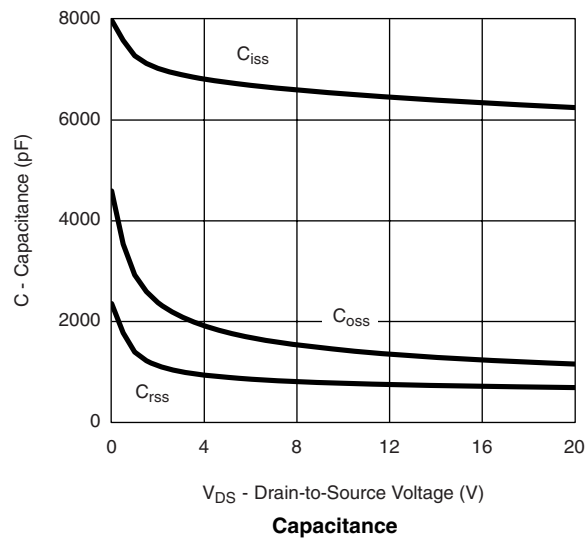
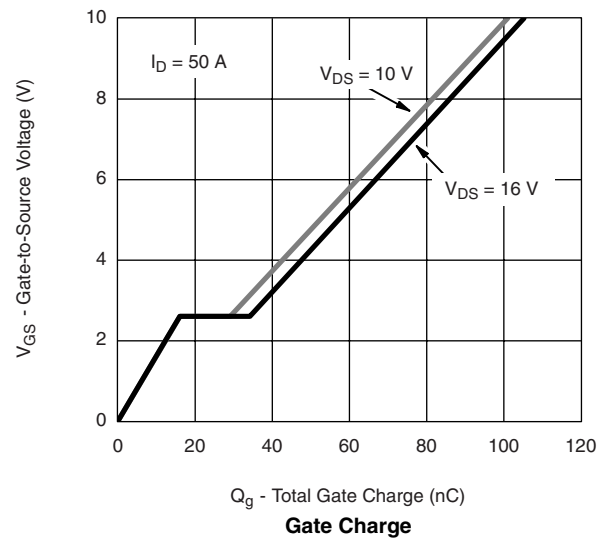
SPECIFICATIONS T <sub>J</sub> = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	20			V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA		21		mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>			- 6.9		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1		3	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 100 °C			20	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 10 V	30			A
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A		0.0027	0.0033	Ω
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 20 A		0.0036	0.0044	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 20 A		100		S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V, f = 1 MHz		6520		pF
Output Capacitance	C <sub>oss</sub>			1430		
Reverse Transfer Capacitance	C <sub>rss</sub>			770		
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 50 A		105	160	nC
Gate-Source Charge	Q <sub>gs</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 50 A		50	75	
Gate-Drain Charge	Q <sub>gd</sub>			17		
Gate Resistance	R <sub>g</sub>	f = 1 MHz		1.2	1.9	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 10 V, R <sub>L</sub> = 0.2 Ω I <sub>D</sub> ≡ 50 A, V <sub>GEN</sub> = 4.5 V, R <sub>g</sub> = 1 Ω		40	60	ns
Rise Time	t <sub>r</sub>			30	45	
Turn-Off Delay Time	t <sub>d(off)</sub>			67	101	
Fall Time	t <sub>f</sub>			33	50	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 10 V, R <sub>L</sub> = 0.2 Ω I <sub>D</sub> ≡ 50 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω		13	20	
Rise Time	t <sub>r</sub>			7	11	
Turn-Off Delay Time	t <sub>d(off)</sub>			40	60	
Fall Time	t <sub>f</sub>			9	14	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			40	A
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>				100	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 20 A		0.81	1.2	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 50 A, di/dt = 100 A/μs, T <sub>J</sub> = 25 °C		38	57	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			34	51	nC
Reverse Recovery Fall Time	t <sub>a</sub>			18		ns
Reverse Recovery Rise Time	t <sub>b</sub>			20		

Notes:

a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

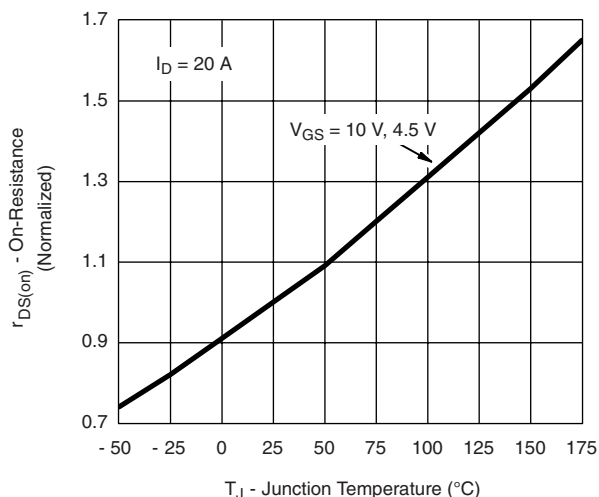
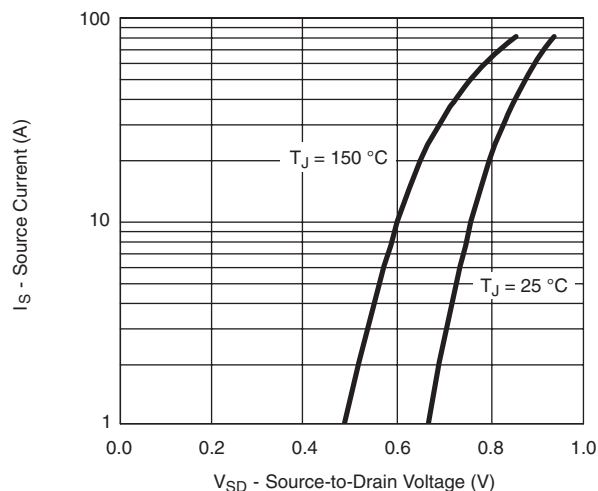
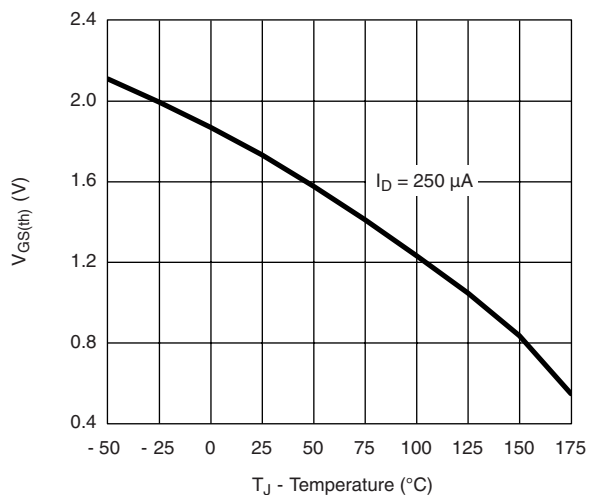
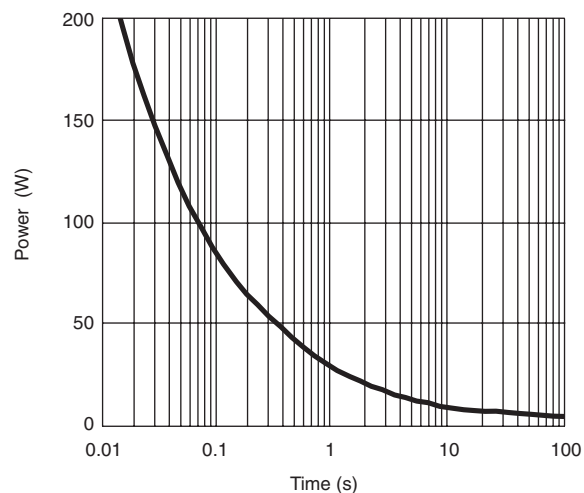
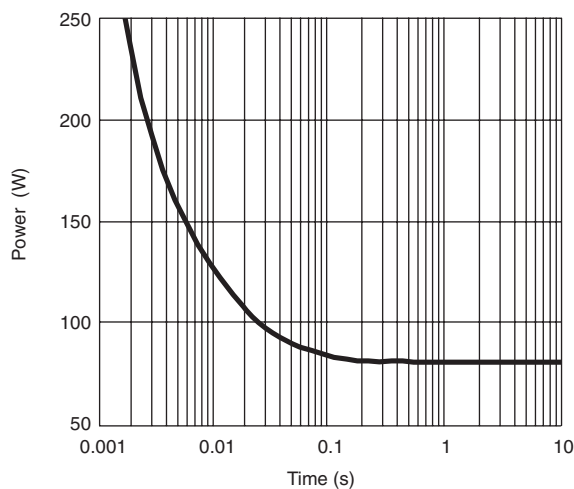
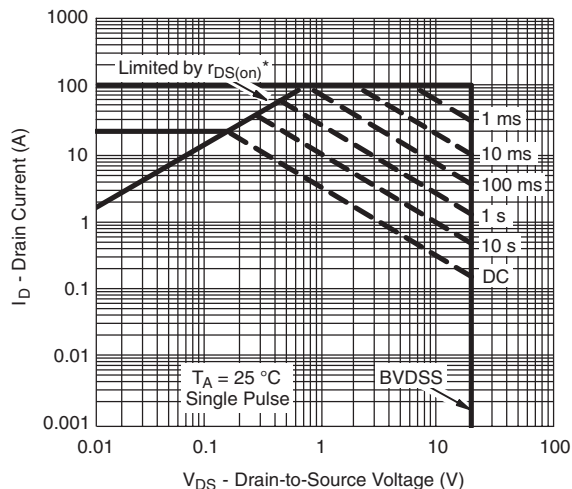
b. Guaranteed by design, not subject to production testing.

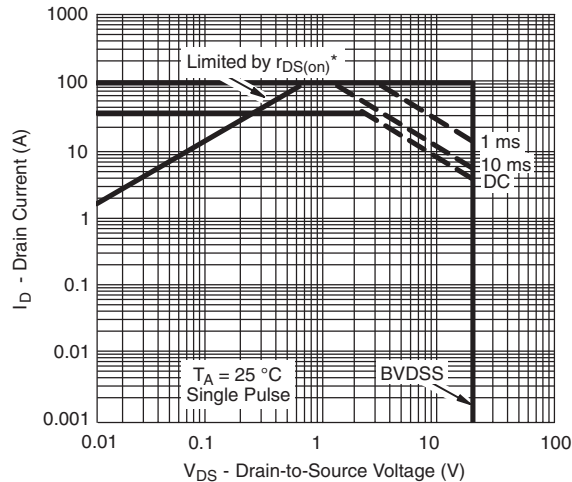
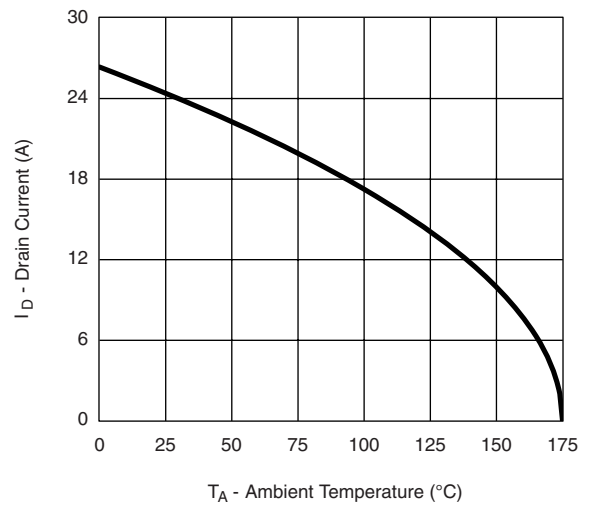
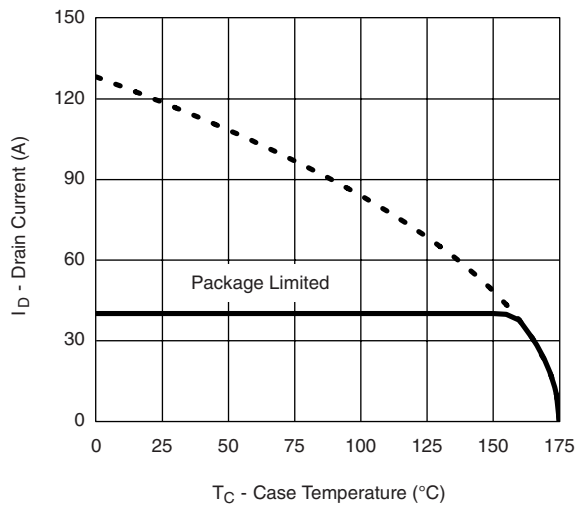
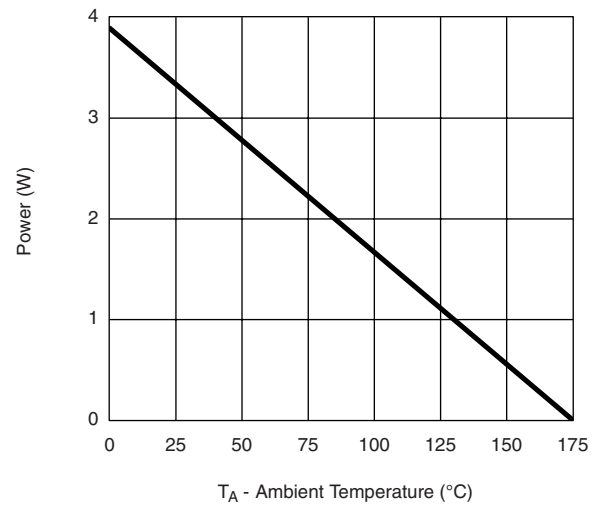
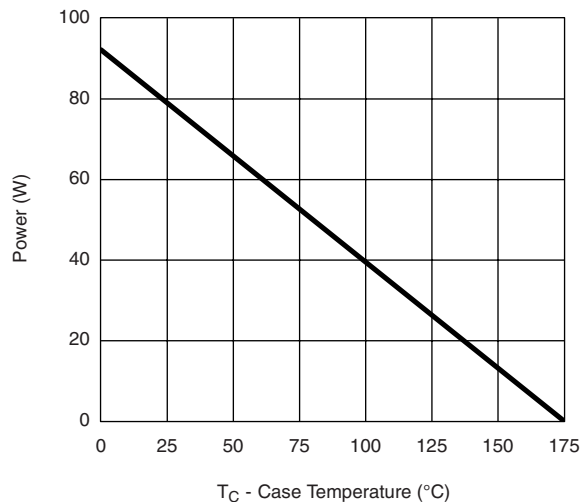
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted**Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current****On-Resistance vs.  $V_{GS}$  vs. Temperature****Capacitance****Gate Charge**

**SUD40N02-3m3P**

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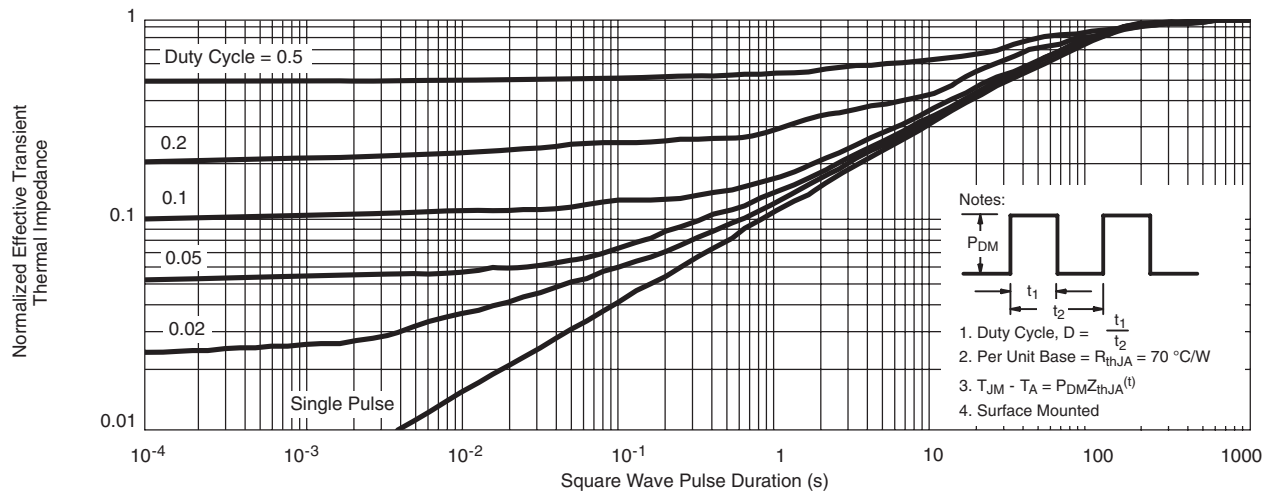
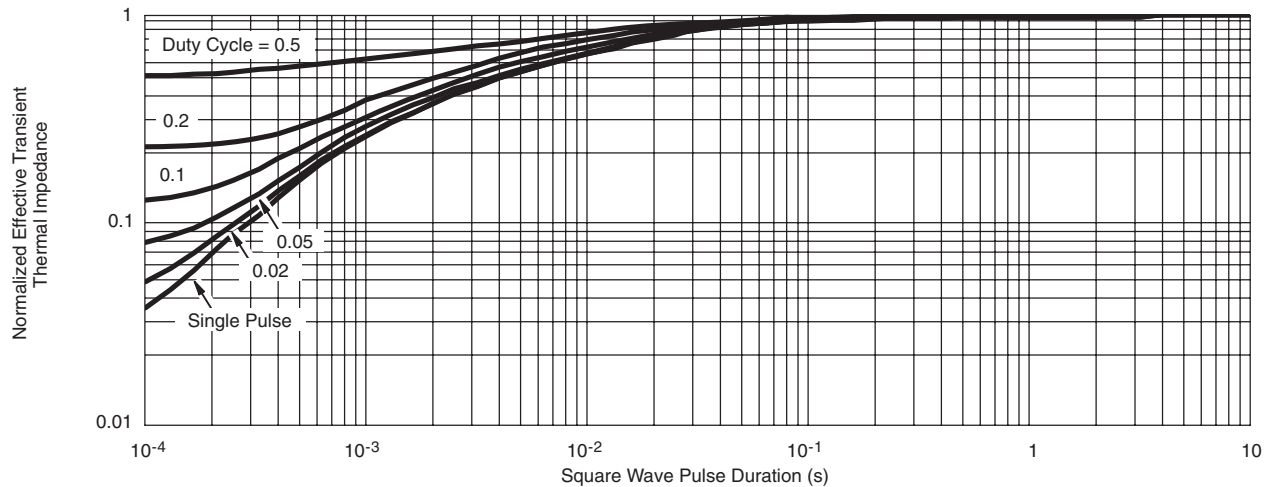
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted**On-Resistance vs. Junction Temperature****Forward Diode Voltage vs. Temperature****Threshold Voltage****Single Pulse Power, Junction-to-Ambient****Single Pulse Power, Junction-to-Case**\*  $V_{GS}$  > minimum  $V_{GS}$  at which  $r_{DS(on)}$  is specified**Safe Operating Area, Junction-to-Ambient**

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $r_{DS(on)}$  is specified**Safe Operating Area, Junction-to-Case****Current Derating\*\*, Junction-to-Ambient****Current Derating\*\*, Junction-to-Case****Power Derating\*\*, Junction-to-Ambient****Power Derating\*\*, Junction-to-Case**

\*\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 175\text{ }^{\circ}\text{C}$ , using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**SUD40N02-3m3P**

Vishay Siliconix

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Case**

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