

N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^b
30	0.0095 at $V_{GS} = 10$ V	63 ^b
	0.014 at $V_{GS} = 4.5$ V	52 ^b

FEATURES

- TrenchFET® Power MOSFET
- Optimized for High- or Low-Side
- 100 % R_g Tested

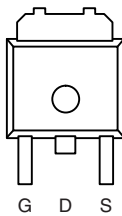


Available
RoHS*
COMPLIANT

APPLICATIONS

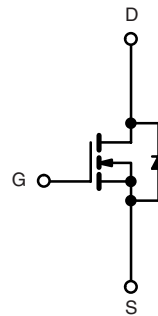
- DC/DC Converters
- Synchronous Rectifiers

TO-252



Top View

Drain Connected to Tab



N-Channel MOSFET

Ordering Information: SUD50N03-09P
SUD50N03-09P-E3 (Lead (Pb)-free)

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ^a	I_D	$T_C = 25$ °C	63 ^b
		$T_C = 100$ °C	44.5 ^b
Pulsed Drain Current	I_{DM}	50	A
Continuous Source Current (Diode Conduction) ^a	I_S	5	
Avalanche Current	I_{AS}	35	
Single Pulse Avalanche Energy	E_{AS}	61	mJ
Maximum Power Dissipation	P_D	$T_C = 25$ °C	65.2
		$T_A = 25$ °C	7.5 ^a
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 10$ s	16	°C/W
		Steady State	40	
Maximum Junction-to-Case	R_{thJC}	1.8	2.3	

Notes:

a. Surface Mounted on FR4 board, $t \leq 10$ s.

b. Based on maximum allowable Junction Temperature, package limitation current is 50 A.

* Pb containing terminations are not RoHS compliant, exemptions may apply.

SPECIFICATIONS T _J = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ. ^a	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	30			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.0		3.0	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			1	μA
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 125 °C			50	
On-State Drain Current ^b	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	50			A
Drain-Source On-State Resistance ^b	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A		0.0076	0.0095	Ω
		V _{GS} = 10 V, I _D = 20 A, T _J = 125 °C			0.015	
		V _{GS} = 4.5 V, I _D = 20 A		0.0115	0.014	
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 20 A	20			S
Dynamic ^a						
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1 MHz		2200		pF
Output Capacitance	C _{oss}			410		
Reverse Transfer Capacitance	C _{rss}			180		
Total Gate Charge ^c	Q _g	V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 50 A		11	16	nC
Gate-Source Charge ^c	Q _{gs}			7.5		
Gate-Drain Charge ^c	Q _{gd}			5.0		
Gate Resistance	R _g		0.5	1.5	2.1	Ω
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = 15 V, R _L = 0.3 Ω I _D ≅ 50 A, V _{GEN} = 10 V, R _g = 2.5 Ω		9	15	ns
Rise Time ^c	t _r			15	25	
Turn-Off Delay Time ^c	t _{d(off)}			22	35	
Fall Time ^c	t _f			8	12	
Source-Drain Diode Ratings and Characteristic T _C = 25 °C						
Pulsed Current	I _{SM}				100	A
Diode Forward Voltage ^b	V _{SD}	I _F = 50 A, V _{GS} = 0 V		1.2	1.5	V
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 50 A, di/dt = 100 A/μs		35	70	ns

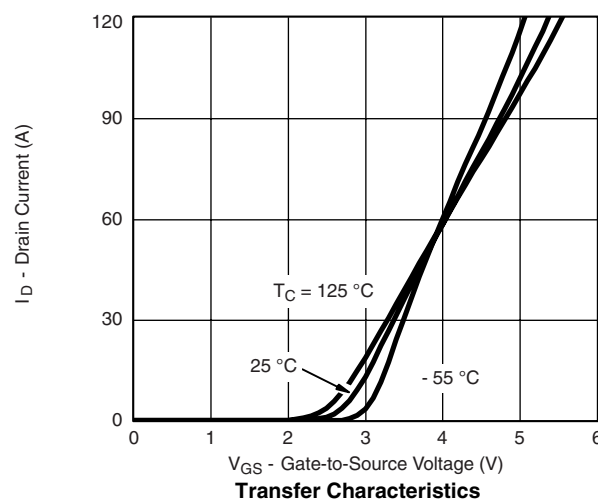
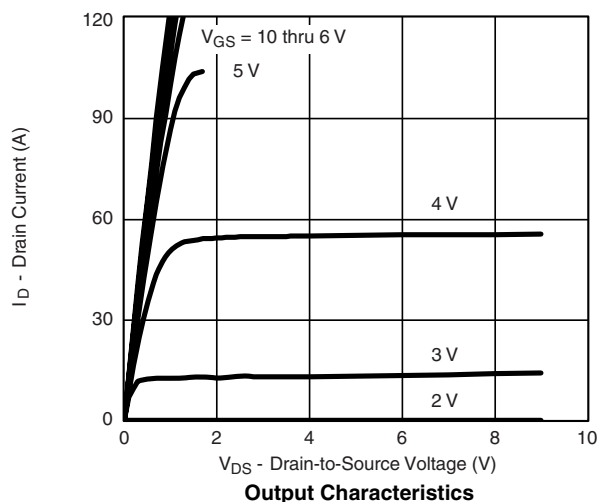
Notes:

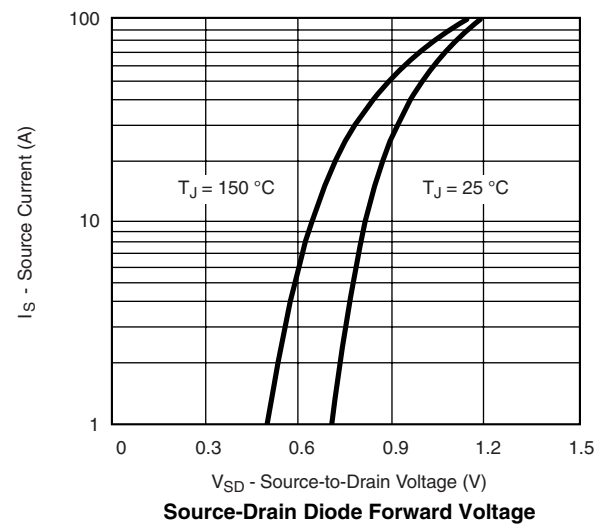
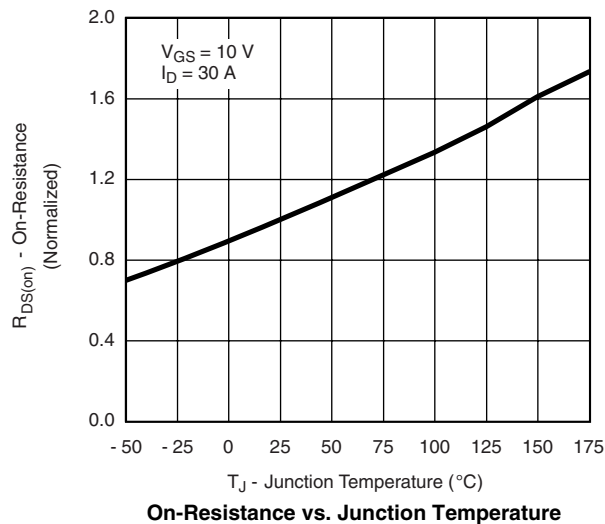
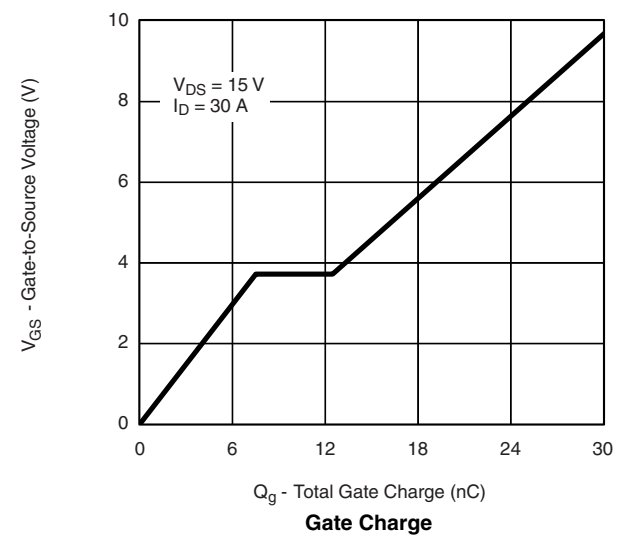
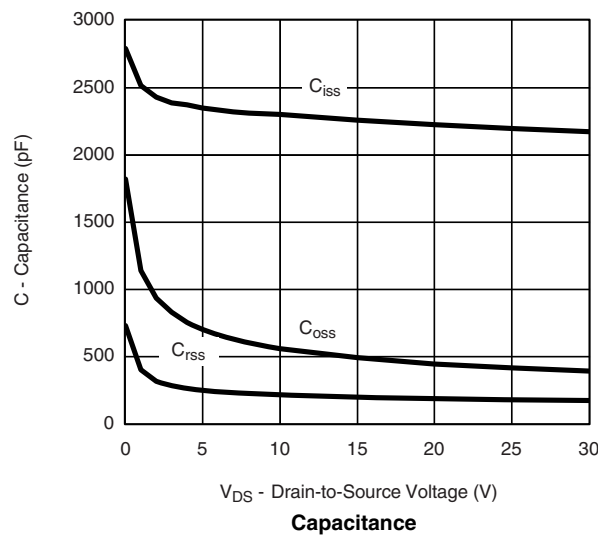
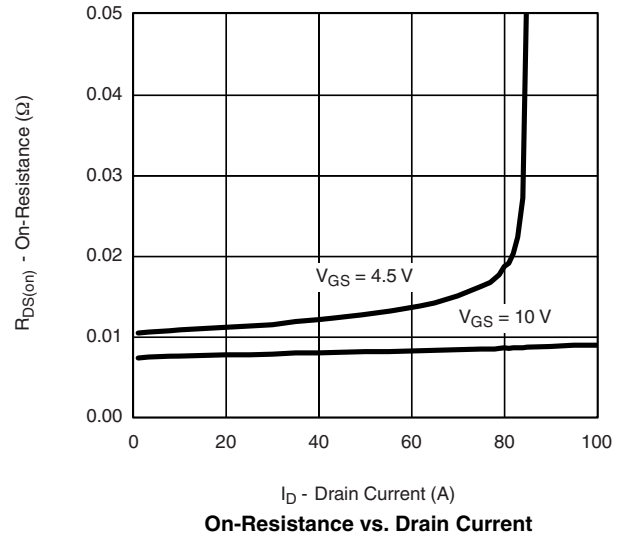
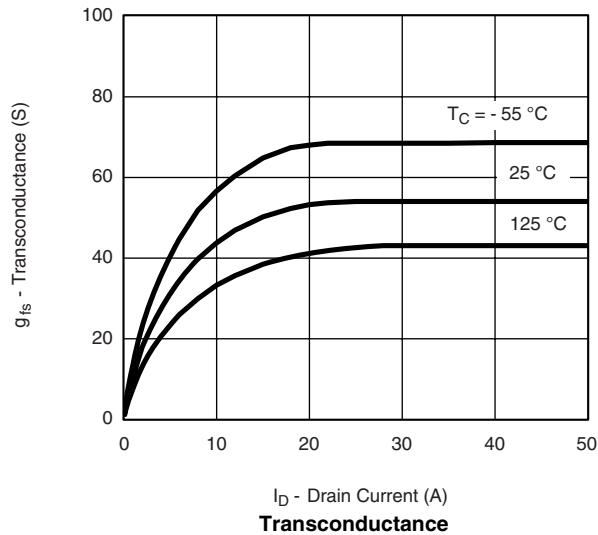
a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

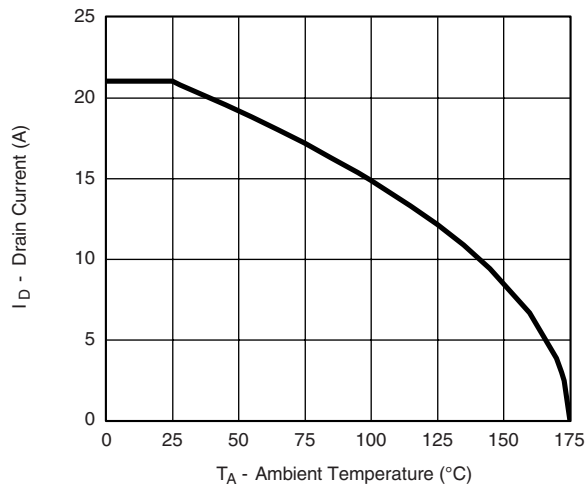
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

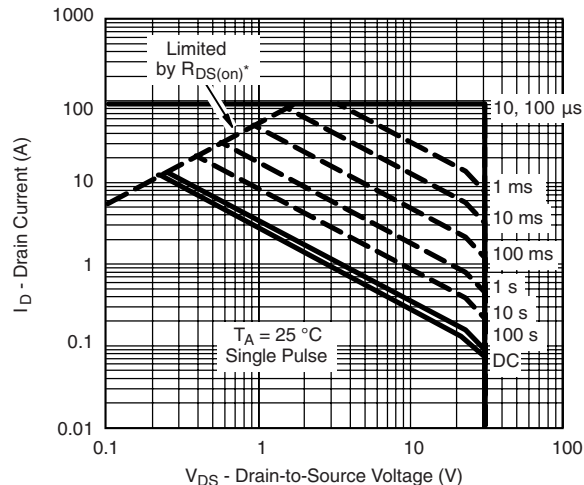
TYPICAL CHARACTERISTICS 25°C , unless otherwise noted

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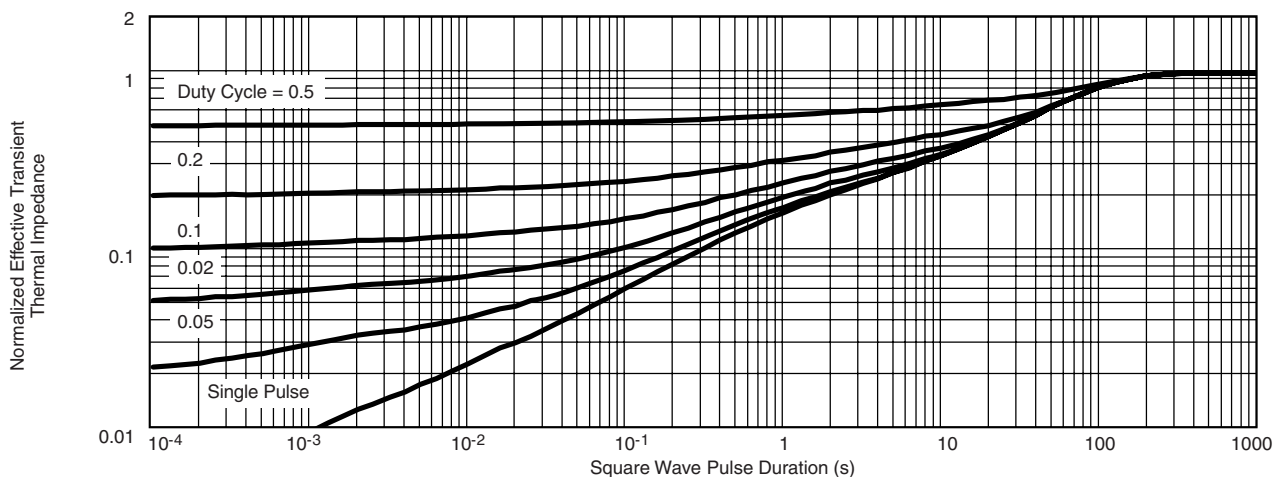
THERMAL RATINGS



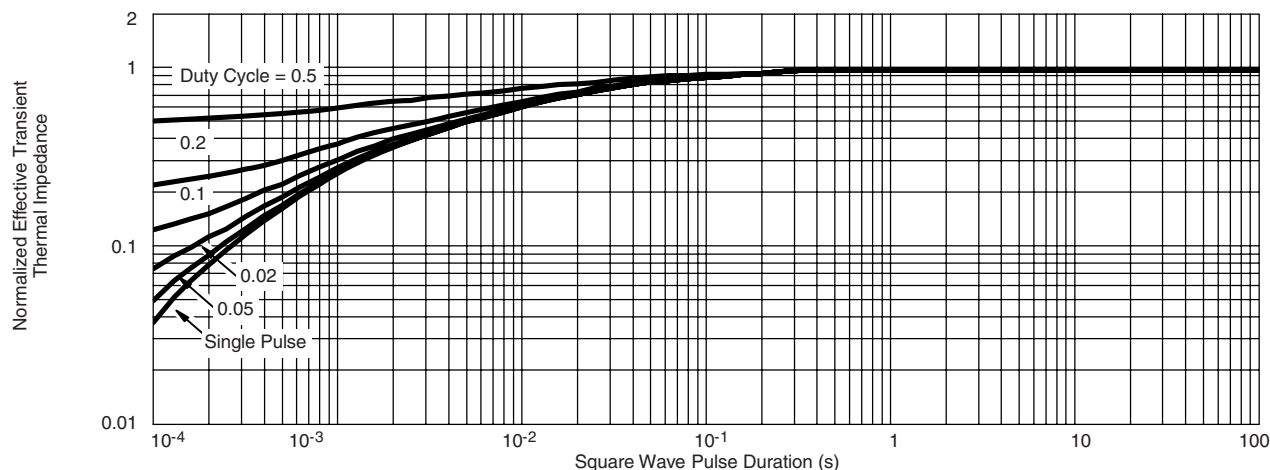
**Maximum Drain Current
vs. Ambient Temperature**



Safe Operating Area
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



Normalized Thermal Transient Impedance, Junction-to-Ambient

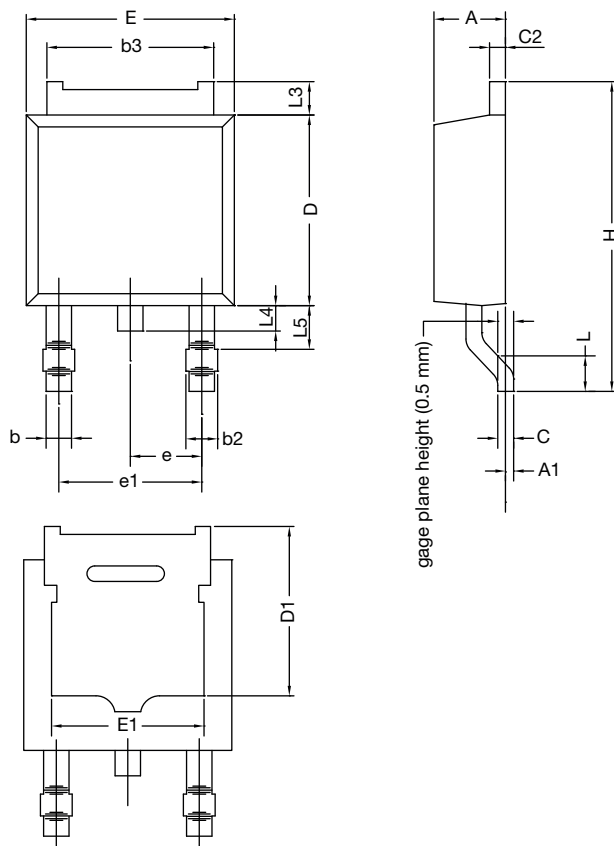


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg71856>.



TO-252AA Case Outline

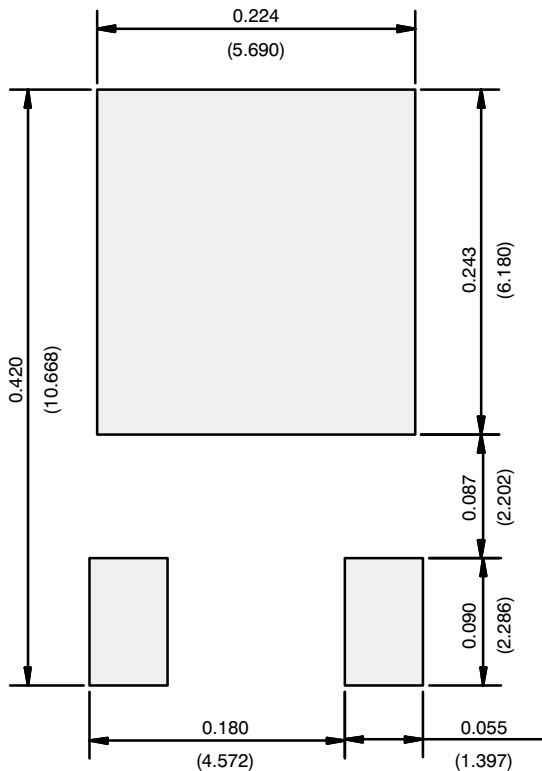


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060
ECN: T16-0236-Rev. P, 16-May-16 DWG: 5347				

Notes

- Dimension L3 is for reference only.

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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