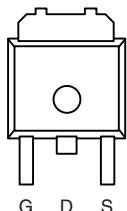


## N-Channel 100 V (D-S), 175 °C MOSFET

PRODUCT SUMMARY			
$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A) <sup>a</sup>	$Q_g$ (Typ.)
100	0.0185 at $V_{GS} = 10$ V	50	48 nC

TO-252



Drain Connected to Tab

Top View

Ordering Information: SUD50N10-18P-E3 (Lead (Pb)-free)

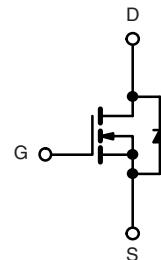
### FEATURES

- TrenchFET® Power MOSFET
- 100 %  $R_g$  and UIS Tested
- Material categorization:  
For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



### APPLICATIONS

- Primary Side Switch
- Isolated DC/DC Converter



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	$V_{DS}$	100	V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$		
Continuous Drain Current ( $T_J = 150$ °C)	$I_D$	50 <sup>a</sup> 39 8.2 <sup>b</sup> 5.8 <sup>b</sup>	A	
Pulsed Drain Current	$I_{DM}$	100		
Continuous Source-Drain Diode Current	$I_S$	50 <sup>a</sup> 2 <sup>b</sup>		
Single Pulse Avalanche Current	$I_{AS}$	45		
Avalanche Energy	$E_{AS}$	101		mJ
Maximum Power Dissipation	$P_D$	136.4 68.2 3 <sup>b</sup> 1.5 <sup>b</sup>		
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 175		°C

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b</sup>	$R_{thJA}$	40	50	°C/W
Maximum Junction-to-Case		0.85	1.1	

Notes:

a. Package limited.

b. Surface mounted on 1" x 1" FR4 board.

**SPECIFICATIONS** ( $T_J = 25^\circ\text{C}$ , unless otherwise noted)

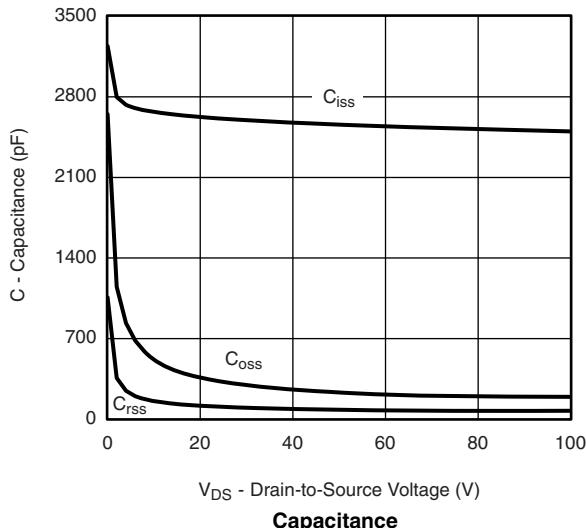
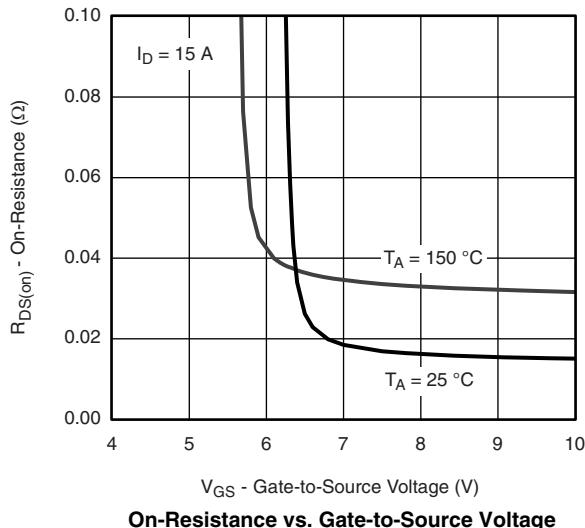
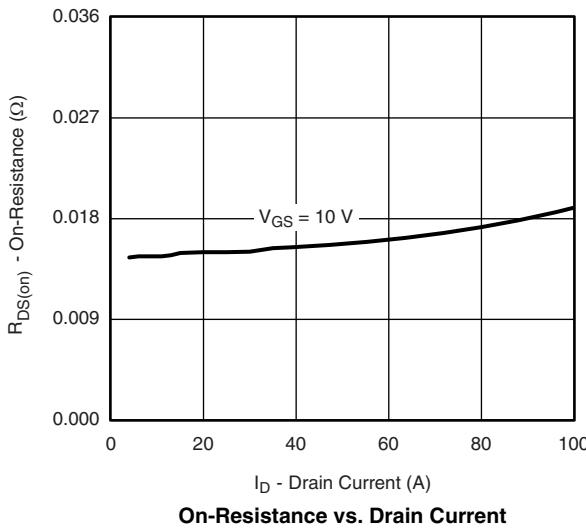
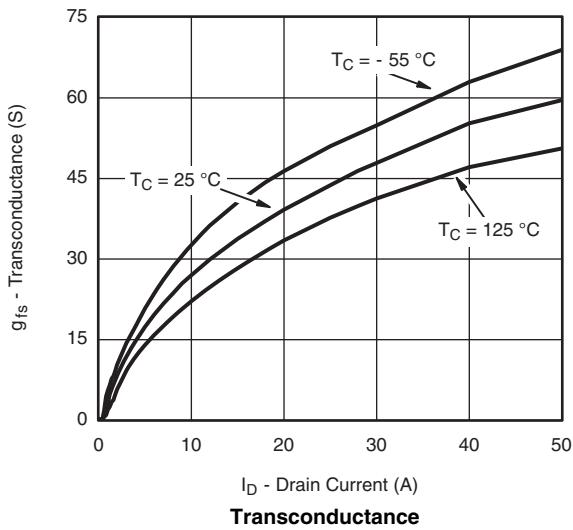
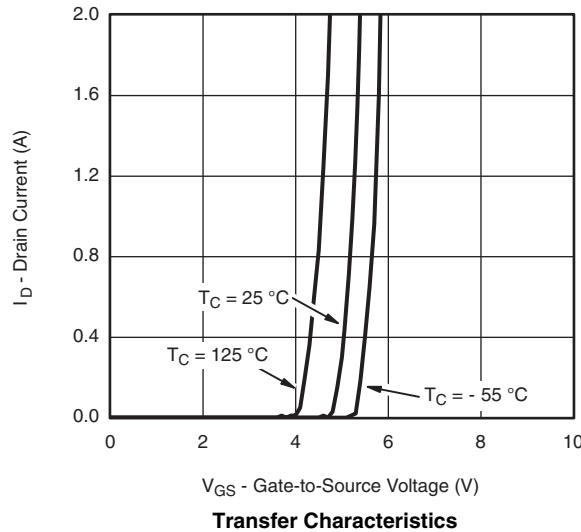
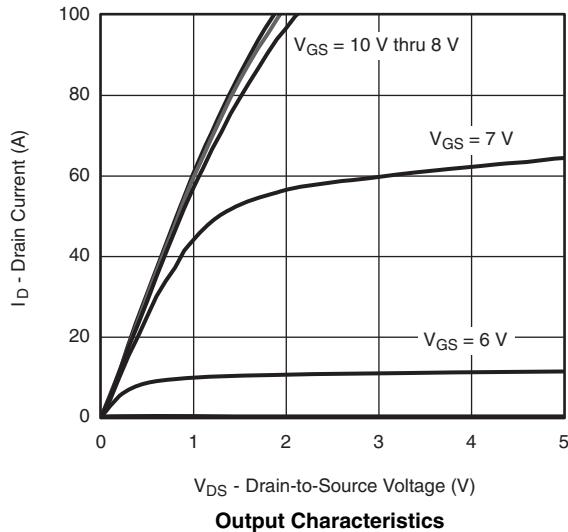
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}$ , $I_D = 250 \mu\text{A}$	100			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250 \mu\text{A}$		110		mV/°C
$V_{GS(\text{th})}$ Temperature Coefficient	$\Delta V_{GS(\text{th})}/T_J$			- 12.5		
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$ , $I_D = 250 \mu\text{A}$	2.5		5	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0 \text{ V}$ , $V_{GS} = \pm 20 \text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 100 \text{ V}$ , $V_{GS} = 0 \text{ V}$			1	μA
		$V_{DS} = 100 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $T_J = 125^\circ\text{C}$			50	
On-State Drain Current <sup>a</sup>	$I_{D(\text{on})}$	$V_{DS} \geq 5 \text{ V}$ , $V_{GS} = 10 \text{ V}$	50			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(\text{on})}$	$V_{GS} = 10 \text{ V}$ , $I_D = 15 \text{ A}$		0.015	0.0185	Ω
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15 \text{ V}$ , $I_D = 15 \text{ A}$		33		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 50 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $f = 1 \text{ MHz}$		2600		pF
Output Capacitance	$C_{oss}$			230		
Reverse Transfer Capacitance	$C_{rss}$			80		
Total Gate Charge	$Q_g$	$V_{DS} = 50 \text{ V}$ , $V_{GS} = 10 \text{ V}$ , $I_D = 50 \text{ A}$		48	75	nC
Gate-Source Charge	$Q_{gs}$			16		
Gate-Drain Charge	$Q_{gd}$			13		
Gate Resistance	$R_g$	$f = 1 \text{ MHz}$		1.6	2.5	Ω
Turn-On Delay Time	$t_{d(\text{on})}$	$V_{DD} = 50 \text{ V}$ , $R_L = 1 \Omega$ $I_D \geq 50 \text{ A}$ , $V_{GEN} = 10 \text{ V}$ , $R_g = 1 \Omega$		12	20	ns
Rise Time	$t_r$			10	20	
Turn-Off Delay Time	$t_{d(\text{off})}$			18	35	
Fall Time	$t_f$			8	15	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode	$I_S$	$T_C = 25^\circ\text{C}$			50	A
Pulse Diode Forward Current <sup>a</sup>	$I_{SM}$				100	
Body Diode Voltage	$V_{SD}$	$I_S = 15 \text{ A}$		0.85	1.5	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = 50 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $T_J = 25^\circ\text{C}$		80	120	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			160	240	nC
Reverse Recovery Fall Time	$t_a$			57		ns
Reverse Recovery Rise Time	$t_b$			23		

Notes:

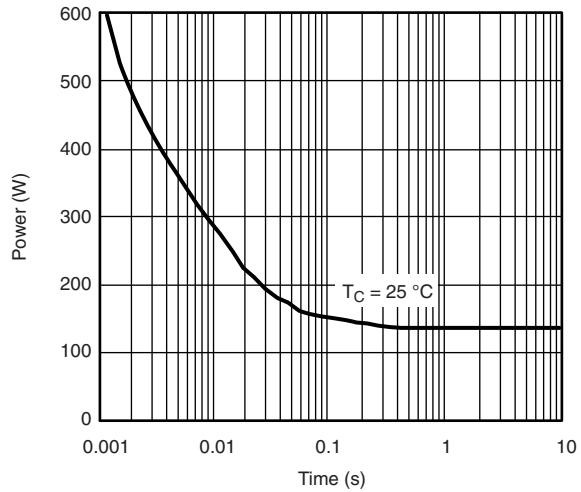
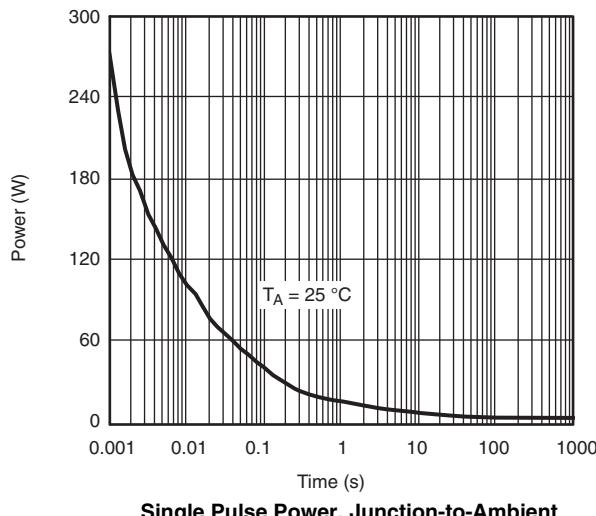
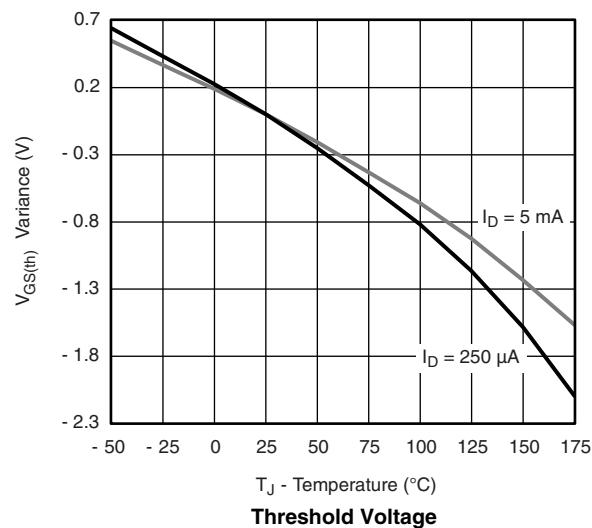
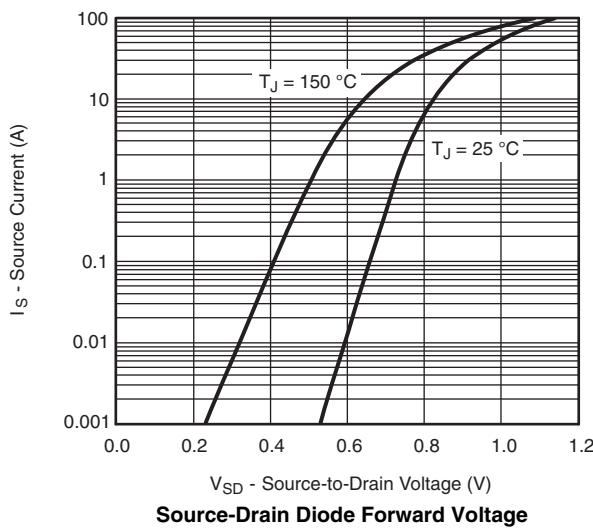
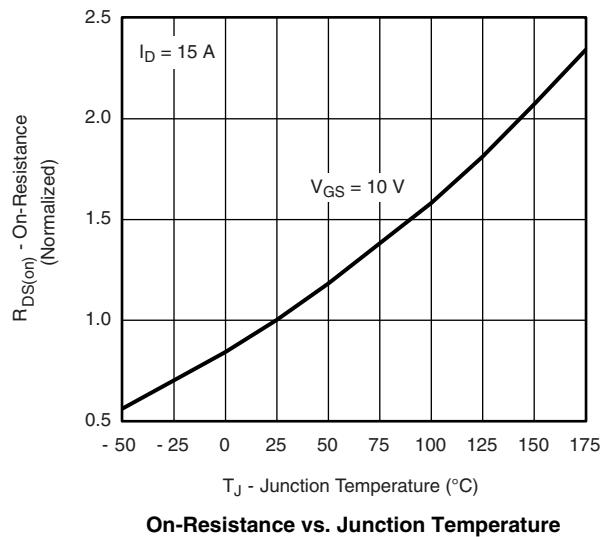
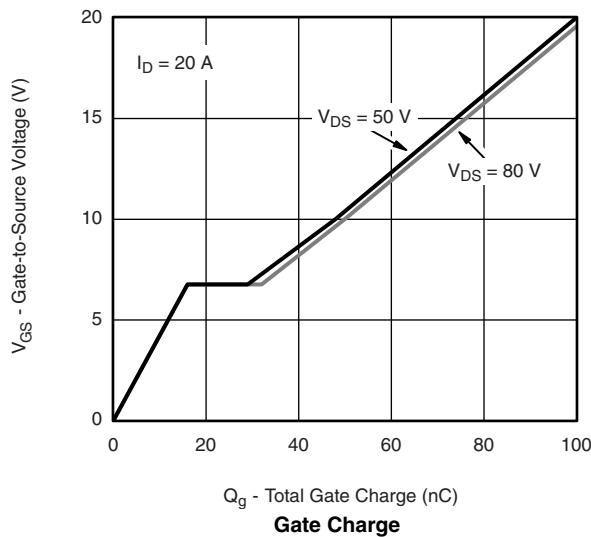
a. Pulse test; pulse width  $\leq 300 \mu\text{s}$ , duty cycle  $\leq 2\%$ .

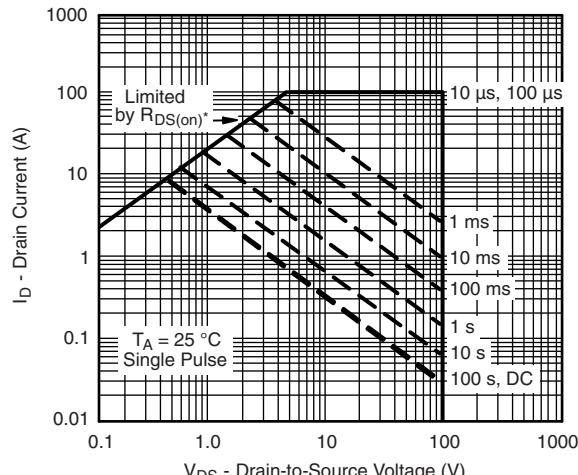
b. Guaranteed by design, not subject to production testing.

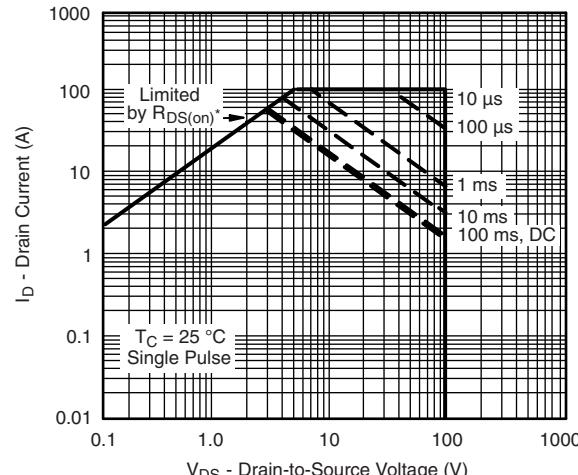
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

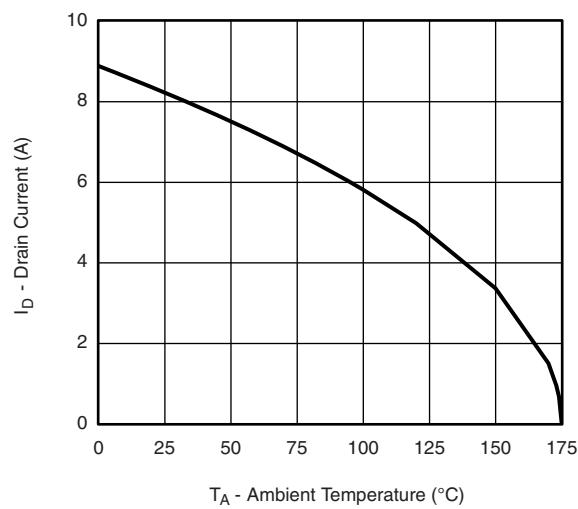
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise note)


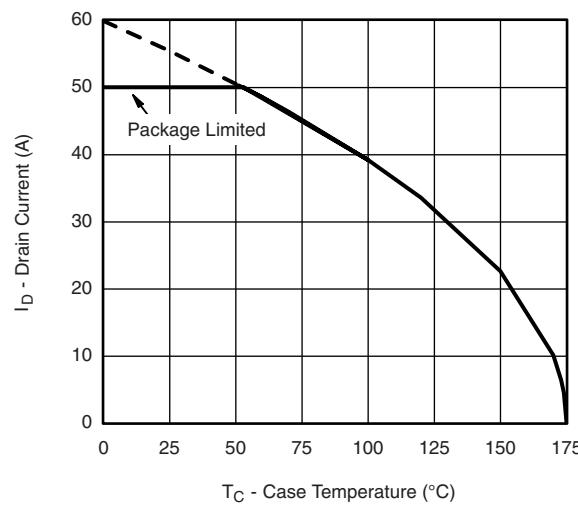
### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

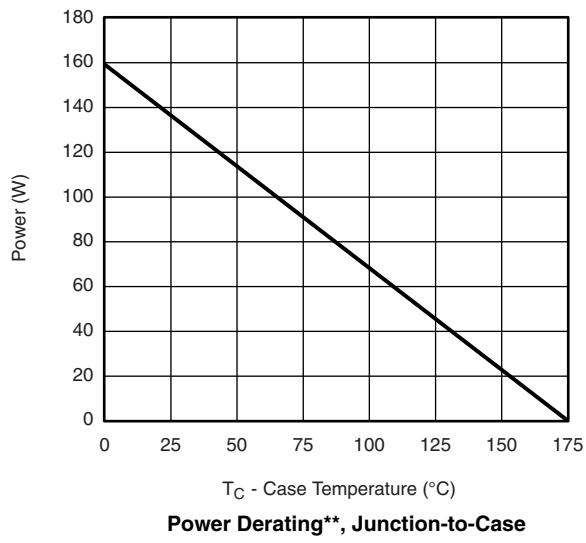
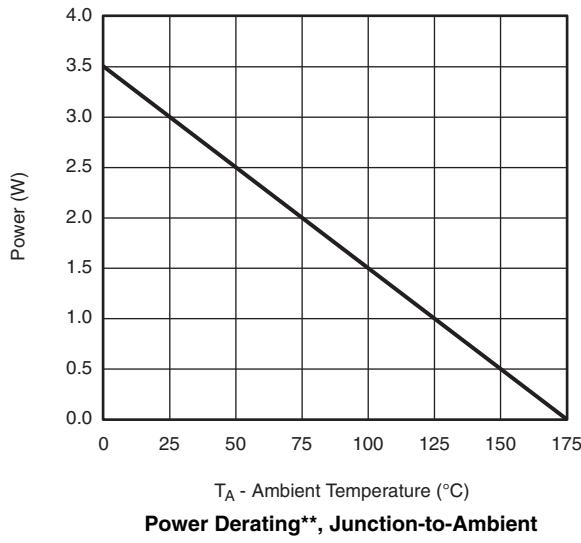
**Safe Operating Area, Junction-to-Ambient**

\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

**Safe Operating Area, Junction-to-Case**

T<sub>A</sub> - Ambient Temperature (°C)

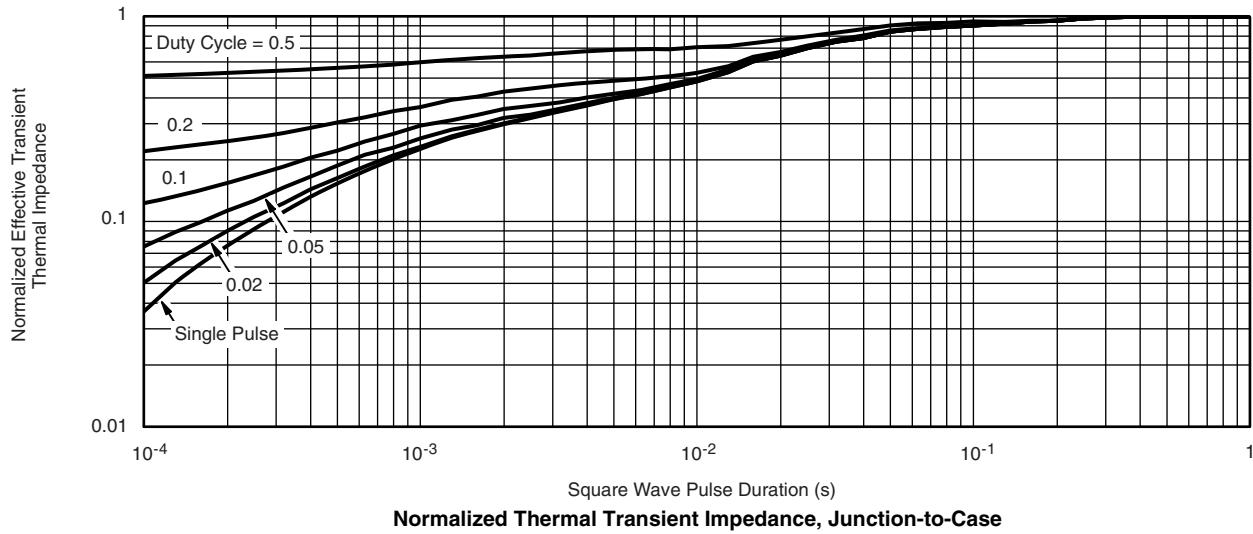
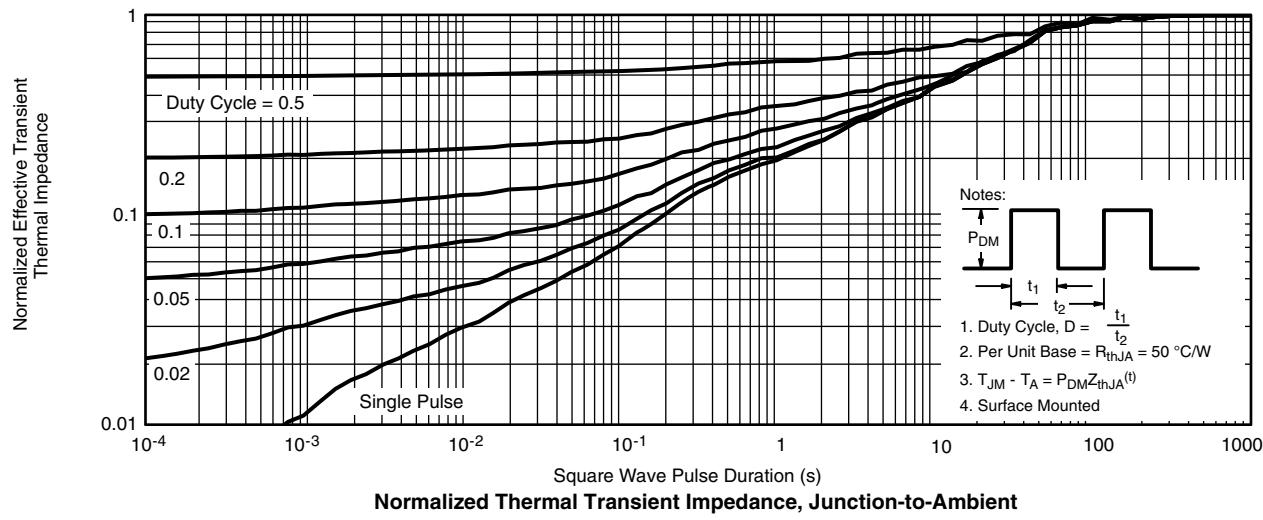
**Current Derating\*\*, Junction-to-Ambient**

T<sub>C</sub> - Case Temperature (°C)

**Current Derating\*\*, Junction-to-Case**

\*\* The power dissipation  $P_D$  is based on  $T_{J(max.)} = 175$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

\*\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 175$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)


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