

N-Channel 60-V (D-S), 175 °C MOSFET, Logic Level

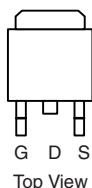
PRODUCT SUMMARY		
$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
60	0.016 at $V_{GS} = 10$ V	50
	0.022 at $V_{GS} = 4.5$ V	43

FEATURES

- TrenchFET® Power MOSFET
- 175 °C Junction Temperature


RoHS*
COMPLIANT

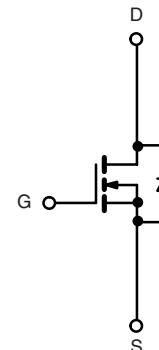
TO-263



DRAIN connected to TAB

Top View

Ordering Information: SUM50N06-16L
SUM50N06-16L-E3 (Lead (Pb)-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 175$ °C)	I_D	50	A
		35	
Pulsed Drain Current	I_{DM}	100	A
Avalanche Current	I_{AR}	40	
Repetitive Avalanche Energy ^a	E_{AR}	80	mJ
Power Dissipation	P_D	93 ^b	W
		3.7 ^c	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Junction-to-Ambient	R_{thJA}	40	°C/W
Junction-to-Case	R_{thJC}	1.6	

Notes:

a. Duty cycle ≤ 1 %.

b. See SOA curve for voltage derating.

c. Surface mounted on FR4 Board, $t \leq 10$ s.

* Pb containing terminations are not RoHS compliant, exemptions may apply.

SUM50N06-16L

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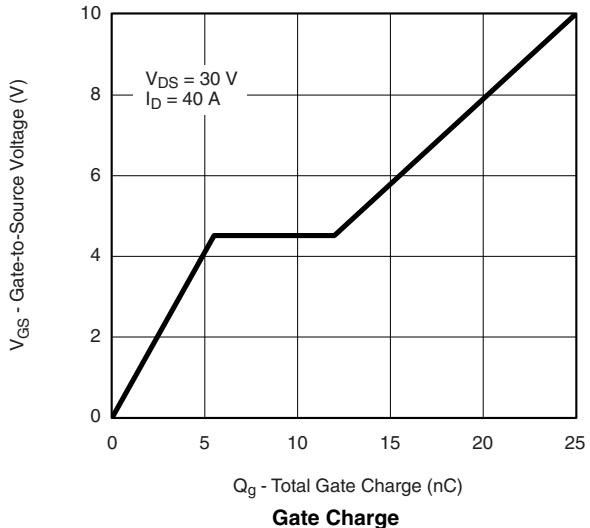
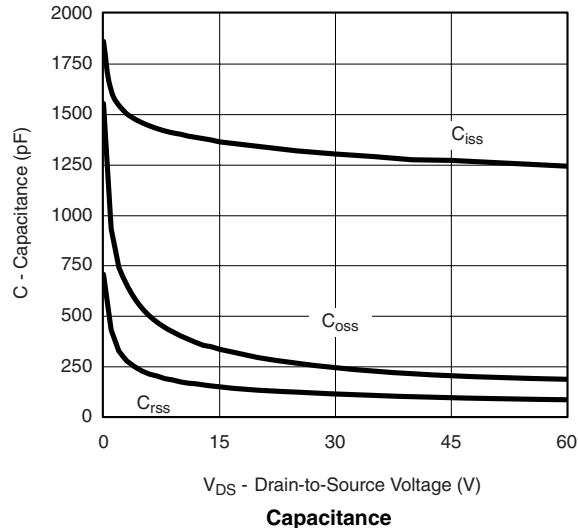
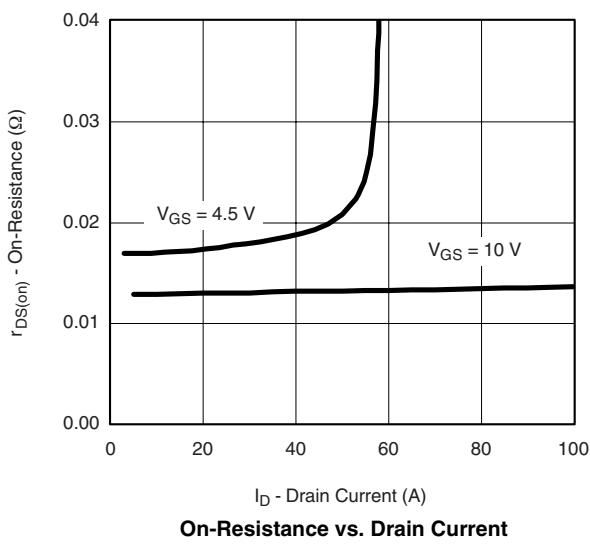
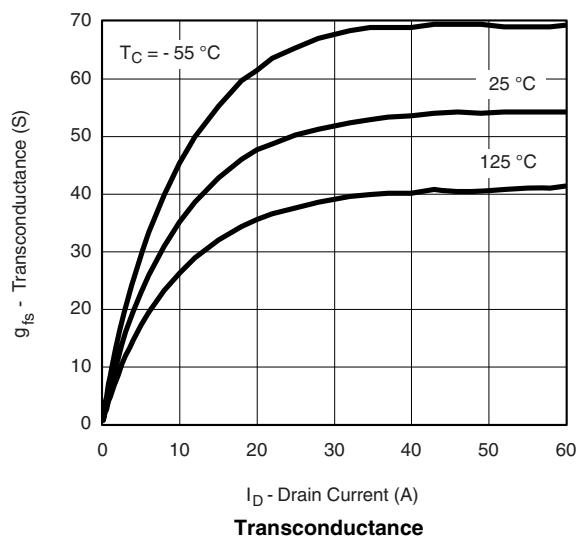
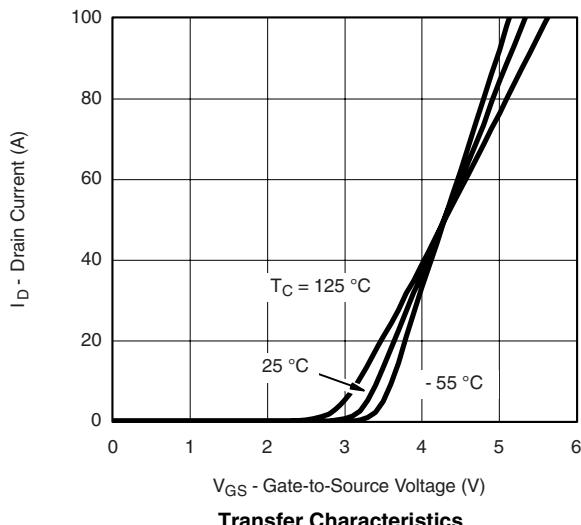
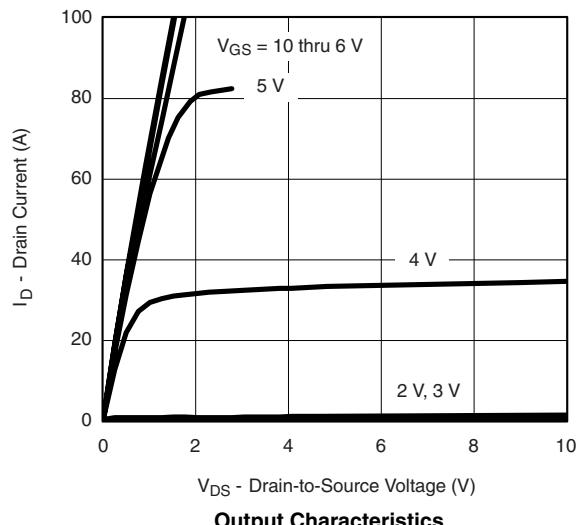
SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0 \text{ V}, I_D = 250 \mu\text{A}$	60			V
Gate-Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}} = V_{\text{GS}}, I_{\text{DS}} = 250 \mu\text{A}$	1.0	2.0	3.0	
Gate-Body Leakage	I_{GSS}	$V_{\text{DS}} = 0 \text{ V}, V_{\text{GS}} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}} = 60 \text{ V}, V_{\text{GS}} = 0 \text{ V}$			1	μA
		$V_{\text{DS}} = 60 \text{ V}, V_{\text{GS}} = 0 \text{ V}, T_J = 125^\circ\text{C}$			50	
		$V_{\text{DS}} = 60 \text{ V}, V_{\text{GS}} = 0 \text{ V}, T_J = 175^\circ\text{C}$			150	
On-State Drain Current ^a	$I_{\text{D}(\text{on})}$	$V_{\text{DS}} = 5 \text{ V}, V_{\text{GS}} = 10 \text{ V}$	50			A
Drain-Source On-State Resistance ^a	$r_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 10 \text{ V}, I_D = 20 \text{ A}$		0.013	0.016	Ω
		$V_{\text{GS}} = 10 \text{ V}, I_D = 20 \text{ A}, T_J = 125^\circ\text{C}$			0.028	
		$V_{\text{GS}} = 10 \text{ V}, I_D = 20 \text{ A}, T_J = 175^\circ\text{C}$			0.036	
		$V_{\text{GS}} = 4.5 \text{ V}, I_D = 20 \text{ A}$		0.017	0.022	
Forward Transconductance ^a	g_{fs}	$V_{\text{DS}} = 15 \text{ V}, I_D = 20 \text{ A}$		50		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{\text{GS}} = 0 \text{ V}, V_{\text{DS}} = 25 \text{ V}, f = 1 \text{ MHz}$		1325		pF
Output Capacitance	C_{oss}			265		
Reverse Transfer Capacitance	C_{rss}			115		
Total Gate Charge ^c	Q_g	$V_{\text{DS}} = 30 \text{ V}, V_{\text{GS}} = 10 \text{ V}, I_D = 50 \text{ A}$		25	40	nC
Gate-Source Charge ^c	Q_{gs}			5.5		
Gate-Drain Charge ^c	Q_{gd}			6.5		
Turn-On Delay Time ^c	$t_{\text{d}(\text{on})}$	$V_{\text{DD}} = 30 \text{ V}, R_L = 0.8 \Omega$ $I_D \approx 50 \text{ A}, V_{\text{GEN}} = 10 \text{ V}, R_G = 2.5 \Omega$		10	20	ns
Rise Time ^c	t_r			9	20	
Turn-Off Delay Time ^c	$t_{\text{d}(\text{off})}$			25	50	
Fall Time ^c	t_f			7	15	
Source-Drain Diode Ratings and Characteristics $T_C = 25^\circ\text{C}^b$						
Continuous Current	I_S				50	A
Pulsed Current	I_{SM}				100	
Forward Voltage ^a	V_{SD}	$I_F = 50 \text{ A}, V_{\text{GS}} = 0 \text{ V}$		1.0	1.5	V
Reverse Recovery Time	t_{rr}	$I_F = 50 \text{ A}, \text{di/dt} = 100 \text{ A}/\mu\text{s}$		35	70	ns
Peak Reverse Recovery Current	$I_{\text{RM}(\text{REC})}$			2.3	4	A
Reverse Recovery Charge	Q_{rr}			0.04	0.14	μC

Notes:

- a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

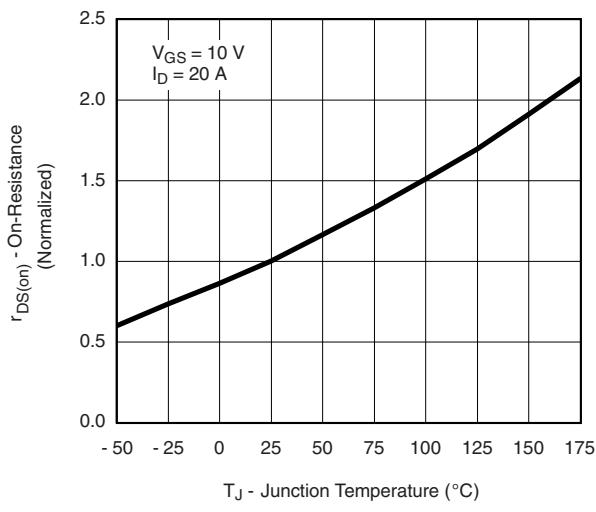
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


SUM50N06-16L

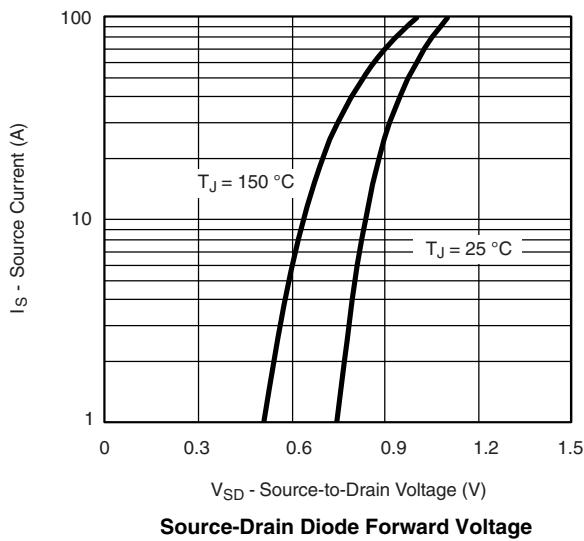
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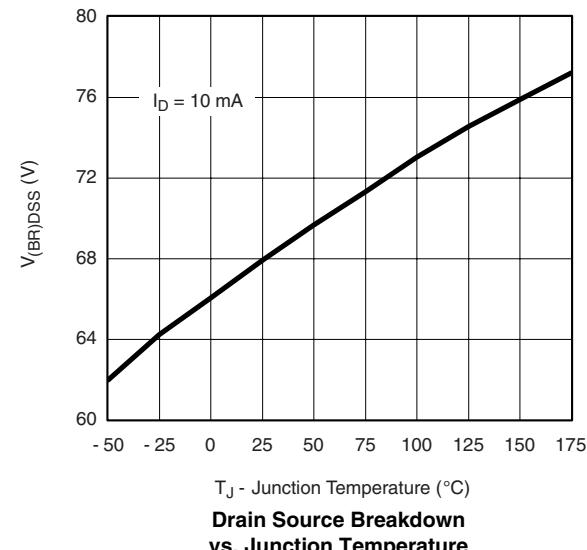
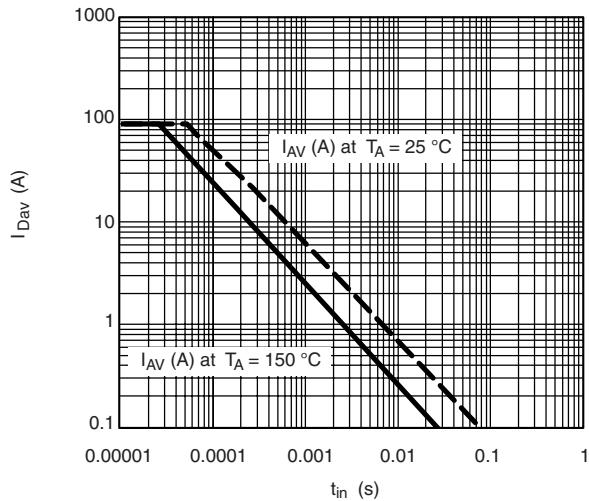
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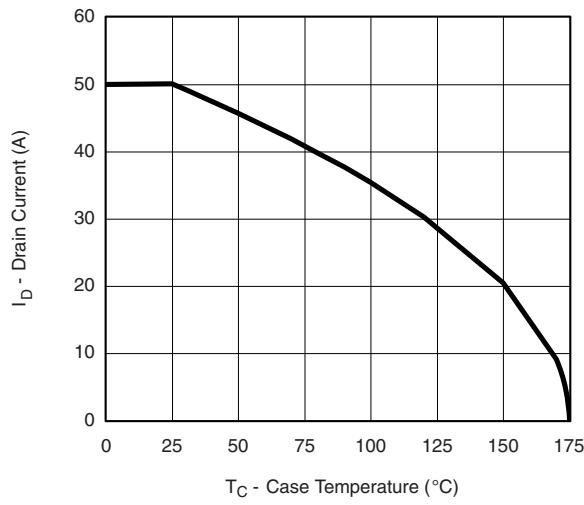
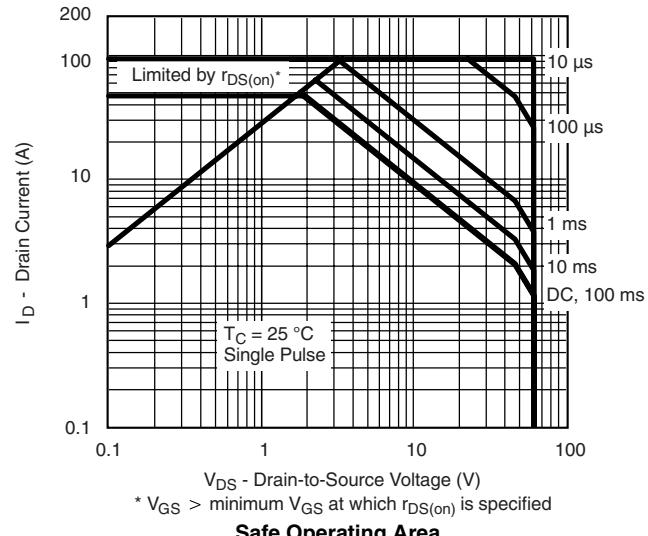
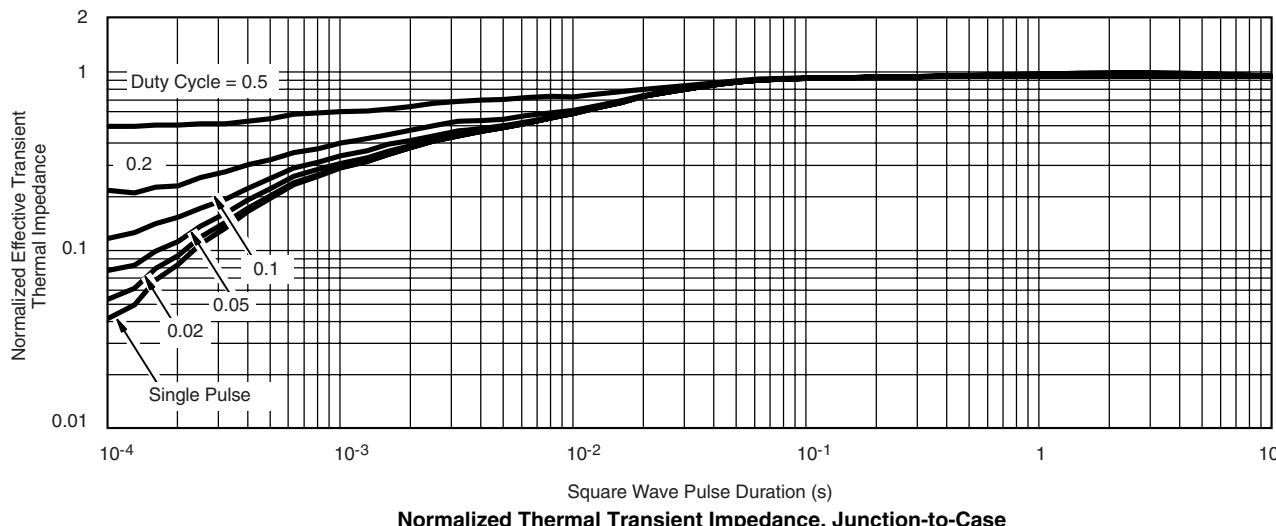
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

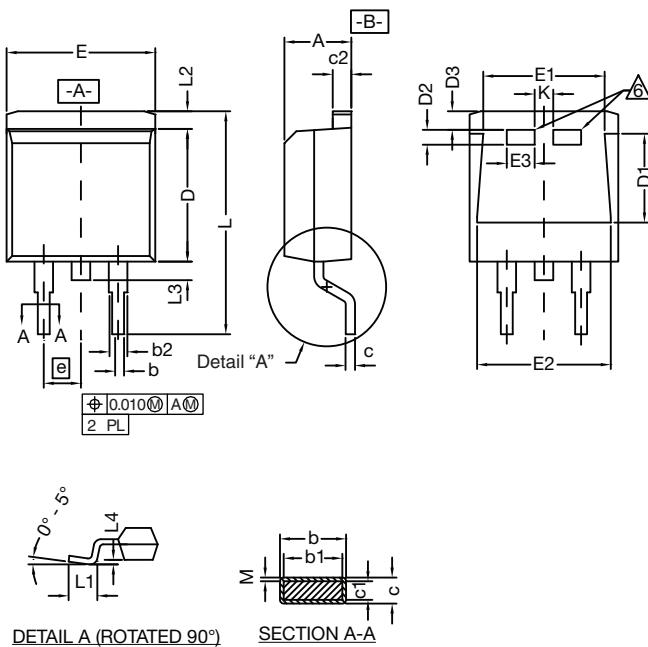


Drain Source Breakdown
vs. Junction Temperature

THERMAL RATINGS

Drain Current vs. Case Temperature

Safe Operating Area

Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?72048>.

TO-263 (D²PAK): 3-LEAD



DIM.	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	0.160	0.190	4.064	4.826	
b	0.020	0.039	0.508	0.990	
b1	0.020	0.035	0.508	0.889	
b2	0.045	0.055	1.143	1.397	
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2	0.045	0.055	1.143	1.397	
D	0.340	0.380	8.636	9.652	
D1	0.220	0.240	5.588	6.096	
D2	0.038	0.042	0.965	1.067	
D3	0.045	0.055	1.143	1.397	
E	0.380	0.410	9.652	10.414	
E1	0.245	-	6.223	-	
E2	0.355	0.375	9.017	9.525	
E3	0.072	0.078	1.829	1.981	
e	0.100 BSC		2.54 BSC		
K	0.045	0.055	1.143	1.397	
L	0.575	0.625	14.605	15.875	
L1	0.090	0.110	2.286	2.794	
L2	0.040	0.055	1.016	1.397	
L3	0.050	0.070	1.270	1.778	
L4	0.010 BSC		0.254 BSC		
M	-	0.002	-	0.050	

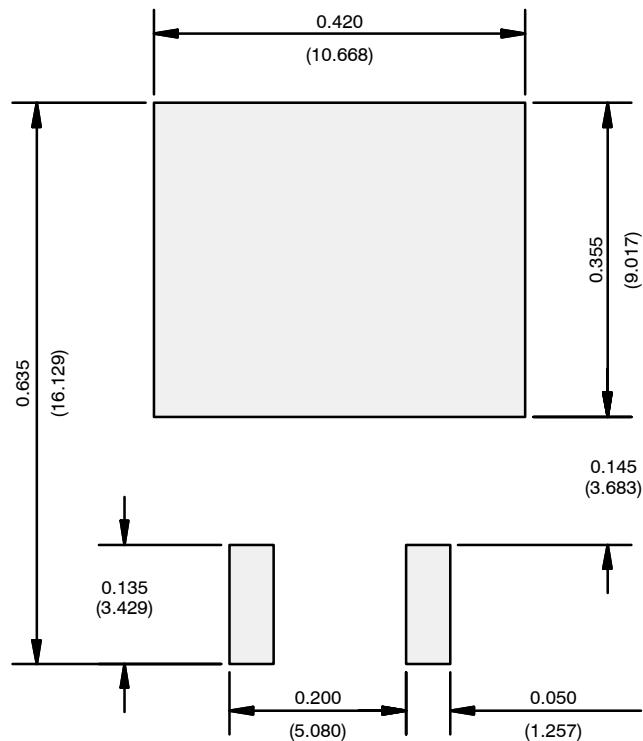
ECN: T10-0738-Rev. J, 03-Jan-11

DWG: 5843

Notes

1. Plane B includes maximum features of heat sink tab and plastic.
2. No more than 25 % of L1 can fall above seating plane by max. 8 mils.
3. Pin-to-pin coplanarity max. 4 mils.
4. *: Thin lead is for SUB, SYB.
Thick lead is for SUM, SYM, SQM.
5. Use inches as the primary measurement.

 This feature is for thick lead.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead

Recommended Minimum Pads
Dimensions in Inches/(mm)

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