



N-Channel 60-V (D-S) MOSFET

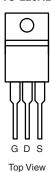
PRODUCT SUMMARY				
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A)	Q _g (Typ.)	
60	0.012 at V _{GS} = 10 V	60 ^d	33	

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- 100 % R_g Tested 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC

COMPLIANT HALOGEN FREE

TO-220AB

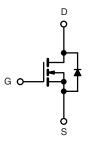


Ordering Information: SUP60N06-12P-E3 (Lead (Pb)-free)

SUP60N06-12P-GE3 (Lead (Pb)-free and Halogen-free)

APPLICATIONS

- Synchronous Rectifier
- **Power Supplies**



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS	$T_C = 25 ^{\circ}C$, unless oth	erwise noted			
Parameter	Symbol	Limit	Unit		
Drain-Source Voltage	V _{DS}	60	٧		
Gate-Source Voltage		V _{GS}	± 20	- V	
Continuous Drain Current (T _{.1} = 150 °C)	T _C = 25 °C	I-	60 ^d		
Continuous Diam Curient (1) = 130 C)	T _C = 70 °C		54 ^d	Α	
Pulsed Drain Current		I _{DM}	80	- A	
Avalanche Current		I _{AS}	40		
Single Avalanche Energy ^a	L = 0.1 mH	E _{AS}	80	mJ	
	T _C = 25 °C	В	100 ^b	W	
Maximum Power Dissipation ^a	T _A = 25 °C ^c	$ P_D$ $-$	3.25		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Limit	Unit	
Junction-to-Ambient (PCB Mount) ^c	R _{thJA}	40	- °C/W	
Junction-to-Case (Drain)	R _{thJC}	1.25		

Notes:

- a. Duty cycle \leq 1 %.
- b. See SOA curve for voltage derating.
- c. When Mounted on 1" square PCB (FR-4 material).
- d. Package limited.

SUP60N06-12P

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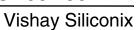


SPECIFICATIONS $T_J = 25$ °	C, unless of	therwise noted				
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{DS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$	60			V
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2.5		4.5	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 250	nA
Zero Gate Voltage Drain Current		$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$			1	
	I _{DSS}	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 125 ^{\circ}\text{C}$			50	μΑ
		V _{DS} = 60 V, V _{GS} = 0 V, T _J = 150 °C			250	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 10 \text{ V}, V_{GS} = 10 \text{ V}$	80			Α
Drain-Source On-State Resistance ^a	В	V _{GS} = 10 V, I _D = 30 A		0.0098	0.012	Ω
	R _{DS(on)}	V _{GS} = 10 V, I _D = 30 A, T _J = 125 °C		0.0155	0.019	
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 15 A		37		S
Dynamic ^b						
Input Capacitance	C _{iss}			1970		pF
Output Capacitance	C _{oss}	$V_{GS} = 0 \text{ V}, V_{DS} = 30 \text{ V}, f = 1 \text{ MHz}$		310		
Reverse Transfer Capacitance	C _{rss}			110		
Total Gate Charge ^c	Q_g			33	55	nC
Gate-Source Charge ^c	Q_{gs}	$V_{DS} = 30 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$		11		
Gate-Drain Charge ^c	Q_{gd}			9		
Gate Resistance	R_{g}	f = 1 MHz	0.3	1.4	2.8	Ω
Turn-On Delay Time ^c	t _{d(on)}			11	20	
Rise Time ^c	t _r	V_{DD} = 30 V, R_L = 1.53 Ω $I_D \cong$ 20 A, V_{GEN} = 10 V, R_g = 1 Ω		11	20	ns ns
Turn-Off Delay Time ^c	t _{d(off)}			16	30	
Fall Time ^c	t _f			8	15	
Source-Drain Diode Ratings and Cha	aracteristics 7	_C = 25 °C ^b	•			
Continuous Current	Is				60	А
Pulsed Current	I _{SM}				80	
Forward Voltage ^a	V _{SD}	I _F = 10 A, V _{GS} = 0 V		0.84	1.5	V
Reverse Recovery Time	t _{rr}	I _F = 10 A, dl/dt = 100 A/μs		40	80	ns
Peak Reverse Recovery Current	I _{RM(REC)}			3.2	5.0	Α
Reverse Recovery Charge	Q _{rr}	·		64	120	nC

Notes:

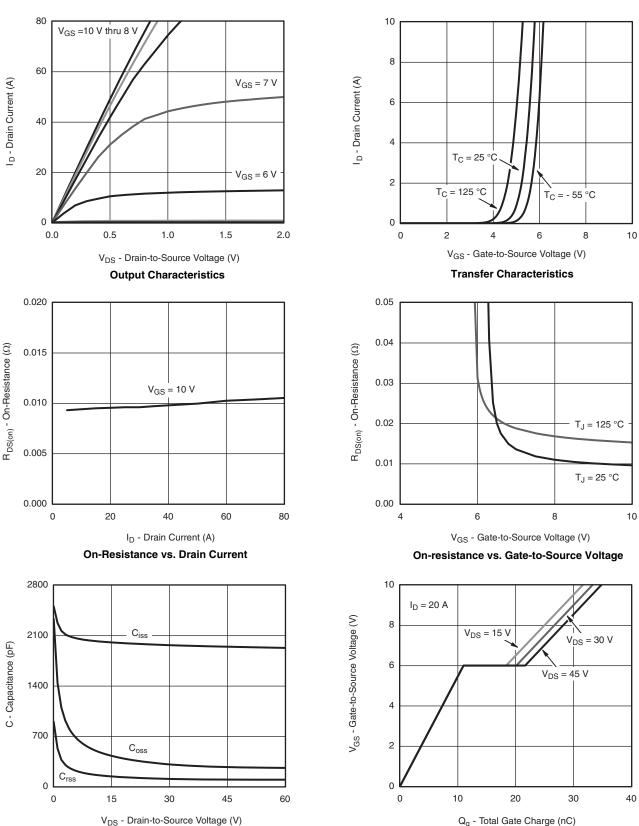
- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.





TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



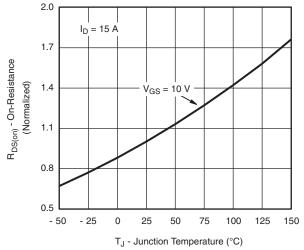
Capacitance

Gate Charge

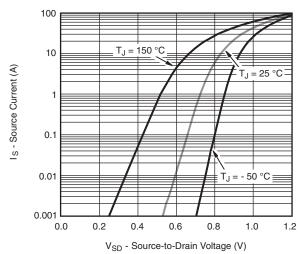
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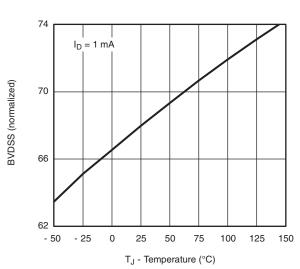
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



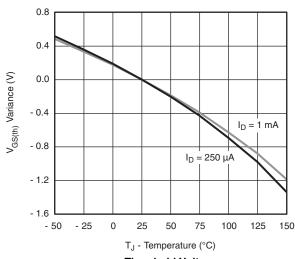
On-Resistance vs. Junction Temperature



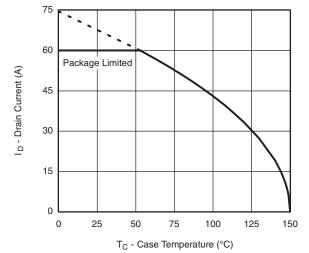
Source-Drain Diode Forward Voltage



Drain-Source Breakdown vs. Junction Temperature



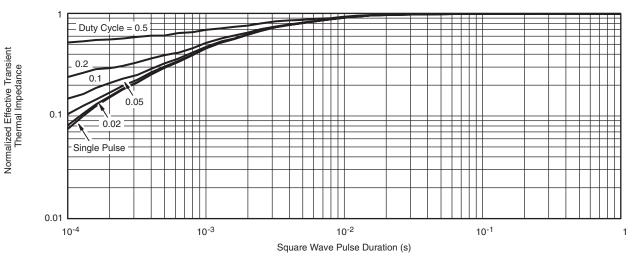
Threshold Voltage



Maximum Drain Current vs. Case Temperature

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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?69070.



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