

General Description

The SX1210 is a low cost single-chip receiver operating in the frequency ranges from 863-870, 902-928 MHz and 950-960 MHz. The SX1210 is optimized for very low power consumption (3mA). It incorporates a baseband demodulator with data rates up to 200 kb/s. Data handling features include a sixty-four byte FIFO, packet handling, CRC and data whitening processing. Its highly integrated architecture allows for minimum external component count whilst maintaining design flexibility. All major RF communication parameters are programmable and most of them may be dynamically set. It complies with European (ETSI EN 300-220 V2.1.1) and North American (FCC part 15.247 and 15.249) regulatory standards.

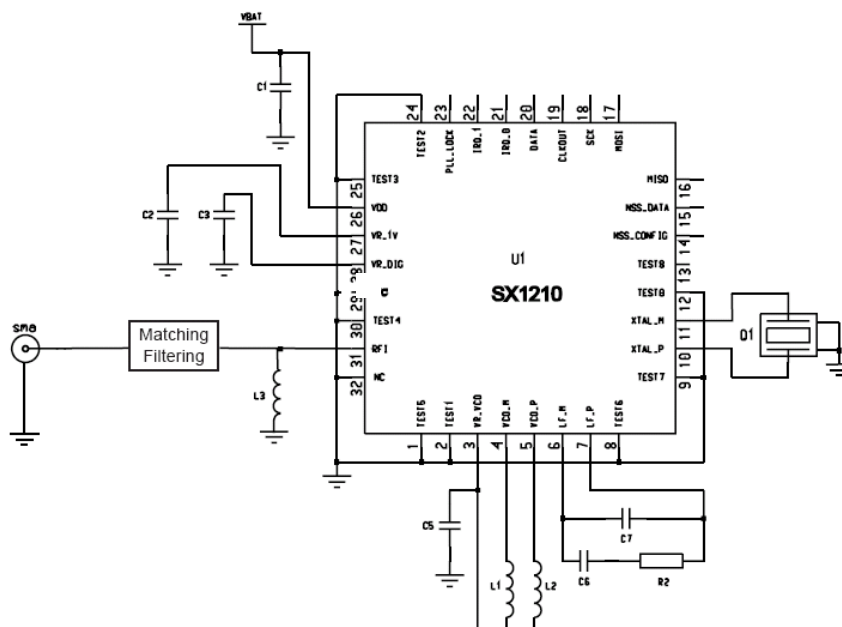
Ordering Information

Table 1: Ordering Information

Part number	Delivery	Minimum Order Quantity / Multiple
SX1210I084TRT	Tape & Reel	3000 pieces

- TQFN-32 package – Operating range [-40;+85°C]
- T refers to Lead Free packaging
- This device is WEEE and RoHS compliant

Application Circuit Schematic



Features

- Low Rx power consumption: 3mA
- Good reception sensitivity: down to -107 dBm at 25 kb/s in FSK, -113 dBm at 2kb/s in OOK
- Packet handling feature with data whitening and CRC processing
- RSSI (Received Signal Strength Indicator) range from Rx noise floor to 0 dBm
- Bit rates up to 200 kb/s, NRZ coding
- On-chip frequency synthesizer
- FSK and OOK modulation
- Incoming sync word recognition
- Built-in Bit-Synchronizer for incoming data and clock synchronization and recovery
- 5 x 5 mm TQFN package
- Optimized Circuit Configuration for Low-cost applications
- Pin to pin compatible with SX1211 Transceiver

Applications

- Wireless alarm and security systems
- Wireless sensor networks
- Automated Meter Reading
- Home and building automation
- Industrial monitoring and control
- Remote Wireless Control

Table of Contents

1. General Description	5	5.3.4. uC Connections	37
1.1. Simplified Block Diagram	5	5.3.5. Continuous Mode Example	37
1.2. Pin Diagram	6	5.4. Buffered Mode	38
1.3. Pin Description	7	5.4.1. General Description	38
2. Electrical Characteristics	8	5.4.2. Rx Processing	38
2.1. ESD Notice	8	5.4.3. Interrupt Signals Mapping	39
2.2. Absolute Maximum Ratings	8	5.4.4. uC Connections	40
2.3. Operating Range	8	5.4.5. Buffered Mode Example	40
2.4. Chip Specification	8	5.5. Packet Mode	41
2.4.1. Power Consumption	8	5.5.1. General Description	41
2.4.2. Frequency Synthesis	9	5.5.2. Packet Format	41
2.4.3. Receiver	10	5.5.3. Rx Processing	43
2.4.4. Digital Specification	11	5.5.4. Packet Filtering	43
3. Architecture Description	12	5.5.5. DC-Free Data Mechanisms	45
3.1. Power Supply Strategy	12	5.5.6. Interrupt Signal Mapping	46
3.2. Frequency Synthesis Description	13	5.5.7. uC Connections	46
3.2.1. Reference Oscillator	13	5.5.8. Packet Mode Example	48
3.2.2. CLKOUT Output	13	5.5.9. Additional Information	48
3.2.3. PLL Architecture	14	6. Configuration and Status Registers	49
3.2.4. PLL Tradeoffs	14	6.1. General Description	49
3.2.5. Voltage Controlled Oscillator	15	6.2. Main Configuration Register - MCPParam	49
3.2.6. PLL Loop Filter	15	6.3. Interrupt Configuration Parameters - IRQParam	51
3.2.7. PLL Lock Detection Indicator	16	6.4. Receiver Configuration parameters - RXParam	53
3.2.8. Frequency Calculation	16	6.5. Sync Word Parameters - SYNCParam	54
3.3. Receiver Description	17	6.6. Oscillator Parameters - OSCParam	55
3.3.1. Architecture	17	6.7. Packet Handling Parameters - PKTPParam	56
3.3.2. LNA and First Mixer	18	7. Application Information	57
3.3.3. IF Gain and Second I/Q Mixer	18	7.1. Crystal Resonator Specification	57
3.3.4. Channel Filters	18	7.2. Software for Frequency Calculation	57
3.3.5. Channel Filters Setting in FSK Mode	19	7.2.1. GUI	57
3.3.6. Channel Filters Setting in OOK Mode	20	7.2.2. .dll for Automatic Production Bench	57
3.3.7. RSSI	20	7.3. Switching Times and Procedures	57
3.3.8. Fdev Setting in Receive Mode	22	7.3.1. Optimized Receive Cycle	58
3.3.9. FSK Demodulator	22	7.3.2. Receiver Frequency Hop Optimized Cycle	59
3.3.10. OOK Demodulator	22	7.4. Reset of the Chip	60
3.3.11. Bit Synchronizer	25	7.4.1. POR	60
3.3.12. Alternative Settings	26	7.4.2. Manual Reset	60
3.3.13. Data Output	26	7.5. Reference Design	61
4. Operating Modes	27	7.5.1. Application Schematic	61
4.1. Modes of Operation	27	7.5.2. PCB Layout	61
4.2. Digital Pin Configuration vs. Chip Mode	27	7.5.3. Bill Of Material	62
5. Data Processing	28	7.5.4. Ordering Information for Tools	63
5.1. Overview	28	7.6. Reference Design Performance	63
5.1.1. Block Diagram	28	7.6.1. Sensitivity Flatness	65
5.1.2. Data Operation Modes	28	7.6.2. Sensitivity vs. LO Drift	66
5.2. Control Block Description	29	7.6.3. Sensitivity vs. Receiver BW	67
5.2.1. SPI Interface	29	7.6.4. Sensitivity Stability over Temperature and Voltage	68
5.2.2. FIFO	31	7.6.5. Sensitivity vs. Bit Rate	68
5.2.3. Sync Word Recognition	33	7.6.6. Adjacent Channel Rejection	69
5.2.4. Packet Handler	34	8. Packaging Information	71
5.2.5. Control	34	8.1. Package Outline Drawing	71
5.3. Continuous Mode	35	8.2. PCB Land Pattern	71
5.3.1. General Description	35	8.3. Tape & Reel Specification	72
5.3.2. Rx Processing	36	9. Revision History	73
5.3.3. Interrupt Signals Mapping	36	10. Contact Information	73

Index of Figures

Figure 1: SX1210 Simplified Block Diagram	5	Figure 31: Rx Processing in Buffered Mode (FIFO size=16, Fifo_fill_method=0)	39
Figure 2: SX1210 Pin Diagram	6	Figure 32: uC Connections in Buffered Mode	40
Figure 3: SX1210 Detailed Block Diagram	12	Figure 33: Packet Mode Conceptual View	41
Figure 4: Power Supply Breakdown	13	Figure 34: Fixed Length Packet Format	42
Figure 5: Frequency Synthesizer Description	14	Figure 35: Variable Length Packet Format	43
Figure 6: LO Generator	14	Figure 36: CRC Implementation	45
Figure 7: Loop Filter	16	Figure 37: Manchester Decoding	45
Figure 8: Receiver Architecture	17	Figure 38: Data Whitening Implementation	46
Figure 9: FSK Receiver Setting	17	Figure 39: uC Connections in Packet Mode	46
Figure 10: OOK Receiver Setting	17	Figure 40: Optimized Rx Cycle	58
Figure 11: Active Channel Filter Description	18	Figure 41: Rx Hop Cycle	59
Figure 12: Butterworth Filter's Actual BW	20	Figure 42: POR Timing Diagram	60
Figure 13: Polyphase Filter's Actual BW	20	Figure 43: Manual Reset Timing Diagram	60
Figure 14: RSSI Dynamic Range	21	Figure 44: Reference Design Circuit Schematic	61
Figure 15: RSSI IRQ Timings	22	Figure 45: Reference Design's Stackup	62
Figure 16: OOK Demodulator Description	23	Figure 46: Reference Design Layout (top view)	62
Figure 17: Floor Threshold Optimization	24	Figure 49: Sensitivity Across the 868 MHz Band	65
Figure 18: BitSync Description	25	Figure 50: Sensitivity Across the 915 MHz Band	65
Figure 19: SX1210's Data Processing Conceptual View	28	Figure 51: FSK Sensitivity Loss vs. LO Drift	66
Figure 20: SPI Interface Overview and uC Connections	29	Figure 52: OOK Sensitivity Loss vs. LO Drift	66
Figure 21: Write Register Sequence	30	Figure 53: FSK Sensitivity vs. Rx BW	67
Figure 22: Read Register Sequence	31	Figure 54: OOK Sensitivity Change vs. Rx BW	67
Figure 23: Read Bytes Sequence (ex: 2 bytes)	31	Figure 55: Sensitivity Stability	68
Figure 24: FIFO and Shift Register (SR)	32	Figure 56: FSK Sensitivity vs. BR	68
Figure 25: FIFO Threshold IRQ Source Behavior	33	Figure 57: OOK Sensitivity vs. BR	69
Figure 26: Sync Word Recognition	33	Figure 58: ACR in FSK Mode	69
Figure 27: Continuous Mode Conceptual View	35	Figure 59: ACR in OOK Mode	70
Figure 28: Rx Processing in Continuous Mode	36	Figure 60: Package Outline Drawing	71
Figure 29: uC Connections in Continuous Mode	37	Figure 61: PCB Land Pattern	71
Figure 30: Buffered Mode Conceptual View	38	Figure 62: Tape & Reel Dimensions	72

Index of Tables

Table 1: Ordering Information	1	Table 18: Relevant Configuration Registers in Buffered Mode (data processing related only)	40
Table 2: SX1210 Pinouts	7	Table 19: Interrupt Mapping in Rx and Stby in Packet Mode	46
Table 3: Absolute Maximum Ratings	8	Table 20: Relevant Configuration Registers in Packet Mode (data processing related only)	48
Table 4: Operating Range	8	Table 21: Registers List	49
Table 5: Power Consumption Specification	8	Table 22: MCPParam Register Description	49
Table 6: Frequency Synthesizer Specification	9	Table 23: IRQParam Register Description	51
Table 7: Receiver Specification	10	Table 24: RXParam Register Description	53
Table 8: Digital Specification	11	Table 25: SYNCParam Register Description	54
Table 9: MCPParam_Freq_band Setting	15	Table 26: OSCParam Register Description	55
Table 10: Operating Modes	27	Table 27: PKTPParam Register Description	56
Table 11: Pin Configuration vs. Chip Mode	27	Table 28: Crystal Resonator Specification	57
Table 12: Data Operation Mode Selection	29	Table 29: Reference Design BOM	62
Table 13: Config vs. Data SPI Interface Selection	30	Table 30: Tools Ordering Information	63
Table 14: Status of FIFO when Switching Between Different Modes of the Chip	33	Table 31: FSK Rx Filters vs. Bit Rate	63
Table 15: Interrupt Mapping in Continuous Rx Mode	36	Table 32: OOK Rx Filters vs. Bit Rate	64
Table 16: Relevant Configuration Registers in Continuous Mode (data processing related only)	37		
Table 17: Interrupt Mapping in Buffered Rx and Stby Modes	39		

Acronyms

BOM	Bill Of Materials	LO	Local Oscillator
BR	Bit Rate	LSB	Least Significant Bit
BW	Bandwidth	MSB	Most Significant Bit
CCITT	Comité Consultatif International Téléphonique et Télégraphique - ITU	NRZ	Non Return to Zero
CP	Charge Pump	NZIF	Near Zero Intermediate Frequency
CRC	Cyclic Redundancy Check	OOK	On Off Keying
DAC	Digital to Analog Converter	PA	Power Amplifier
DDS	Direct Digital Synthesis	PCB	Printed Circuit Board
DLL	Dynamically Linked Library	PFD	Phase Frequency Detector
ERP	Equivalent Radiated Power	PLL	Phase-Locked Loop
ETSI	European Telecommunications Standards Institute	POR	Power On Reset
FCC	Federal Communications Commission	RBW	Resolution BandWidth
Fdev	Frequency Deviation	RF	Radio Frequency
FIFO	First In First Out	RSSI	Received Signal Strength Indicator
FS	Frequency Synthesizer	Rx	Receiver
FSK	Frequency Shift Keying	SAW	Surface Acoustic Wave
GUI	Graphical User Interface	SPI	Serial Peripheral Interface
IC	Integrated Circuit	SR	Shift Register
ID	IDentificator	Stby	Standby
IF	Intermediate Frequency	Tx	Transmitter
IRQ	Interrupt ReQuest	uC	Microcontroller
ITU	International Telecommunication Union	VCO	Voltage Controlled Oscillator
LFSR	Linear Feedback Shift Register	XO	Crystal Oscillator
LNA	Low Noise Amplifier	XOR	eXclusive OR

This product datasheet contains a detailed description of the SX1210 performance and functionality. Please consult the Semtech website for the latest updates or errata.

1. General Description

The SX1210 is a single chip FSK and OOK receiver capable of operation in the 863-870 MHz and 902-928 MHz license free ISM frequency bands, as well as the 950 - 960 MHz frequency band. It complies with both the relevant European and North American standards, EN 300-220 V2.1.1 (June 2006 release) and FCC Part 15 (10-1-2006 edition). A unique feature of this circuit is its extremely low current consumption in full active mode of only 3mA (typ). The SX1210 is available in a 5x5 mm TQFN-32 package.

1.1. Simplified Block Diagram

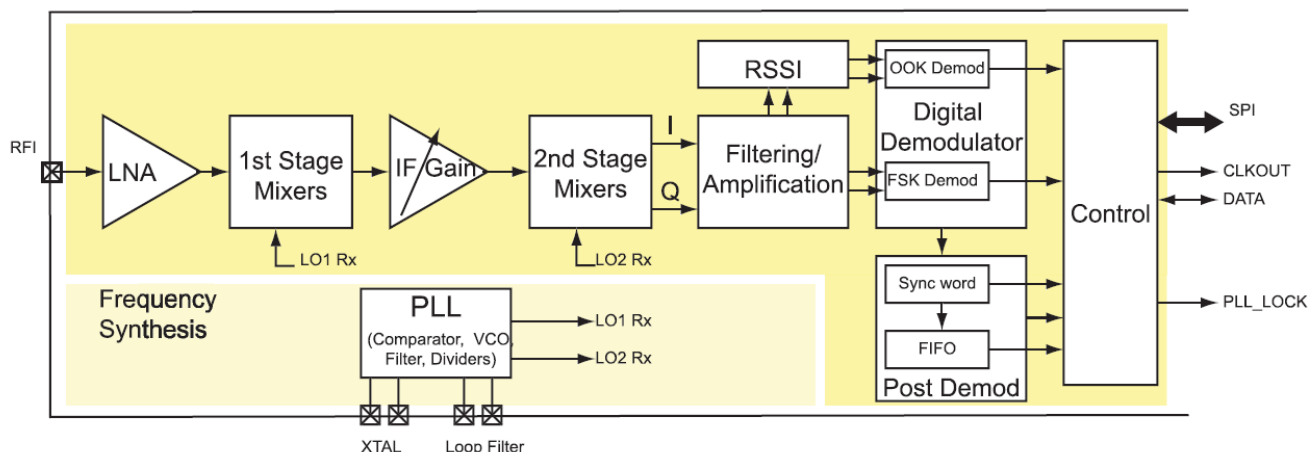


Figure 1: SX1210 Simplified Block Diagram

1.2. Pin Diagram

The following diagram shows the pins arrangement of the QFN package, top view.

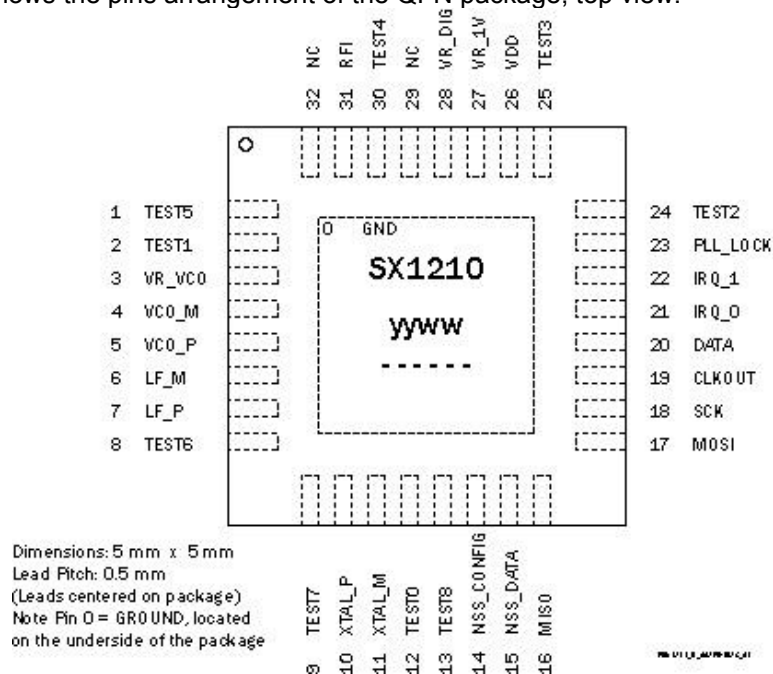


Figure 2: SX1210 Pin Diagram

Notes:

- yyww refers to the date code
- ----- refers to the lot number

1.3. Pin Description

Table 2: SX1210 Pinouts

Number	Name	Type	Description
0	GND	I	Exposed ground pad
1	TEST5	I/O	Connect to GND
2	TEST1	I/O	Connect to GND
3	VR_VCO	O	Regulated supply of the VCO
4	VCO_M	I/O	VCO tank
5	VCO_P	I/O	VCO tank
6	LF_M	I/O	PLL loop filter
7	LF_P	I/O	PLL loop filter
8	TEST6	I/O	Connect to GND
9	TEST7	I/O	Connect to GND
10	XTAL_P	I/O	Crystal connection
11	XTAL_M	I/O	Crystal connection
12	TEST0	I	Connect to GND
13	TEST8	I/O	POR. Do not connect if unused
14	NSS_CONFIG	I	SPI CONFIG enable
15	NSS_DATA	I	SPI DATA enable
16	MISO	O	SPI data output
17	MOSI	I	SPI data input
18	SCK	I	SPI clock input
19	CLKOUT	O	Clock output
20	DATA	O	NRZ data output (Continuous mode)
21	IRQ_0	O	Interrupt output
22	IRQ_1	O	Interrupt output
23	PLL_LOCK	O	PLL lock detection output
24	TEST2	I/O	Connect to GND
25	TEST3	I/O	Connect to GND
26	VDD	I	Supply voltage
27	VR_1V	O	Regulated supply of the analog circuitry
28	VR_DIG	O	Regulated supply of digital circuitry
29	NC	-	Connect to GND
30	TEST4	I/O	Connect to GND
31	RFI	I	RF input
32	NC	-	Connect to GND

Note: pin 13 (Test 8) can be used as a manual reset trigger. See section 7.4.2 for details on its use.

2. Electrical Characteristics



2.1. ESD Notice

The SX1210 is a high performance radio frequency device. It satisfies:

- Class 2 of the JEDEC standard JESD22-A114-B (Human Body Model), except on pins 3-4-5-27-28-31-where it satisfies Class 1A.
- Class III of the JEDEC standard JESD22-C101C (Charged Device Model) on all pins.

It should thus be handled with all the necessary ESD precautions to avoid any permanent damage.

2.2. Absolute Maximum Ratings

Stresses above the values listed below may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 3: Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
VDDmr	Supply voltage	-0.3	3.7	V
Tmr	Storage temperature	-55	125	°C
Pmr	Input level	-	0	dBm

2.3. Operating Range

Table 4: Operating Range

Symbol	Description	Min	Max	Unit
VDDop	Supply Voltage	2.1	3.6	V
Trop	Temperature	-40	+85	°C
ML	Input Level	-	0	dBm

2.4. Chip Specification

Conditions: Temp = 25 °C, VDD = 3.3 V, crystal frequency = 12.8 MHz, carrier frequency = 869 or 915 MHz, modulation FSK, data rate = 25 kb/s, Fdev = 50 kHz, fc = 100 kHz, unless otherwise specified.

2.4.1. Power Consumption

Table 5: Power Consumption Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
IDDSL	Supply current in sleep mode		-	0.1	2	μA
IDDST	Supply current in standby mode, CLKOUT disabled	Crystal oscillator running	-	65	95	μA
IDDFS	Supply current in FS mode	Frequency synthesizer running	-	1.3	1.7	mA
IDDR	Supply current in receiver mode		-	3.0	3.5	mA

⁽¹⁾ Guaranteed by design and characterization

2.4.2. Frequency Synthesis

Table 6: Frequency Synthesizer Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
FR	Frequency ranges	Programmable but requires specific BOM	863	-	870	MHz
			902	-	928	MHz
			950	-	960	MHz
BR_F	Bit rate (FSK)	NRZ	1.56	-	200	Kb/s
BR_O	Bit rate (OOK)	NRZ	1.56	-	32	Kb/s
FDA	Frequency deviation (FSK)		33	50	200	kHz
XTAL	Crystal oscillator frequency		9	12.8	15	MHz
FSTEP	Frequency synthesizer step	Variable, depending on the frequency.	-	2	-	kHz
TS_OSC	Oscillator wake-up time	From Sleep mode ⁽¹⁾	-	1.5	5	ms
TS_FS	Frequency synthesizer wake-up time at most 10 kHz away from the target	From Stby mode	-	500	800	μs
TS_HOP	Frequency synthesizer hop time at most 10 kHz away from the target	200 kHz step	-	180	-	μs
		1 MHz step	-	200	-	μs
		5 MHz step	-	250	-	μs
		7 MHz step	-	260	-	μs
		12 MHz step	-	290	-	μs
		20 MHz step	-	320	-	μs
		27 MHz step	-	340	-	μs

⁽¹⁾ Guaranteed by design and characterization

2.4.3. Receiver

- On the following table, f_c and f_o describe the bandwidth of the active channel filters as described in section 3.3.4.2. All sensitivities are measured receiving a PN15 sequence, for a BER of 0.1. %

Table 7: Receiver Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
RFS_F	Sensitivity (FSK)	869 MHz, BR=25 kb/s, Fdev=50 kHz, $f_c=100$ kHz	-	-107	-	dBm
		869 MHz, BR=66.7 kb/s, Fdev=100 kHz, $f_c=200$ kHz	-	-103	-	dBm
		915 MHz, BR=25 kb/s, Fdev=50 kHz, $f_c=100$ kHz	-	-105	-	dBm
		915 MHz, BR=66.7 kb/s, Fdev=100 kHz, $f_c=200$ kHz	-	-101	-	dBm
RFS_O	Sensitivity (OOK)	869 MHz, 2kb/s NRZ $f_c-f_o=50$ kHz, $f_o=50$ kHz	-	-113	-	dBm
		869 MHz, 16.7 kb/s NRZ $f_c-f_o=100$ kHz, $f_o=100$ kHz	-	-106	-	dBm
		915 MHz, 2kb/s NRZ $f_c-f_o=50$ kHz, $f_o=50$ kHz	-	-111	-	dBm
		915 MHz, 16.7 kb/s NRZ $f_c-f_o=100$ kHz, $f_o=100$ kHz	-	-105	-	dBm
CCR	Co-channel rejection	Modulation as wanted signal	-	-12	-	dBc
ACR	Adjacent channel rejection	Offset = 300 kHz, unwanted tone is not modulated	-	27	-	dB
		Offset = 600 kHz, unwanted tone is not modulated	-	52	-	dB
		Offset = 1.2 MHz, unwanted tone is not modulated	-	57	-	dB
BI	Blocking immunity	Offset = 1 MHz, unmodulated	-	-48	-	dBm
		Offset = 2 MHz, unmodulated, no SAW	-	-37	-	dBm
		Offset = 10 MHz, unmodulated, no SAW	-	-33	-	dBm
RXBW_F ^(1,2)	Receiver bandwidth in FSK mode	Single side BW Polyphase Off	50	-	250	kHz
RXBW_O ^(1,2)	Receiver bandwidth in OOK mode	Single side BW Polyphase On	50	-	400	kHz
IIP3	Input 3 rd order intercept point	Interferers at 1MHz and 1.950 MHz offset	-	-28	-	dBm
TS_RE ⁽¹⁾	Receiver wake-up time	From FS to Rx ready	-	280	500	µs
TS_RE2 ⁽¹⁾	Receiver wake-up time	From Stby to Rx ready	-	600	900	µs
TS_RE_HOP	Receiver hop time from Rx ready to Rx ready with a frequency hop	200 kHz step	-	400	-	µs
		1MHz step	-	400	-	µs
		5MHz step	-	460	-	µs
		7MHz step	-	480	-	µs
		12MHz step	-	520	-	µs
		20MHz step	-	550	-	µs
		27MHz step	-	600	-	µs
TS_RSSI	RSSI sampling time	From Rx ready	-	-	1/Fdev	s
DR_RSSI	RSSI dynamic Range	Ranging from sensitivity	-	70	-	dB

⁽¹⁾ Guaranteed by design and characterization

- ⁽²⁾ This reflects the whole receiver bandwidth, as described in sections 3.3.4.1 and 3.3.4.2

2.4.4. Digital Specification

Conditions: Temp = 25 °C, VDD = 3.3 V, crystal frequency = 12.8 MHz, unless otherwise specified.

Table 8: Digital Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
VIH	Digital input level high		0.8*VDD	-	-	V
VIL	Digital input level low		-	-	0.2*VDD	V
VOH	Digital output level high	I _{max} =1mA	0.9*VDD	-	-	V
VOL	Digital output level low	I _{max} =-1mA	-	-	0.1*VDD	V
SCK_CONFIG	SPI Config. clock frequency		-	-	6	MHz
SCK_DATA	SPI data clock frequency		-	-	1	MHz
T_DATA	DATA hold and setup time		2	-	-	µs
T_MOSI_C	MOSI setup time for SPI Config.		250	-	-	ns
T_MOSI_D	MOSI setup time for SPI Data.		312	-	-	ns
T_NSSC_L	NSS_CONFIG low to SCK rising edge. SCK falling edge to NSS_CONFIG high.		500	-	-	ns
T_NSSD_L	NSS_DATA low to SCK rising edge. SCK falling edge to NSS_DATA high.		625	-	-	ns
T_NSSC_H	NSS_CONFIG rising to falling edge.		500	-	-	ns
T_NSSD_H	NSS_DATA rising to falling edge.		625	-	-	ns

Note: on pin 10 (XTAL_P) and 11 (XTAL_N), maximum voltages of 1.8V can be applied.

3. Architecture Description

This section describes in depth the architecture of this ultra low-power receiver:

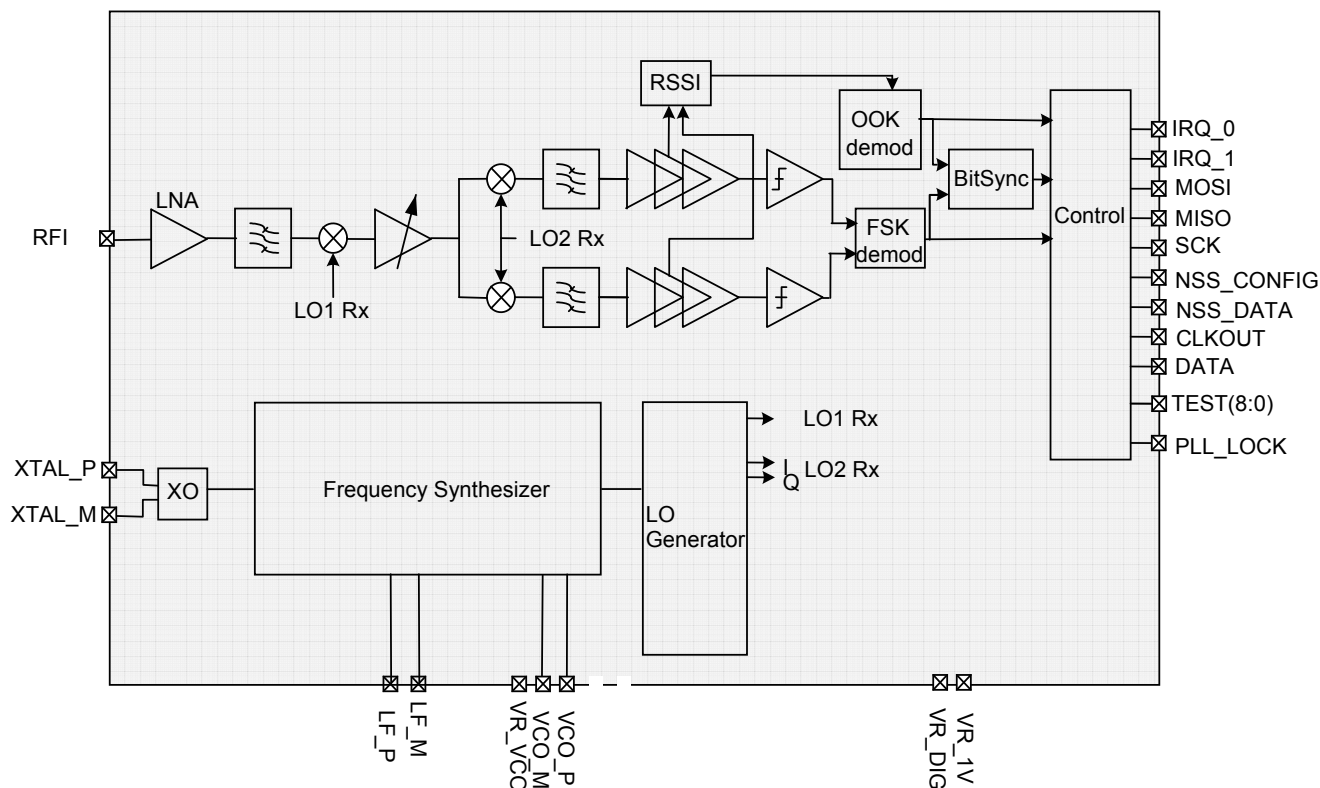


Figure 3: SX1210 Detailed Block Diagram

3.1. Power Supply Strategy

To provide stable sensitivity and linearity characteristics over a wide supply range, the SX1210 is internally regulated. This internal regulated power supply structure is described below:

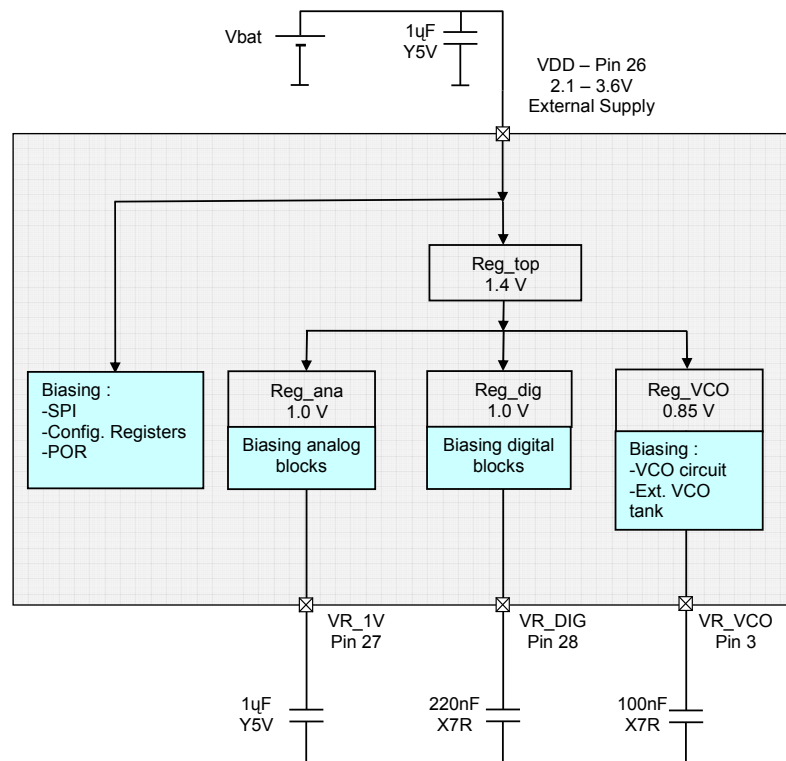


Figure 4: Power Supply Breakdown

To ensure correct operation of the regulator circuit, the decoupling capacitor connection shown in Figure 4 is required. These decoupling components are recommended for any design.

3.2. Frequency Synthesis Description

The frequency synthesizer of the SX1210 is a fully integrated integer-N type PLL. The PLL circuit requires only five external components for the PLL loop filter and the VCO tank circuit.

3.2.1. Reference Oscillator

The SX1210 embeds a crystal oscillator, which provides the reference frequency for the PLL. The recommended crystal specification is given in section 7.1.

3.2.2. CLKOUT Output

The reference frequency, or a sub-multiple of it, can be provided on CLKOUT (pin 19) by activating the bit OSCParam_Clkout_on. The division ratio is programmed through bits OSCParam_Clkout_freq. The two applications of the CLKOUT output are:

- To provide a clock output for a companion uC, thus saving the cost of an additional oscillator. CLKOUT can be made available in any operation mode, except Sleep mode, and is automatically enabled at power-up.
- To provide an oscillator reference output. Measurement of the CLKOUT signal enables simple software trimming of the initial crystal tolerance.

Note: To minimize the current consumption of the SX1210, ensure that the CLKOUT signal is disabled when unused.

3.2.3. PLL Architecture

The crystal oscillator (XO) forms the reference oscillator of an Integer-N Phase Locked Loop (PLL), whose operation is discussed in the following section. Figure 5 shows a block schematic of the SX1210 PLL. Here the crystal reference frequency and the software controlled dividers R, P and S determine the output frequency of the PLL.

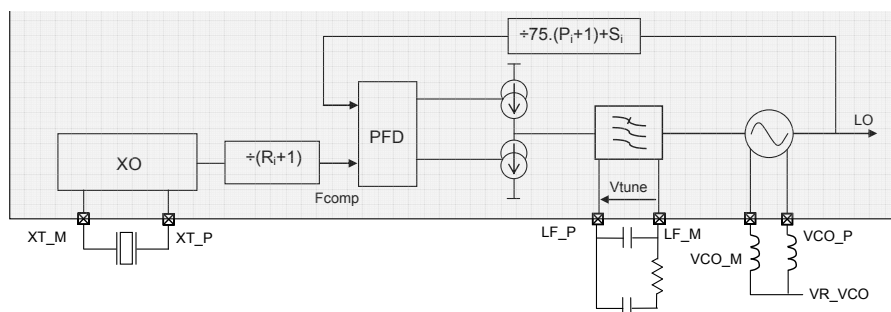


Figure 5: Frequency Synthesizer Description

The VCO tank inductors are connected on an external differential input. Similarly, the loop filter is also located externally. However, there is an internal 8pF capacitance at VCO input that should be subtracted from the desired loop filter capacitance.

The output signal of the VCO is used as the input to the local oscillator (LO) generator stage, illustrated in Figure 6. The VCO frequency is subdivided and used in a series of up (down) conversions for transmission (reception).

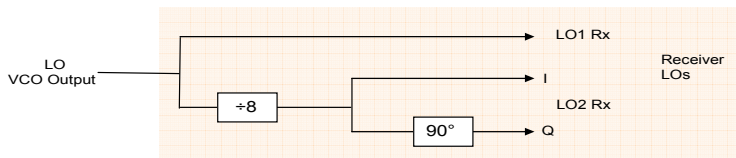


Figure 6: LO Generator

3.2.4. PLL Tradeoffs

With an integer-N PLL architecture, the following criterion must be met to ensure correct operation:

- The comparison frequency, F_{comp} , of the Phase Frequency Detector (PFD) input must remain higher than six times the PLL bandwidth (PLLBW) to guarantee loop stability and to reject harmonics of the comparison frequency F_{comp} . This is expressed in the inequality:

$$PLLBW \leq \frac{F_{comp}}{6}$$

- However the PLLBW has to be sufficiently high to allow adequate PLL lock times
- Because the divider ration R determines F_{comp} , it should be set close to 119, leading to $F_{comp} \approx 100$ kHz which will ensure suitable PLL stability and speed.

With the recommended Bill Of Materials (BOM) of the reference design of section 7.5.3, the PLL prototype is the following:

- $64 \leq R \leq 169$
- $S < P+1$
- PLLBW = 15 kHz nominal
- Startup times and reference frequency spurs as specified.

3.2.5. Voltage Controlled Oscillator

The integrated VCO requires only two external tank circuit inductors. As the input is differential, the two inductors should have the same nominal value. The performance of these components is important for both the phase noise and the power consumption of the PLL. It is recommended that a pair of high Q factor inductors is selected. These should be mounted orthogonally to other inductors (in particular the LNA biasing inductor) to reduce spurious coupling between the LNA input and VCO.

For best performance wound type inductors, with tight tolerance, should be used as described in section 7.5.3.

3.2.5.1. SW Settings of the VCO

To guarantee the optimum operation of the VCO over the SX1210's frequency and temperature ranges, the following settings should be programmed into the SX1210:

Target channel (MHz)	863- 870	902- 915	915- 928	950- 960
Freq_band	10	00	01	10

Table 9: MCPParam_Freq_band Setting

3.2.5.2. Trimming the VCO Tank by Hardware and Software

To ensure that the frequency band of operation may be accurately addressed by the R, P and S dividers of the synthesizer, it is necessary to ensure that the VCO is correctly centered. Note that for the reference design (see section 7.5) no centering is necessary. However, any deviation from the reference design may require the optimization procedure, outlined below, to be implemented. This procedure is simplified thanks to the built-in VCO trimming feature which is controlled over the SPI interface. This tuning does not require any RF test equipment, and can be achieved by simply measuring V_{tune} , the voltage between pins 6 (LFM) and 7 (LFP).

The VCO is centered if the voltage is within the range:

$$50 \leq V_{tune}(mV) \leq 150mV$$

If this inequality is not satisfied then adjust the MCPParam_VCO_trim bits from 00 whilst monitoring V_{tune} . This allows the VCO voltage to be trimmed in + 60 mV increments. Should the desired voltage range be inaccessible, the voltage may be adjusted further by changing the tank circuit inductance value. Note that an increase in inductance will result in an increase V_{tune} .

Note for mass production: The VCO capacitance is piece to piece dependant. As such, the optimization proposed above should be verified on several prototypes, to ensure that the population is centered on 100 mV.

3.2.6. PLL Loop Filter

To adequately reject spurious components arising from the comparison frequency F_{comp} , an external 2nd order loop filter is employed.

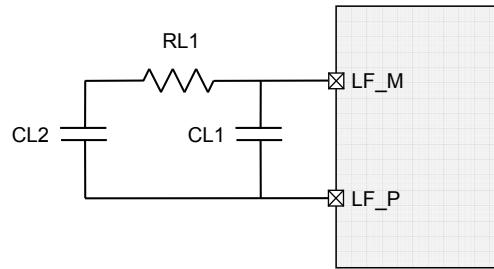


Figure 7: Loop Filter

Following the recommendations made in section 3.2.4, the loop filter proposed in the reference design's bill of material on section 7.5.3 should be used. The loop filter settings are frequency band independent and are hence relevant to all implementations of the SX1210.

3.2.7. PLL Lock Detection Indicator

The SX1210 also features a PLL lock detect indicator. This is useful for optimizing power consumption, by adjusting the synthesizer wake up time (TS_FS), since the PLL startup time is lower than specified under nominal conditions. The lock status can be read on bit IRQParam_PLL_lock, and must be cleared by writing a "1" to this same register. In addition, the lock status can be reflected in pin 23 PLL_LOCK, by setting the bit IRQParam_Enable_lock_detect.

3.2.8. Frequency Calculation

As shown in Figure 5 the PLL structure comprises three different dividers, R, P and S, which set the output frequency through the LO. A second set of dividers is also available to allow rapid switching between a pair of frequencies: R1/P1/S1 and R2/P2/S2. These six dividers are programmed by six bytes of the register MCPParam from addresses 6 to 11.

3.2.8.1. FSK Mode

The following formula gives the relationship between the local oscillator, and R, P and S values, when using FSK modulation.

$$F_{rf}, f_{sk} = \frac{9}{8} F_{lo}$$

$$F_{rf}, f_{sk} = \frac{9}{8} \frac{F_{xtal}}{R+1} [75(P+1) + S]$$

3.2.8.2. OOK Mode

Due to the low intermediate frequency (Low-IF) architecture of the SX1210 the frequency should be configured so as to ensure the correct low-IF receiver baseband center frequency, IF2.

$$F_{rf}, o_{ok} = \frac{9}{8} F_{lo} - IF2$$

$$F_{rf}, o_{ok} = \frac{9}{8} \frac{F_{xtal}}{R+1} [75(P+1) + S] - IF2$$

Note that from Section 3.3.4, it is recommended that IF2 be set to 100 kHz.

3.3. Receiver Description

The SX1210 is set to receive mode when MCPParam_Chip_mode = 011.

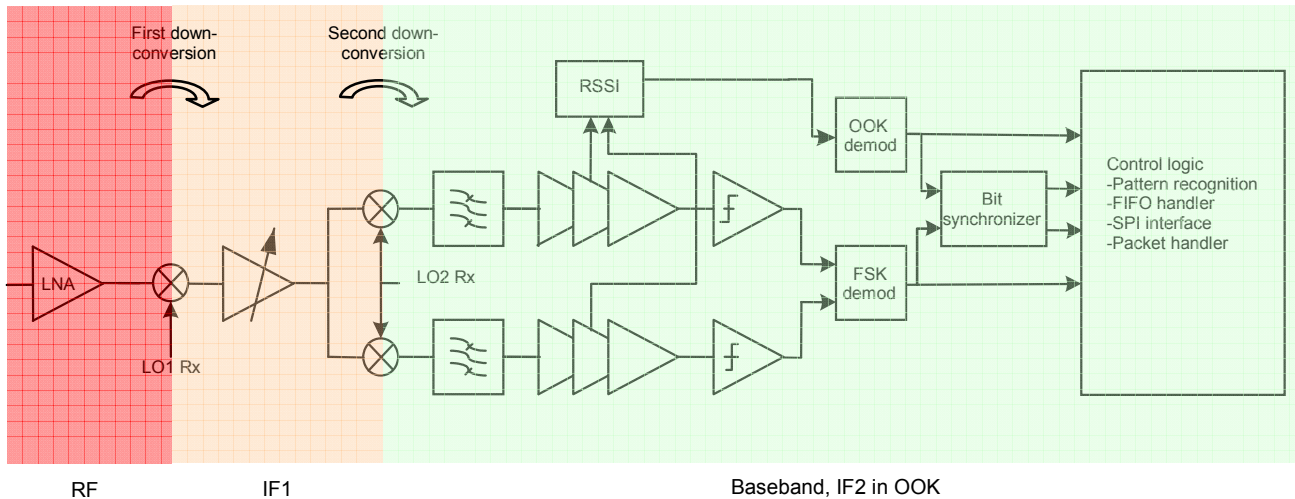


Figure 8: Receiver Architecture

3.3.1. Architecture

The SX1210 receiver employs a super-heterodyne architecture. Here, the first IF is $1/9^{\text{th}}$ of the RF frequency (approximately 100MHz). The second down-conversion down-converts the I and Q signals to base band in the case of the FSK receiver (Zero IF) and to a low-IF (IF2) for the OOK receiver.

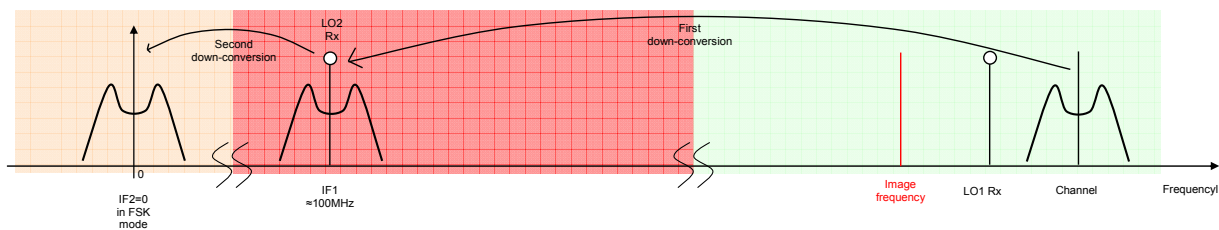


Figure 9: FSK Receiver Setting

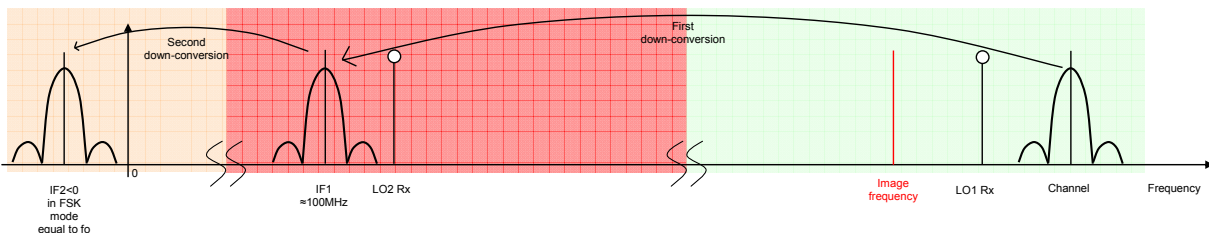


Figure 10: OOK Receiver Setting

After the second down-conversion stage, the received signal is channel-select filtered and amplified to a level adequate for demodulation. Both FSK and OOK demodulation are available. Finally, an optional Bit Synchronizer (BitSync) is provided, to be supply a synchronous clock and data stream to a companion uC in Continuous mode,

or to fill the FIFO buffers with glitch-free data in Buffered mode. The operation of the receiver is now described in detail.

Note: Image rejection is achieved by the SAW filter.

3.3.2. LNA and First Mixer

The performance of this amplifier is such that the Noise Figure (NF) of the receiver can be estimated to be ≈ 7 dB.

3.3.3. IF Gain and Second I/Q Mixer

Following the LNA and first down-conversion, there is an IF amplifier whose gain can be programmed from -13.5 dB to 0 dB in 4.5 dB steps, via the register MCParm_IF_gain. The default setting corresponds to 0 dB gain, but lower values can be used to increase the RSSI dynamic range. Refer to section 3.3.7 for additional information.

3.3.4. Channel Filters

The second mixer stages are followed by the channel select filters. The channel select filters have a strong influence on the noise bandwidth and selectivity of the receiver and hence its sensitivity. Each filter comprises a passive and active section.

3.3.4.1. Passive Filter

Each channel select filter features a passive second-order RC filter, with a bandwidth programmable through the bits RXParam_PassiveFilt. As the wider of the two filters, its effect on the sensitivity is negligible, but its bandwidth has to be setup instead to optimize blocking immunity. The value entered into this register sets the single side bandwidth of this filter. For optimum performance it should be set to 3 to 4 times the cutoff frequency of the active Butterworth (or polyphase) filter described in the next section.

$$3 * F_{C_{ButterFilt}} \leq BW_{passive, filter} \leq 4 * F_{C_{ButterFilt}}$$

3.3.4.2. Active Filter

The 'fine' channel selection is performed by an active, third-order, Butterworth filter, which acts as a low-pass filter for the zero-IF configuration (FSK), or a complex polyphase filter for the Low-IF (OOK) configuration. The RXParam_PolyFilt_on bit enables/disables the polyphase filter.

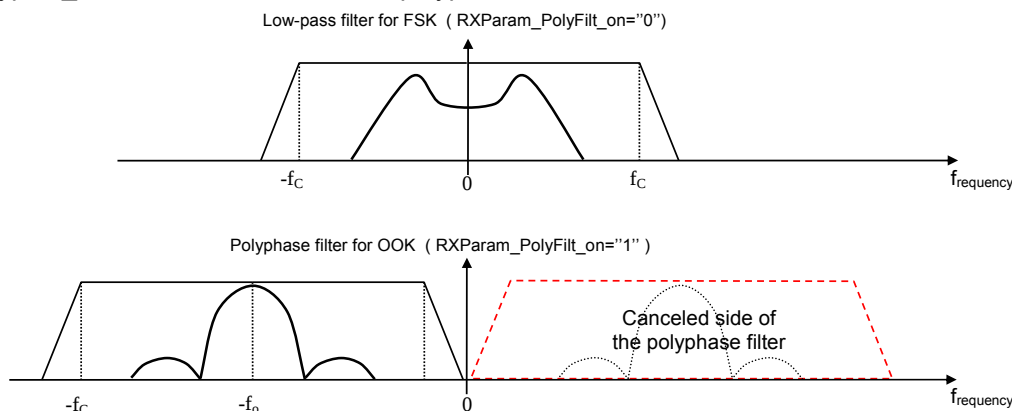


Figure 11: Active Channel Filter Description

As can be seen from Figure 11, the required bandwidth of this filter varies between the two demodulation modes.

- FSK mode: The 99% energy bandwidth of an FSK modulated signal is approximated to be:

$$BW_{99\%,FSK} = 2 * \left[F_{dev} + \frac{BR}{2} \right]$$

The bits `RXParam_ButterFilt` set f_c , the cutoff frequency of the filter. As we are in a Zero-IF configuration, the FSK lobes are centered around the virtual “DC” frequency. The choice of f_c should be such that the modulated signal falls in the filter bandwidth, anticipating the Local Oscillator frequency drift over the operating temperature and aging of the device:

$$2 * f_c > BW_{99\%,FSK} + LO_{drifts}$$

Please refer to the charts in section 3.3.5 for an accurate overview of the filter bandwidth vs. setting.

- OOK mode: The 99% energy bandwidth of an OOK modulated signal is approximated to be:

$$BW_{99\%,OOK} = \frac{2}{T_{bit}} = 2.BR$$

The bits `RXParam_PolypFilt_center` set f_o , the center frequency of the polyphase filter when activated. f_o should always be chosen to be equal to the low Intermediate Frequency of the receiver (IF2). This is why, in the GUI described in section 7.2.1 of this document, the low IF frequency of the OOK receiver denoted IF2 has been replaced by f_o .

The following setting is recommended:

$$f_o = 100kHz$$

$$RXParam_PolypFilt = "0011"$$

The value stored in `RXParam_ButterFilt` determines f_c , the filter cut-off frequency. So the user should set f_c according to:

$$2 * (f_c - f_o) > BW_{99\%,OOK} + LO_{drifts}$$

Again, f_c as a function of `RXParam_ButterFilt` is given in the section 3.3.6.

3.3.5. Channel Filters Setting in FSK Mode

F_c , the 3dB cutoff frequency of the Butterworth filter used in FSK reception, is programmed through the bit `RXParam_ButterFilt`. However, the whole receiver chain influences this cutoff frequency. Thus the channel select and resultant filter bandwidths are summarized in the following chart:

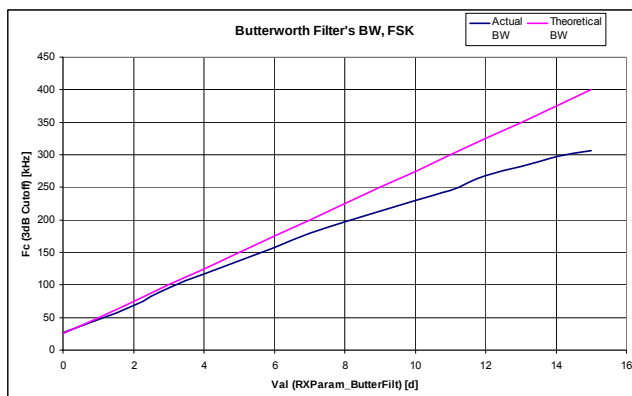


Figure 12: Butterworth Filter's Actual BW

Table 31 suggests filter settings in FSK mode, along with the corresponding passive filter bandwidth and the accepted tolerance on the crystal reference.

3.3.6. Channel Filters Setting in OOK Mode

The center frequency, f_0 , is always set to 100kHz. The following chart shows the receiver bandwidth when changing RXParam_Butterfilt bits, whilst the polyphase filter is activated.

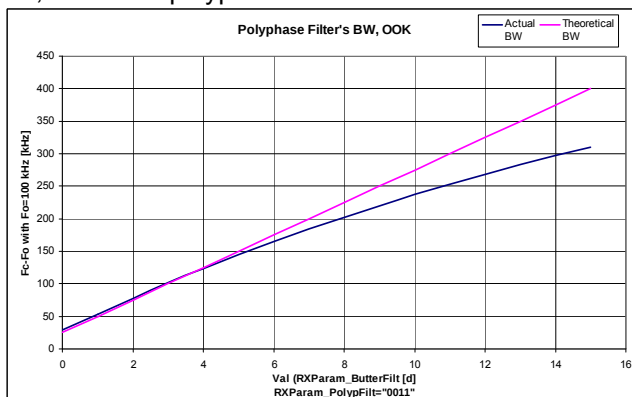


Figure 13: Polyphase Filter's Actual BW

Table 32 suggests a few filter settings in OOK mode, along with the corresponding passive filter bandwidth and the accepted tolerance on the crystal reference.

3.3.7. RSSI

After filtering, the In-phase and Quadrature signals are amplified by a chain of 11 amplifiers, each with 6dB gain. The outputs of these amplifiers are used to evaluate the Received Signal Strength (RSSI).

3.3.7.1. Resolution and Accuracy

Whilst the RSSI resolution is 0.5 dB, the absolute accuracy is not expected to be better than ± 3 dB due to process and external component variation. Higher accuracy whilst performing absolute RSSI measurements will require additional calibration.

3.3.7.2. Acquisition Time

In OOK mode, the RSSI evaluates the signal strength by sampling $I(t)$ and $Q(t)$ signals 16 times in each period of the chosen IF2 frequency (refer to section 3.3.1). In FSK mode, the signals are sampled 16 times in each Fdev period, Fdev being the frequency deviation of the companion transmitter. An average is then performed over a sliding window of 16 samples. Hence, the RSSI output register RXParam_RSSI is updated 16 times in each Fdev or IF2 period.

The following settings should be respected:

- FSK Mode: Ensure that the Fdev parameter (as described in MCPParam_Fdev) remains consistent with the actual frequency deviation of the companion transmitter.
- OOK reception: Ensure that the Fdev parameter (as described in MCPParam_Fdev) is equal with the frequency of $I(t)$ and $Q(t)$ signals, i.e. the second Intermediate Frequency, IF2, of the receiver (Note that this equals F_o , the center frequency of the polyphase filter).

3.3.7.3. Dynamic Range

The dynamic range of the RSSI is over 70 dB, extending from the nominal sensitivity level. The IF gain setting available in MCPParam_IF_gain is used to achieve this dynamic range:

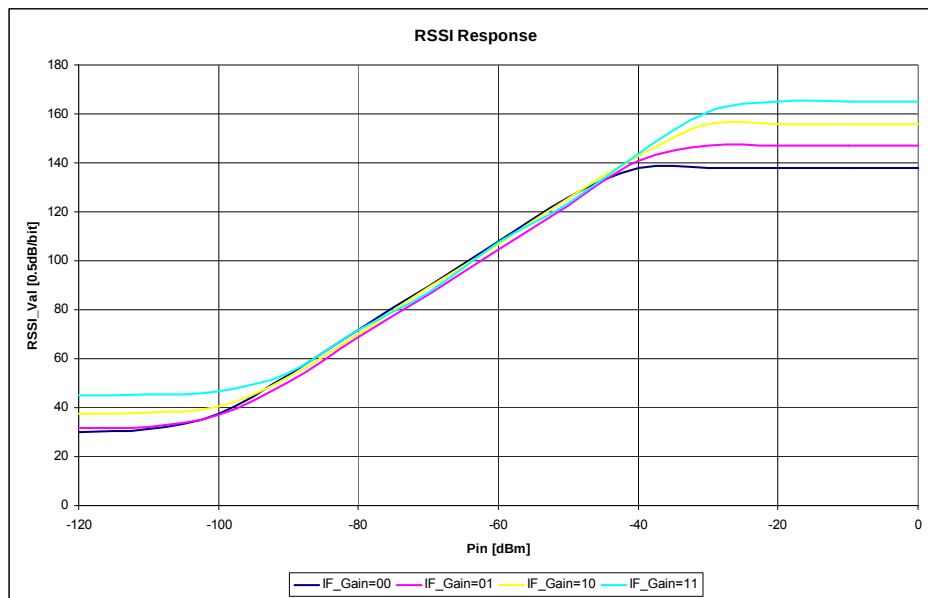


Figure 14: RSSI Dynamic Range

The RSSI response versus input signal is independent of the receiver filter bandwidth. However in the absence of any input signal, the minimum value directly reflects upon the noise floor of the receiver, which is dependant on the filter bandwidth of the receiver.

3.3.7.4. RSSI IRQ Source

The SX1210 can also be used to detect a RSSI level above a pre-configured threshold. The threshold is set in IRQParam_RSSI_irq_thresh and the IRQ status stored in IRQParam_RSSI_irq (cleared by writing a "1").

An interrupt can be mapped to the IRQ0 or IRQ1 pins via bits IRQParam_Rx_stby_irq0 or IRQParam_Rx_stby_irq1. Figure 15 shows the timing diagram of the RSSI interrupt source, with IRQParam_RSSI_irq_thresh set to 28.

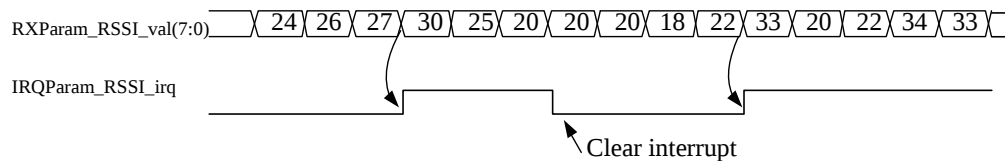


Figure 15: RSSI IRQ Timings

3.3.8. Fdev Setting in Receive Mode

The effect of the Fdev setting is different between FSK and OOK modes:

3.3.8.1. FSK Rx Mode

In FSK mode the Fdev setting, as configured by MCPParam_Freq_Dev, sets sampling frequencies on the receiver. The user should make it consistent with the frequency deviation of the FSK signal that is received.

3.3.8.2. OOK Rx Mode

The frequency deviation Fdev, as described above, sets the sampling rate of the RSSI block. It is therefore necessary to set Fdev to the recommended low-IF frequency, IF2, of 100 kHz:

$$Fdev = IF2 = 100kHz$$

$$MCPParam_Freq_dev = "00000011"$$

3.3.9. FSK Demodulator

The FSK demodulator provides data polarity information, based on the relative phase of the input I and Q signals at the baseband. Its outputs can be fed to the Bit Synchronizer to recover the timing information. The user can also use the raw, unsynchronized, output of the FSK demodulator in Continuous mode.

The FSK demodulator of the SX1210 operates most effectively for FSK signals with a modulation index greater than or equal to two:

$$\beta = \frac{2 * Fdev}{BR} \geq 2$$

3.3.10. OOK Demodulator

The OOK demodulator performs a comparison of the RSSI output and a threshold value. Three different threshold modes are available, programmed through the RXPParam_OOK_thresh_type register.

The recommended mode of operation is the "Peak" threshold mode, illustrated below in Figure 16:

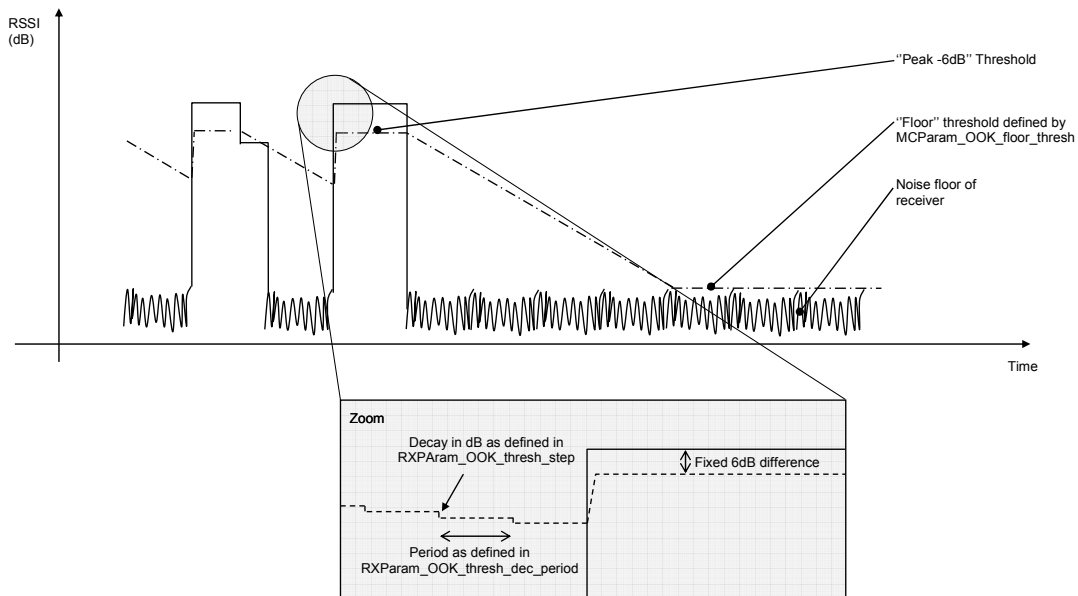


Figure 16: OOK Demodulator Description

In peak threshold mode the comparison threshold level is the peak value of the RSSI, reduced by 6dB. In the absence of an input signal or during the reception of a logical "0", the acquired peak value is decremented by one `RXParam_OOK_thresh_step` every `RXParam_OOK_thresh_dec_period`.

When the RSSI output is null for a long time (for instance after a long string of "0" received, or if no transmitter is present), the peak threshold level will continue falling until it reaches the "Floor Threshold" that is programmed through the register `MCPParam_OOK_floor_thresh`.

The default settings of the OOK demodulator lead to the performance stated in the electrical specification. However, in applications in which sudden signal drops are awaited during a reception, the three parameters shall be optimized accordingly.

3.3.10.1. Optimizing the Floor Threshold

`MCPParam_OOK_floor_thres` determines the sensitivity of the OOK receiver, as it sets the comparison threshold for weak input signals (i.e. those close to the noise floor). Significant sensitivity improvements can be generated if configured correctly.

Note that the noise floor of the receiver at the demodulator input depends on:

- The noise figure of the receiver.
- The gain of the receive chain from antenna to base band.
- The matching - including SAW filter.
- The bandwidth of the channel filters.

It is therefore important to note that the setting of `MCPParam_OOK_floor_thresh` will be application dependant. The following procedure is recommended to optimize `MCPParam_OOK_floor_thresh`.

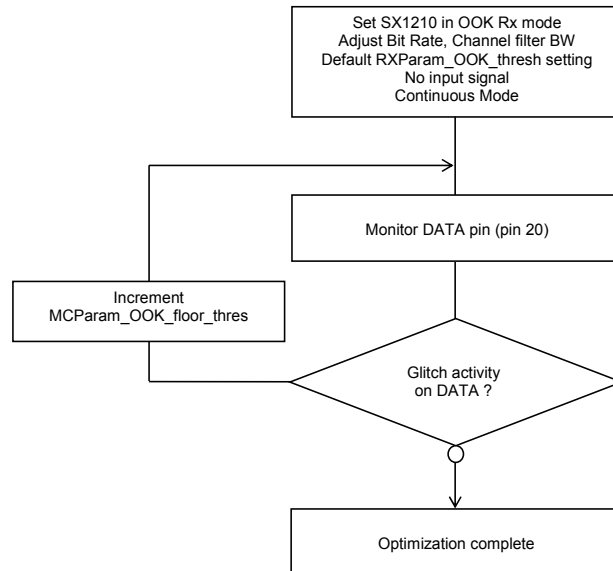


Figure 17: Floor Threshold Optimization

The new floor threshold value found during this test should be the value used for OOK reception with those receiver settings.

Note that if the output signal on DATA is logic “1”, the value of MCPParam_OOK_floor_thres is below the noise floor of the receiver chain. Conversely, if the output signal on DATA is logic “1”, the value of MAParam_floor_thres is several dB above the noise floor.

3.3.10.2. Optimizing OOK Demodulator Response for Fast Fading Signals

A sudden drop in signal strength can cause the bit error rate to increase. For applications where the expected signal drop can be estimated the following OOK demodulator parameters RXParam_OOK_thresh_step and RXParam_OOK_thresh_dec_period can be optimized as described below for a given number of threshold decrements per bit RXParam_OOK_thresh_dec_period:

- 000 → once in each chip period (d)
- 001 → once in 2 chip periods
- 010 → once in 4 chip periods
- 011 → once in 8 chip periods
- 100 → twice in each chip period
- 101 → 4 times in each chip period
- 110 → 8 times in each chip period
- 111 → 16 times in each chip period

For each decrement of RXParam_OOK_thresh_step:

- 000 → 0.5 dB (d)
- 001 → 1.0 dB
- 010 → 1.5 dB
- 011 → 2.0 dB
- 100 → 3.0 dB
- 101 → 4.0 dB
- 110 → 5.0 dB
- 111 → 6.0 dB

3.3.10.3. Alternative OOK Demodulator Threshold Modes

In addition to the Peak OOK threshold mode, the user can alternatively select two other types of threshold detectors:

- Fixed threshold: The value is selected through the `MCPParam_OOK_floor_thresh` register (refer to section 3.3.10.1 for further information concerning optimization of the floor threshold).
- Average threshold: Data supplied by the RSSI block is averaged with the following cutoff frequency:

$$RXParam_OOK_cutoff = 00 \Rightarrow F_{cutoff} = \frac{BR}{8 * \pi}$$

$$RXParam_OOK_cutoff = 11 \Rightarrow F_{cutoff} = \frac{BR}{32 * \pi}$$

In the first example, the higher cut-off frequency enables a sequence of up to 8 consecutive “0” or “1” to be supported, whilst the lower cut-off frequency presented in the second example allows for the correct reception of up to 32 consecutive “0” or “1”.

3.3.11. Bit Synchronizer

The Bit Synchronizer (BitSync) is a block that provides a clean and synchronized digital output, free of glitches.

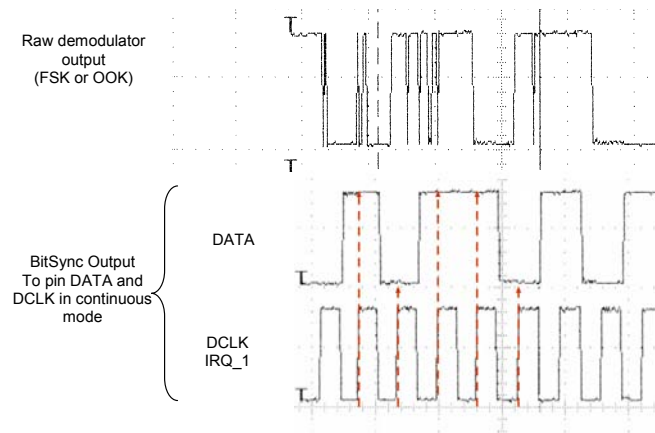


Figure 18: BitSync Description

The BitSync can be disabled through the bits `RXParam_Bitsync_off`, and by holding pin IRQ1 low. However, for optimum receiver performance, its use when running Continuous mode is strongly advised. With this option a DCLK signal is present on pin IRQ_1.

The BitSync is automatically activated in Buffered and Packet modes. The bit synchronizer bit-rate is controlled by `MCPParam_BR`. For a given bit rate, this parameter is determined by:

$$BR = \frac{F_{XTAL}}{64 * [1 + MCPParam_BR]}$$

For proper operation, the Bit Synchronizer must first receive three bytes of alternating logic value preamble, i.e. "0101" sequences. After this startup phase, the rising edge of DCLK signal is centered on the demodulated bit. Subsequent data transitions will preserve this centering.

This has two implications:

- Firstly, if the Bit Rates of Transmitter and Receiver are known to be the same, the SX1210 will be able to receive an infinite unbalanced sequence (all "0s" or all "1s") with no restriction.
- If there is a difference in Bit Rate between Tx and Rx, the amount of adjacent bits at the same level that the BitSync can withstand can be estimated as:

$$NumberOfBits = \frac{1}{2} * \frac{BR}{\Delta BR}$$

This implies approximately 6 consecutive unbalanced bytes when the Bit Rate precision is 1%, which is easily achievable (crystal tolerance is in the range of 50 to 100 ppm).

3.3.12. Alternative Settings

Bit Synchronizer and Active channel filter settings are a function of the reference oscillator crystal frequency, F_{XTAL} . Settings other than those programmable with a 12.8 MHz crystal can be obtained by selection of the correct reference oscillator frequency. Please contact your local Semtech representative for further details.

3.3.13. Data Output

After OOK or FSK demodulation, the baseband signal is made available to the user on pin 20, DATA, when Continuous mode is selected.

In Buffered and Packet modes, the data is retrieved from the FIFO through the SPI interface.

4. Operating Modes

This section summarizes the settings for each operating mode of the SX1210, and explains the functionality available and the timing requirements for switching between modes.

4.1. Modes of Operation

Table 10: Operating Modes

Mode	MCParm_Chip_mode	Active blocks
Sleep	000	SPI, POR
Standby	001	SPI, POR, Top regulator, digital regulator, XO, CLKOUT (if activated through OSCParam_Clkout)
FS	010	Same + VCO regulator, all PLL and LO generation blocks
Receive	011	Same as FS mode + LNA, first mixer, IF amplifier, second mixer set, channel filters, baseband amplifiers and limiters, RSSI, OOK or FSK demodulator, BitSync and all digital features if enabled

4.2. Digital Pin Configuration vs. Chip Mode

Table 11 describes the state of the digital IOs in each of the above described modes of operation, regardless of the data operating mode.

Table 11: Pin Configuration vs. Chip Mode

Chip Mode Pin	Sleep mode	Standby mode	FS mode	Receive mode	Comment
NSS_CONFIG	Input	Input	Input	Input	NSS_CONFIG has the priority over NSS_DATA
NSS_DATA	Input	Input	Input	Input	
MISO	Input	Input	Input	Input	Output only if NSS_CONFIG or NSSDATA='0'
MOSI	Input	Input	Input	Input	
SCK	Input	Input	Input	Input	
IRQ_0	High-Z	Output (1)	Output (1)	Output	
IRQ_1	High-Z	Output (1)	Output (1)	Output	
DATA (3)	High-Z	High-Z	High-Z	Output	
CLKOUT	High-Z	Output	Output	Output	
PLL_LOCK	High-Z	Output (4)	Output (4)	Output (4)	

Notes:

- (1): High-Z if Continuous mode is activated, else Output
- (2): Valid logic states must be applied to inputs at all times to avoid unwanted leakage currents
- (3): Tie to Vss (or Vdd) when not in active receive mode.
- (4): Output if PLL_lock_en = 1, else High-Z

5. Data Processing

5.1. Overview

5.1.1. Block Diagram

Figure 19, illustrates the SX1210 data processing circuit. Its role is to interface the data from the demodulator and the uC access points (SPI, IRQ and DATA pins). It also controls all the configuration registers.

The circuit contains several control blocks which are described in the following paragraphs.

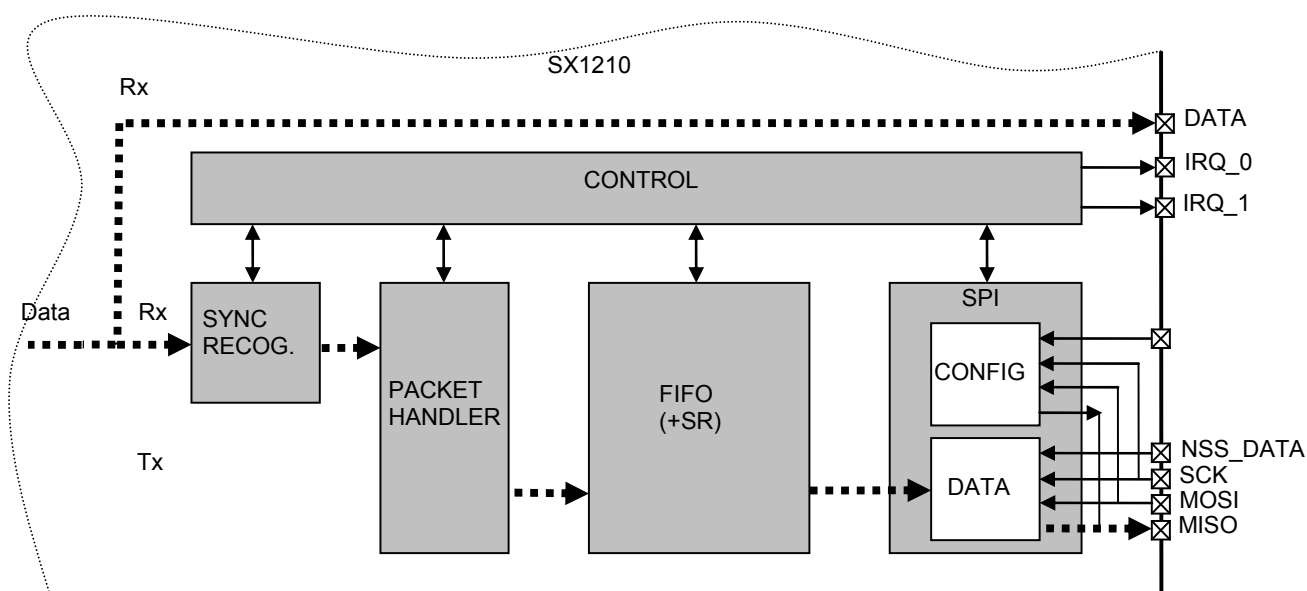


Figure 19: SX1210's Data Processing Conceptual View

The SX1210 implements several data operation modes, each with their own data path through the data processing section. Depending on the data operation mode selected, some control blocks are active whilst others remain disabled.

5.1.2. Data Operation Modes

The SX1210 has three different data operation modes selectable by the user:

- **Continuous mode:** each bit received is accessed in real time at the DATA pin. This mode may be used if adequate external signal processing is available.
- **Buffered mode:** each byte received is stored in a FIFO and accessed via the SPI bus. uC processing overhead is hence significantly reduced compared to Continuous mode operation. The packet length is unlimited.
- **Packet mode (recommended):** user only retrieves payload bytes to/from the FIFO. Sync word is automatically detected and stripped off while optional CRC check and DC free data decoding can be performed. The uC processing overhead is hence reduced further compared to Buffered mode. The maximum payload length is limited to the maximum FIFO limit of 64 bytes

Table 12: Data Operation Mode Selection

MCPParam_Data_mode	Data Operation Mode
00	Continuous
01	Buffered
1x	Packet

Each of these data operation modes is described fully in the following sections.

5.2. Control Block Description

5.2.1. SPI Interface

5.2.1.1. Overview

As illustrated in the Figure 20 below, the SX1210's SPI interface consists of two sub blocks:

- **SPI Config:** used in all data operation modes to read and write the configuration registers which control all the parameters of the chip (operating mode, bit rate, etc...)
- **SPI Data:** used in Buffered and Packet mode to read data bytes from the FIFO. (FIFO interrupts can be used to manage the FIFO content.)

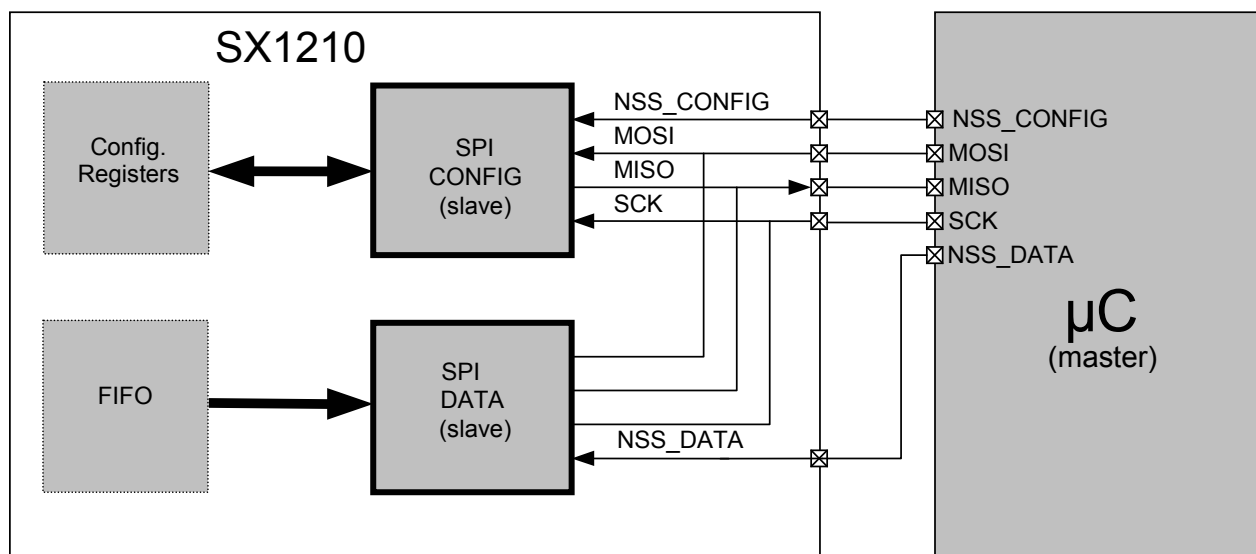


Figure 20: SPI Interface Overview and uC Connections

Both interfaces are configured in slave mode whilst the uC is configured as the master. They have separate selection pins (NSS_CONFIG and NSS_DATA) but share the remaining pins:

- **SCK (SPI Clock):** clock signal provided by the uC
- **MOSI (Master Out Slave In):** data input signal provided by the uC
- **MISO (Master In Slave Out):** data output signal provided by the SX1210

As described below, only one interface can be selected at a time with NSS_CONFIG having the priority:

Table 13: Config vs. Data SPI Interface Selection

NSS_DATA	NSS_CONFIG	SPI Interface
0	0	Config
0	1	Data
1	0	Config
1	1	None

The following paragraphs describe how to use each of these interfaces.

5.2.1.2. SPI Config

▪ Write Register

To write a value into a configuration register the timing diagram below should be carefully followed by the uC. The register's new value is effective from the rising edge of NSS_CONFIG.

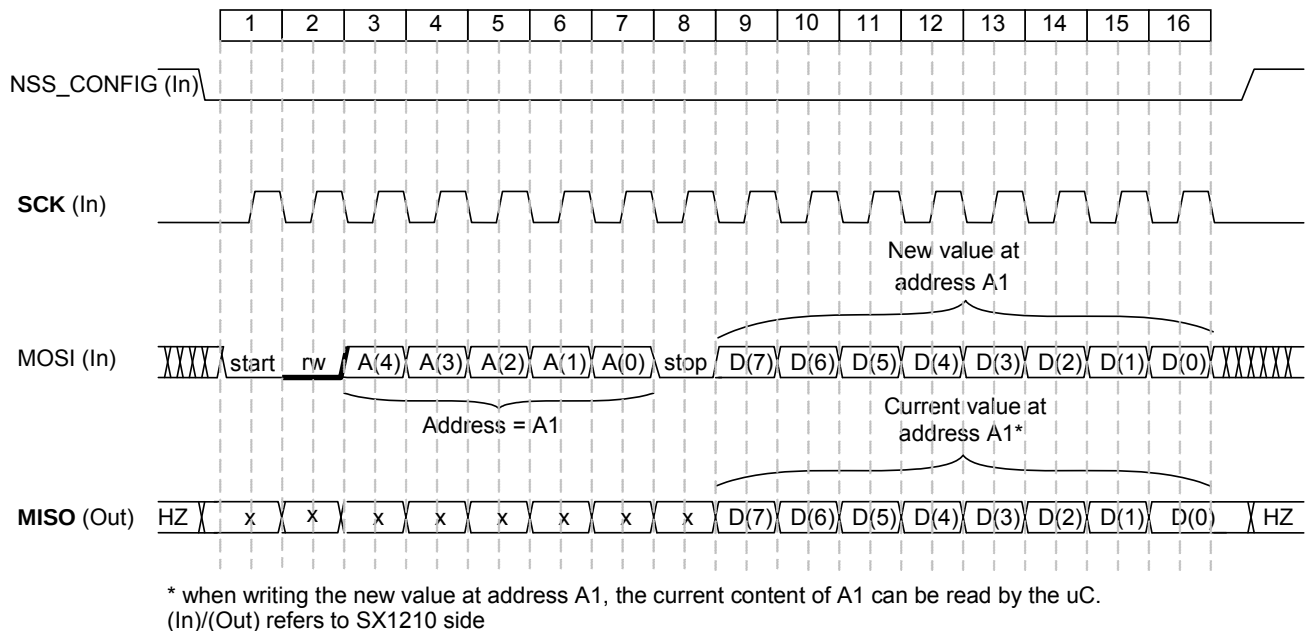


Figure 21: Write Register Sequence

Note that when writing more than one register successively, it is not compulsory to toggle NSS_CONFIG back high between two write sequences. The bytes are alternatively considered as address and value. In this instance, all new values will become effective on rising edge of NSS_CONFIG.

▪ Read Register

To read the value of a configuration register the timing diagram below should be carefully followed by the uC.

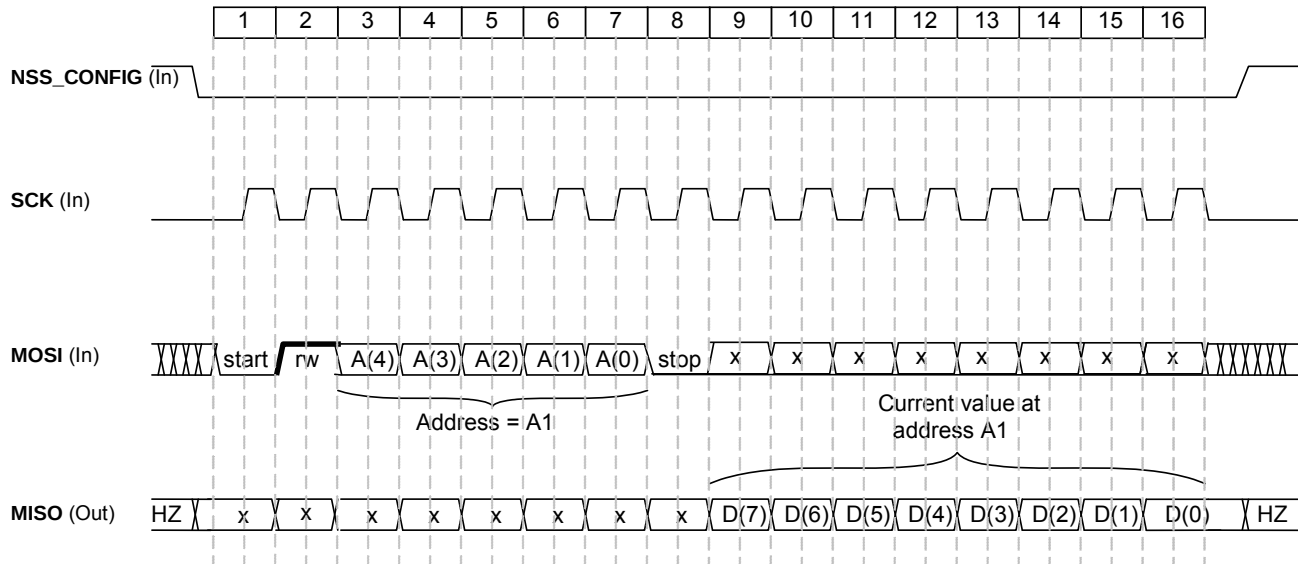


Figure 22: Read Register Sequence

Note that when reading more than one register successively, it is not compulsory to toggle NSS_CONFIG back high between two read sequences. The bytes are alternatively considered as address and value.

5.2.1.3. SPI Data

To read bytes from the FIFO the timing diagram below should be carefully followed by the uC.

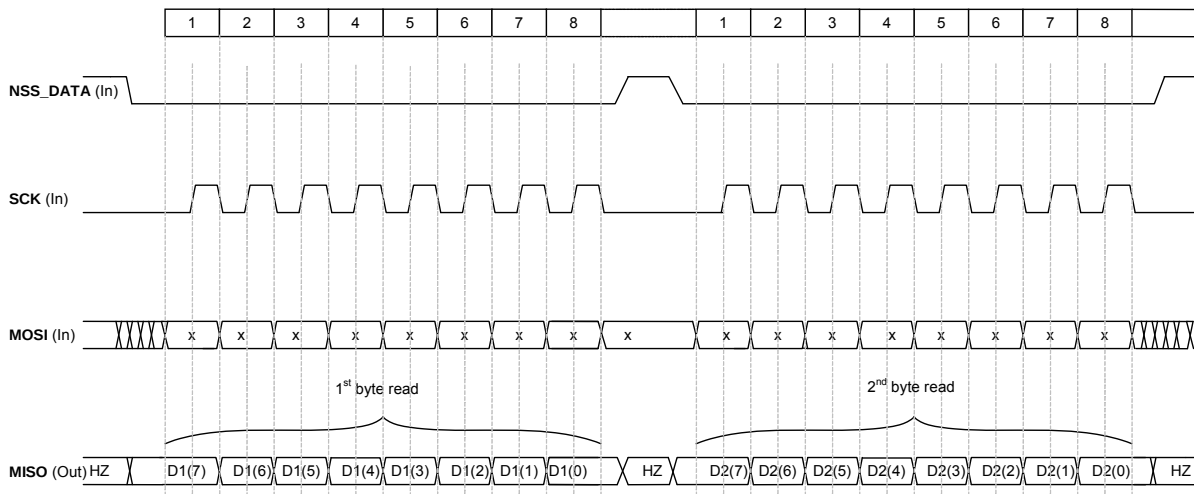


Figure 23: Read Bytes Sequence (ex: 2 bytes)

Note that it is compulsory to toggle NSS_DATA back high between each byte read.

5.2.2. FIFO

5.2.2.1. Overview and Shift Register (SR)

In Buffered and Packet modes of operation, data that have been received are stored in a configurable FIFO (First In First Out) device. It is accessed via the SPI Data interface and provides several interrupts for transfer management.

The FIFO is 1 byte (8 bits) wide hence it only performs byte (parallel) operations, whereas the demodulator functions serially. A shift register is therefore employed to interface the two devices. In Rx the shift register gets bit by bit data from the demodulator and writes them byte by byte to the FIFO. This is illustrated in figure below.

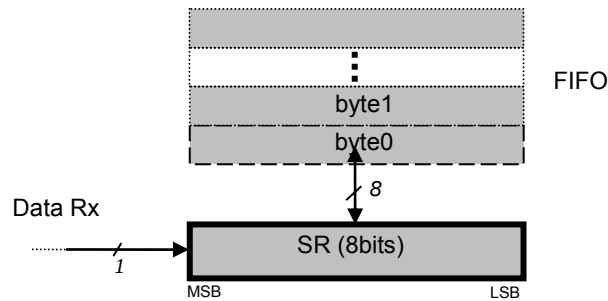


Figure 24: FIFO and Shift Register (SR)

5.2.2.2. Size Selection

The FIFO width is programmable, to 16, 32, 48 or 64 bytes via `MCPParam_Fifo_size`

5.2.2.3. Interrupt Sources and Flags

All interrupt sources and flags are configured in the `IRQParam` section of the configuration register, with the exception of `Fifo_threshold` :

- `/Fifoempty`: `/Fifoempty` interrupt source is low when byte 0, i.e. whole FIFO, is empty. Otherwise it is high. Note that when retrieving data from the FIFO, `/Fifoempty` is updated on `NSS_DATA` falling edge, i.e. when `/Fifoempty` is updated to low state the currently started read operation must be completed. In other words, `/Fifoempty` state must be checked **after** each read operation for a decision on the next one (`/Fifoempty` = 1: more byte(s) to read; `/Fifoempty` = 0: no more byte to read).
- `Write_byte`: `Write_byte` interrupt source goes high for 1 bit period each time a new byte is transferred from the SR to the FIFO (i.e. each time a new byte is received)
- `Fifofull`: `Fifofull` interrupt source is high when the last FIFO byte, i.e. the whole FIFO, is full. Otherwise it is low.
- `Fifo_overrun_clr`: `Fifo_overrun_clr` flag is set when a new byte is written by the SR while the FIFO is already full. Data is lost and the flag should be cleared by writing a 1, note that the FIFO will also be cleared.
- `Fifo_threshold`: `Fifo_threshold` interrupt source's behavior can be programmed via `MCPParam_Fifo_thresh` (B value). This behavior is illustrated in Figure 25.

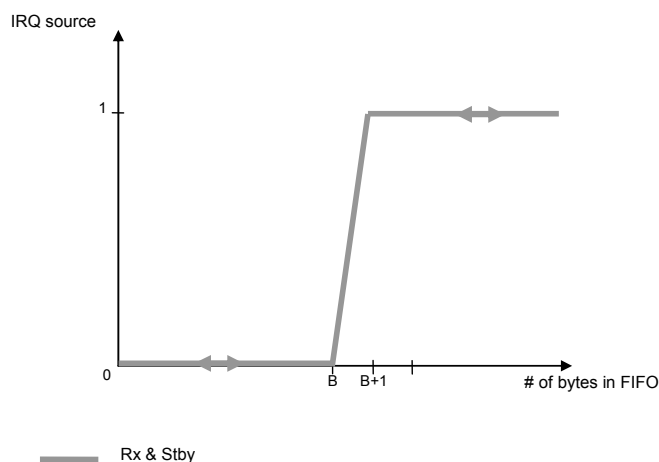


Figure 25: FIFO Threshold IRQ Source Behavior

5.2.2.4. FIFO Clearing

Table 14 below summarizes the status of the FIFO when switching between different modes

Table 14: Status of FIFO when Switching Between Different Modes of the Chip

From	To	FIFO Status	Comments
Stby	Rx	Cleared	
Rx	Stby	Not cleared	In Packet & Buffered modes FIFO can be read in Stby after Rx
Any	Sleep	Cleared	

5.2.3. Sync Word Recognition

5.2.3.1. Overview

Sync word recognition (also called Pattern recognition in previous products) is activated by setting RXPParam_Sync_on. The bit synchronizer must also be activated.

The block behaves like a shift register; it continuously compares the incoming data with its internally programmed Sync word and asserts the Sync IRQ source on each occasion that a match is detected. This is illustrated in Figure 26.

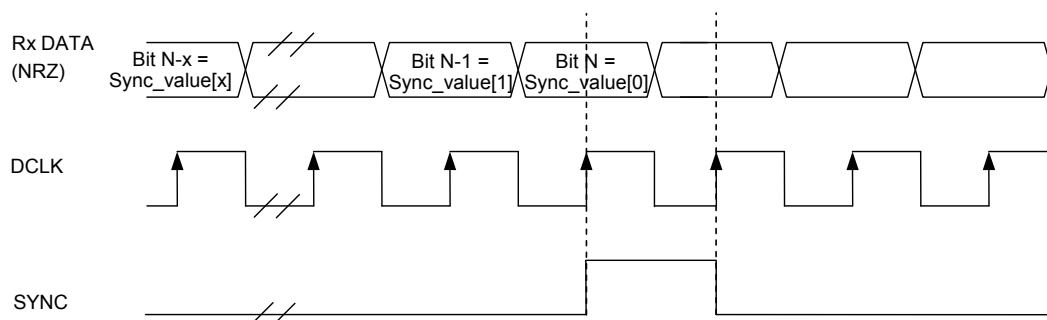


Figure 26: Sync Word Recognition

During the comparison of the demodulated data, the first bit received is compared with bit 7 (MSB) of byte at address 22 and the last bit received is compared with bit 0 (LSB) of the last byte whose address is determined by the length of the Sync word.

When the programmed Sync word is detected the user can assume that this incoming packet is for the node and can be processed accordingly.

5.2.3.2. Configuration

- Size: Sync word size can be set to 8, 16, 24 or 32 bits via `RXParam_Sync_size`.
- Error tolerance: The number of errors tolerated in the Sync word recognition can be set to 0, 1, 2 or 3 via `RXParam_Sync_tol`.
- Value: The Sync word value is configured in `SYNCParm_Sync_value`.

5.2.4. Packet Handler

The packet handler is the block used in Packet mode. Its functionality is fully described in section 5.5.

5.2.5. Control

The control block configures and controls the full chip's behavior according to the settings programmed in the configuration registers.

5.3. Continuous Mode

5.3.1. General Description

As illustrated in Figure 27, in Continuous mode the NRZ data from the demodulator is directly accessed by the uC on the DATA pin (20). The SPI Data, FIFO and packet handler are thus inactive.

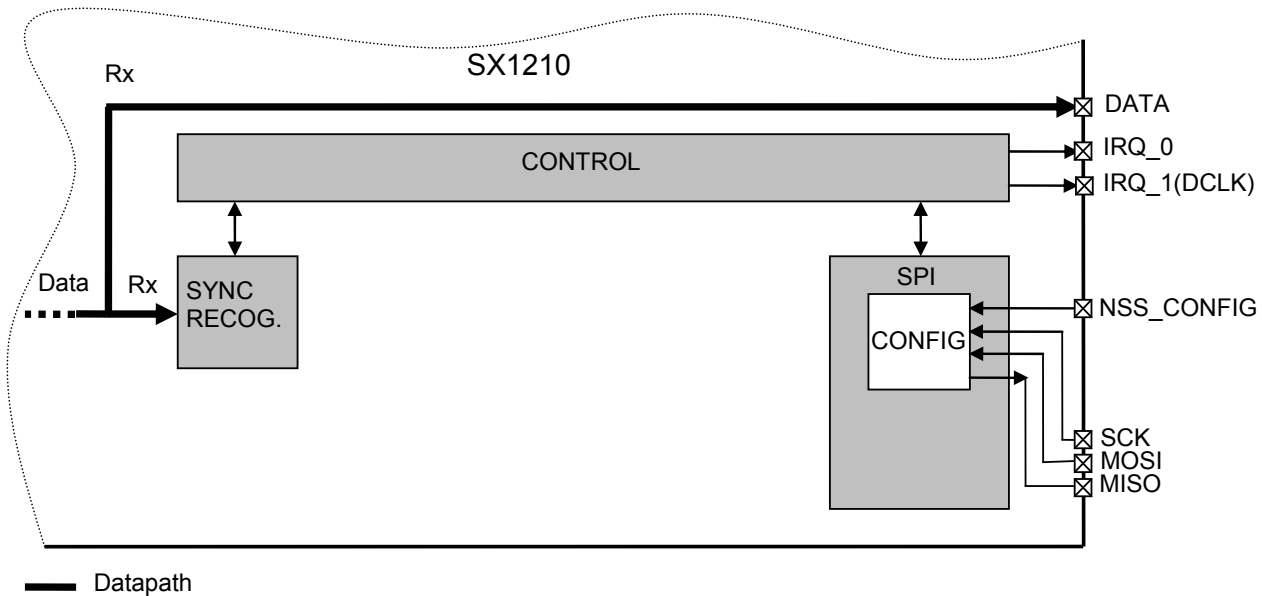


Figure 27: Continuous Mode Conceptual View

5.3.2. Rx Processing

If the bit synchronizer is disabled, the raw demodulator output is made directly available on DATA pin and no DCLK signal is provided.

Conversely, if the bit synchronizer is enabled, synchronous cleaned data and clock are made available respectively on DATA and IRQ_1 pins. DATA is sampled on the rising edge of DCLK and updated on the falling edge as illustrated in Figure 28.

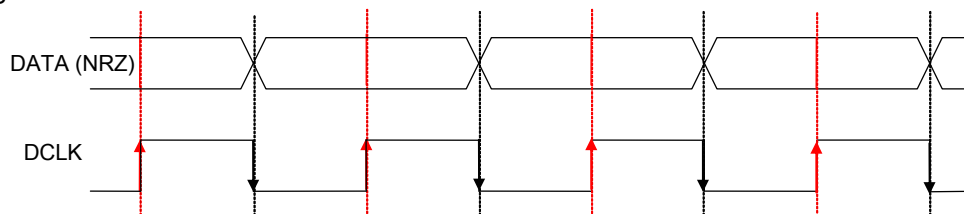


Figure 28: Rx Processing in Continuous Mode

Note that in Continuous mode it is always recommended to enable the bit synchronizer to clean the DATA signal even if the DCLK signal is not used by the uC. (bit synchronizer is automatically enabled in Buffered and Packet mode).

5.3.3. Interrupt Signals Mapping

The tables below give the description of the interrupts available in Continuous mode.

	Rx_stby_irq_0	Rx
IRQ_0	00 (d)	Sync
	01	RSSI
	1x	-
IRQ_1		DCLK

Table 15: Interrupt Mapping in Continuous Rx Mode

Note: In Continuous mode, no interrupt is available in Stby mode

5.3.4. uC Connections

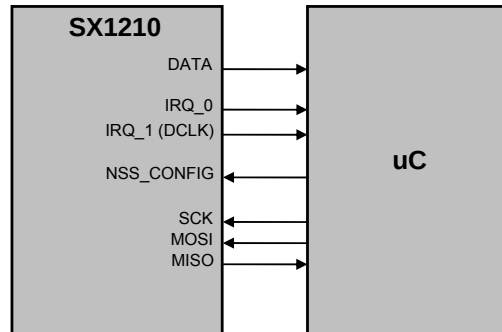


Figure 29: uC Connections in Continuous Mode

Note that some connections may not be needed depending on the application:

- IRQ_0: if Sync and RSSI interrupts are not used. In this case, leave floating.
- IRQ_1: DCLK connection is not compulsory. In this case, leave floating.
- MISO: if no read register access is needed. In this case, pull-up to VDD through a 100 kΩ resistor.

In addition, NSS_DATA pin (unused in continuous mode) should be pulled-up to VDD through a 100 kΩ resistor. Please refer to Table 11 for SX1210's pins configuration

5.3.5. Continuous Mode Example

- Configure all data processing related registers listed below appropriately. In this example we assume that both Bit synchronizer and Sync word recognition are on.

Table 16: Relevant Configuration Registers in Continuous Mode (data processing related only)

		Description
MCPParam	Data_mode_x	Defines data operation mode (→ Continuous)
IRQParam	Rx_stby_irq_0	Defines IRQ_0 source in Rx mode
RXParam	Sync_on	Enables Sync word recognition
	Sync_size	Defines Sync word size
	Sync_tol	Defines the error tolerance on Sync word recognition
SYNCPParam	Sync_value	Defines Sync word value

- Program Rx interrupts: IRQ_0 mapped to Sync (Rx_stby_irq_0="00") and IRQ_1 mapped to DCLK (Bit synchronizer enabled)
- Go to Rx mode (note that Rx is not ready immediately, see Figure 40)
- Wait for Sync interrupt
- Get all packet bits on DATA pin synchronously with DCLK signal provided on IRQ_1
- Go to Sleep mode

5.4. Buffered Mode

5.4.1. General Description

As illustrated in Figure 30, for Buffered mode operation the NRZ data from the demodulator is not directly accessed by the uC but stored in the FIFO and accessed via the SPI Data interface. This frees the uC for other tasks between processing data from the SX1210, furthermore it simplifies software development and reduces uC performance requirements (speed, reactivity). Note that in this mode the packet handler stays inactive.

An important feature is also the ability to empty the FIFO in Stby mode, ensuring low power consumption and adding greater software flexibility.

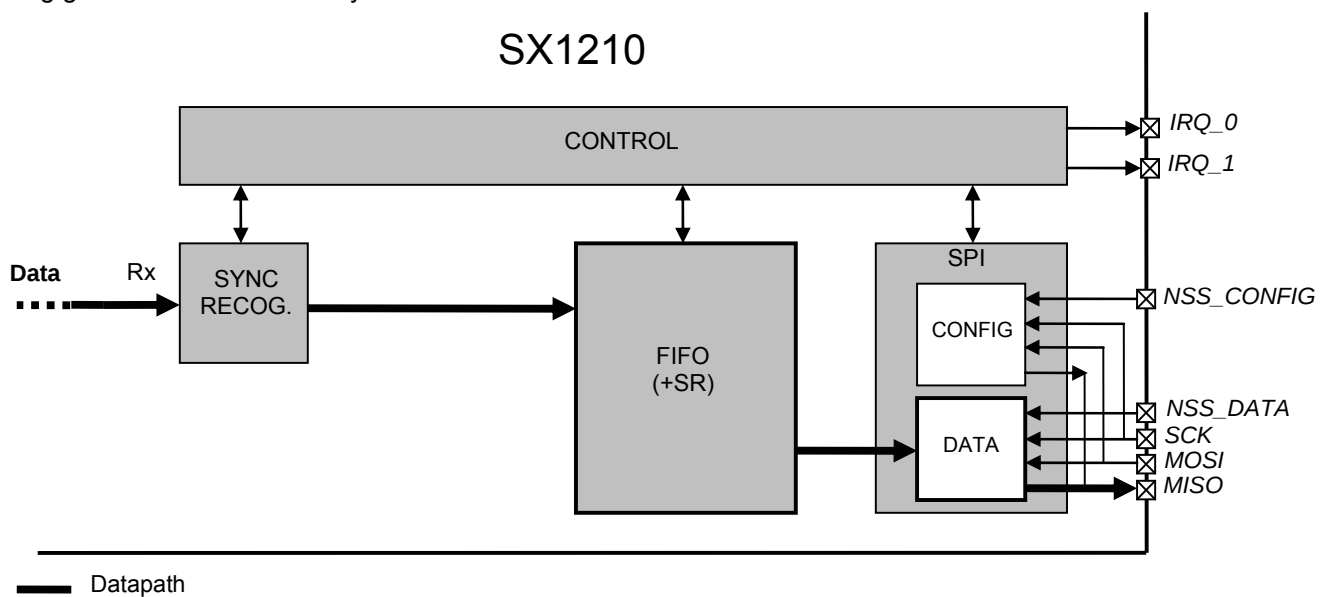


Figure 30: Buffered Mode Conceptual View

Note that Bit Synchronizer is automatically enabled in Buffered mode. The Sync word recognition must be enabled (RXParam_Sync_on=1) independently of the FIFO filling method selected (IRQParam_Fifo_fill_method).

5.4.2. Rx Processing

After entering Rx in Buffered mode, the chip requires the uC to retrieve the received data from the FIFO. The FIFO will actually start being filled with received bytes either; when a Sync word has been detected (in this case only the bytes following the Sync word are filled into the FIFO) or when the Fifo_fill bit is asserted by the user - depending on the state of bit, IRQParam_Fifo_fill_method.

In Buffered mode, the packet length is not limited i.e. as long as Fifo_fill is set, the received bytes are shifted into the FIFO.

The uC software must therefore manage the transfer of the FIFO contents by interrupt and ensure reception of the correct number of bytes. (In this mode, even if the remote transmitter has stopped, the demodulator will output random bits from noise)

When the FIFO is full, Fifofull IRQ source is asserted to alert the uC, that at that time, the FIFO can still be unfilled without data loss. If the FIFO is not unfilled, once the SR is also full (i.e. 8 bits periods later) Fifo_overnrnrn_clr is asserted and SR's content is lost.

Figure 31 illustrates an Rx processing with a 16 bytes FIFO size and Fifo_fill_method=0. Please note that in the illustrative example of section 5.4.5, the uC does not retrieve any byte from the FIFO through SPI Data, causing overrun.

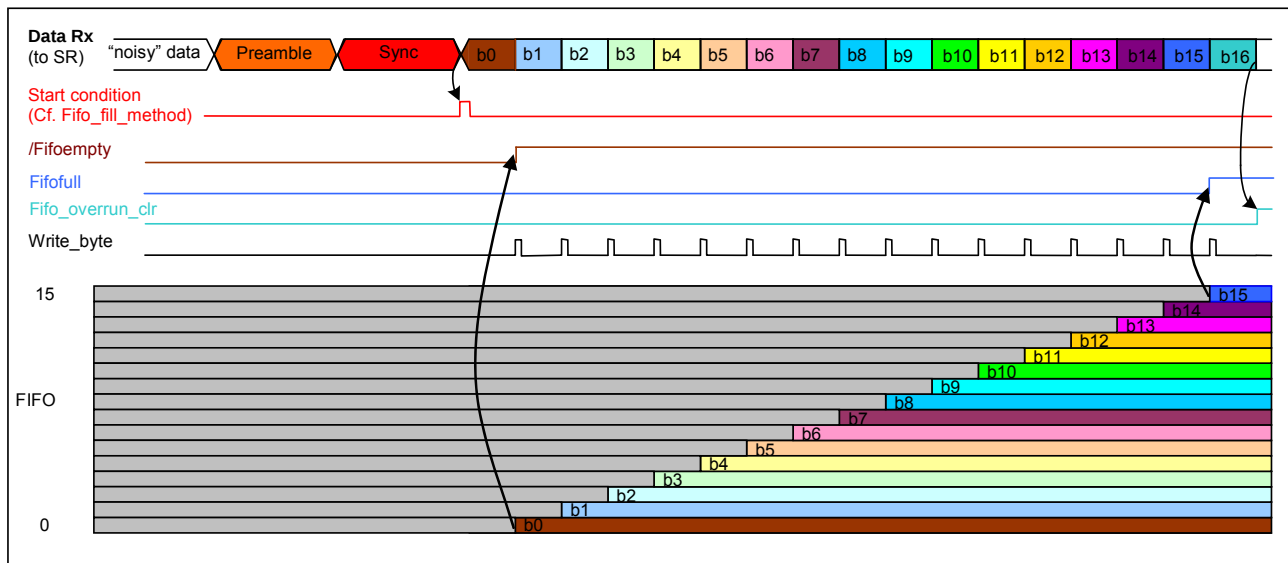


Figure 31: Rx Processing in Buffered Mode (FIFO size=16, Fifo_fill_method=0)

5.4.3. Interrupt Signals Mapping

The tables below describe the interrupts available in Buffered mode.

	Rx_stby_irq_x	Rx	Stby
IRQ_0	00 (d)	-	-
	01	Write_byte	-
	10	/Fifoempty	/Fifoempty
	11	Sync	-
IRQ_1	00 (d)	-	-
	01	Fifofull	Fifofull
	10	RSSI	-
	11	Fifo_threshold	Fifo_threshold

Table 17: Interrupt Mapping in Buffered Rx and Stby Modes

5.4.4. uC Connections

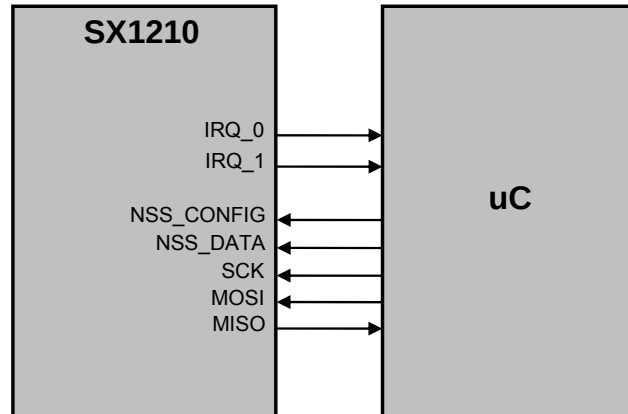


Figure 32: uC Connections in Buffered Mode

Note that depending upon the application, some uC connections may not be needed:

- IRQ_0: if none of the relevant IRQ sources are used. In this case, leave floating.
- IRQ_1: if none of the relevant IRQ sources are used. In this case, leave floating.

In addition, DATA pin (unused in buffered mode) should be pulled-up to VDD through a 100 kΩ resistor. Please refer to Table 11 for the SX1210's pin configuration.

5.4.5. Buffered Mode Example

- Configure all data processing related registers listed below appropriately. In this example we assume Sync word recognition is on and Fifo_fill_method=0.

		Description
MCPParam	Data_mode_x	Defines data operation mode (→Buffered)
	Fifo_size	Defines FIFO size
	Fifo_thresh	Defines FIFO threshold
IRQParam	Rx_stby_irq_0	Defines IRQ_0 source in Rx & Stby modes
	Rx_stby_irq_1	Defines IRQ_1 source in Rx & Stby modes
	Fifo_fill_method	Defines FIFO filling method
	Fifo_fill	Controls FIFO filling status
RXParam	Sync_size	Defines Sync word size
	Sync_tol	Defines the error tolerance on Sync word detection
SYNCPParam	Sync_value	Defines Sync word value

Table 18: Relevant Configuration Registers in Buffered Mode (data processing related only)

- Program Rx/Stby interrupts: IRQ_0 mapped to /Fifoempty (Rx_stby_irq_0=10) and IRQ_1 mapped to Fifo_threshold (Rx_stby_irq_1=01). Configure Fifo_thresh to an appropriate value (ex: to detect packet end if its length is known)
- Go to Rx mode (note that Rx is not ready immediately, Cf section 7.3.1).
- Wait for Fifo_threshold interrupt (i.e. Sync word has been detected and FIFO filled up to the defined threshold).
- If it is packet end, go to Stby (SR's content is lost).
- Read packet bytes from FIFO until /Fifoempty goes low (or correct number of bytes is read).
- Go to Sleep mode.

5.5. Packet Mode

5.5.1. General Description

Similar to Buffered mode operation, in Packet mode the NRZ data from the demodulator is not directly accessed by the uC but stored in the FIFO and accessed via the SPI Data interface.

In addition, the SX1210's packet handler performs several packet oriented tasks such as Preamble and Sync word extraction, CRC check, dewhitening of data, address filtering, etc. This simplifies still further software and reduces uC overhead by performing these repetitive tasks within the RF chip itself.

Another important feature is ability to empty the FIFO in Stby mode, ensuring optimum power consumption and adding more flexibility for the software.

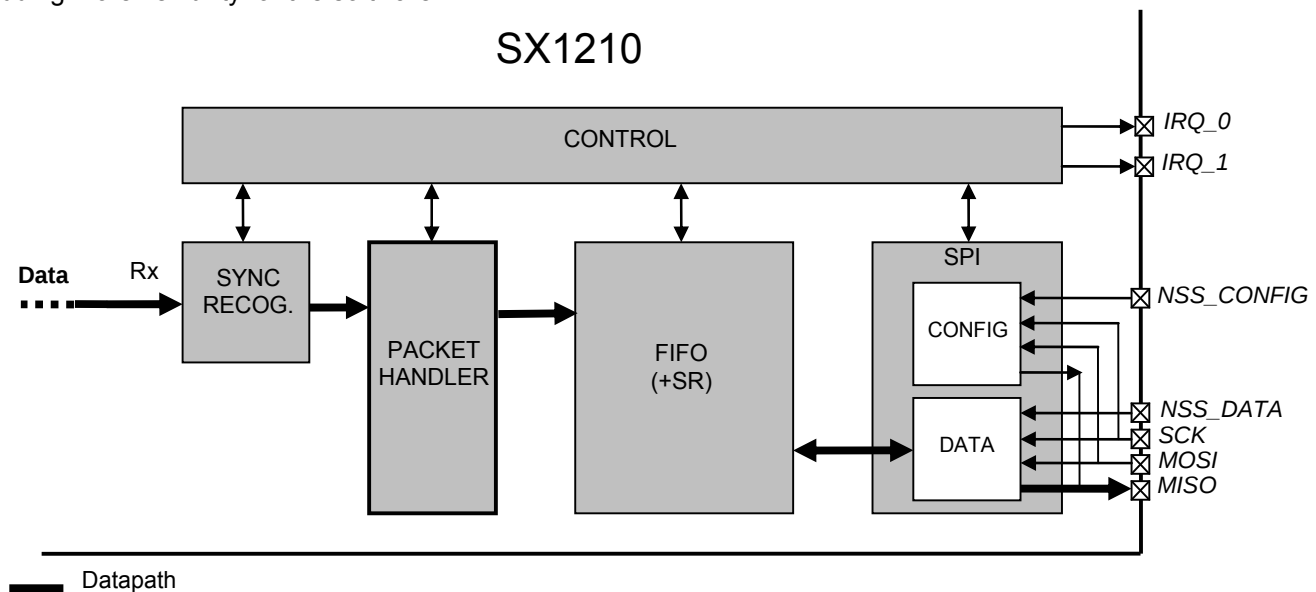


Figure 33: Packet Mode Conceptual View

Note that Bit Synchronizer and Sync word recognition are automatically enabled in Packet mode.

5.5.2. Packet Format

Two types of packet formats are supported: fixed length and variable length, selectable by the PKTParam_Pkt_format bit. The maximum size of the payload is limited by the size of the FIFO selected (16, 32, 48 or 64 bytes).

5.5.2.1. Fixed Length Packet Format

In applications where the packet length is fixed in advance, this mode of operation may be of interest to minimize RF overhead (no length byte field is required). All nodes should be programmed with the same packet length value.

The length of the payload is set by the PKTParam_Payload_length register and is limited by the size of the FIFO selected.

The length stored in this register relates only to the payload which includes the message and the optional address byte. In this mode, the payload must contain at least one byte, i.e. address or message byte.

An illustration of a fixed length packet is shown in Figure 34. It contains the following fields:

- Preamble (1010...).
- Sync word (Network ID).
- Optional Address byte (Node ID).
- Message data.
- Optional 2-bytes CRC checksum.

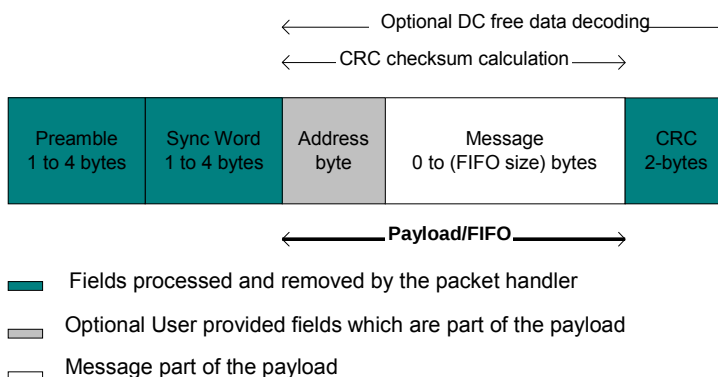


Figure 34: Fixed Length Packet Format

5.5.2.2. Variable Length Packet Format

This mode is necessary in applications where the length of the packet is not known in advance and can vary over time. It is then necessary for the transmitter to send the length information together with each packet in order for the receiver to operate properly.

In this mode the length of the payload, indicated by the length byte in Figure 35, is given by the first byte of the FIFO and is limited only by the size (width of 8bits) of the FIFO selected. Note that the length byte itself is not included in its calculation. In this mode, the payload must contain at least 2 bytes, i.e. length + address or message byte.

An illustration of a variable length packet is shown in Figure 35. It contains the following fields:

- Preamble (1010...).
- Sync word (Network ID).
- Length byte
- Optional Address byte (Node ID).
- Message data.
- Optional 2-bytes CRC checksum.

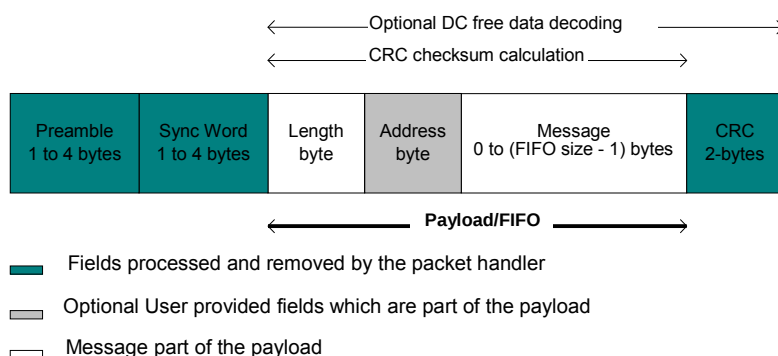


Figure 35: Variable Length Packet Format

5.5.3. Rx Processing

In Rx mode the packet handler extracts the user payload to the FIFO by performing the following operations:

- Receiving the preamble and stripping it off.
- Detecting the Sync word and stripping it off.
- Optional DC-free decoding of data.
- Optionally checking the address byte.
- Optionally checking CRC and reflecting the result on CRC_status bit and CRC_OK IRQ source.

Only the payload (including optional address and length fields) is made available in the FIFO.

Payload_ready and CRC_OK interrupts (the latter only if CRC is enabled) can be generated to indicate the end of the packet reception.

By default, if the CRC check is enabled and fails for the current packet, then the FIFO is automatically cleared and neither of the two interrupts are generated and new packet reception is started. This autoclear function can be disabled via PKTParam_CRC_autoclr bit and, in this case, even if CRC fails, the FIFO is not cleared and only Payload_ready IRQ source is asserted.

Once fully received, the payload can also be fully or partially retrieved in Stby mode via PKTParam_Fifo_stby_access. At the end of the reception, although the FIFO automatically stops being filled, it is still up to the user to explicitly exit Rx mode if required. (e.g. go to Stby to get payload). FIFO must be empty for a new packet reception to start.

5.5.4. Packet Filtering

SX1210's packet handler offers several mechanisms for packet filtering ensuring that only useful packets are made available to the uC, reducing significantly system power consumption and software complexity.

5.5.4.1. Sync Word Based

Sync word filtering/recognition is automatically enabled in Packet mode. It is used for identifying the start of the payload and also for network identification. As previously described, the Sync word recognition block is configured (size, error tolerance, value) via RXParam_Sync_size, RXParam_Sync_tol and SYNCParam configuration registers. This information is used to filter packets in Rx.

Every received packet which does not start with this locally configured Sync word is automatically discarded and no interrupt is generated.

When the Sync word is detected, payload reception automatically starts and Sync IRQ source is asserted.

5.5.4.2. Address Based

Address filtering can be enabled via the PKTParam_Adrs_filt bits. It adds another level of filtering, above Sync word, typically useful in a multi-node networks where a network ID is shared between all nodes (Sync word) and each node has its own ID (address).

Three address based filtering options are available:

- Adrs_filt = 01: Received address field is compared with internal register Node_Adrs. If they match then the packet is accepted and processed, otherwise it is discarded.
- Adrs_filt = 10: Received address field is compared with internal register Node_Adrs and the constant 0x00. If either is a match, the received packet is accepted and processed, otherwise it is discarded. This additional check with a constant is useful for implementing broadcast in a multi-node networks.
- Adrs_filt = 11: Received address field is compared with internal register Node_Adrs and the constants 0x00 & 0xFF. If any of the three matches, then the received packet is accepted and processed, otherwise it is discarded. These additional checks with constants are useful for implementing broadcast commands of all nodes.

Please note that the received address byte, as part of the payload, is not stripped off the packet and is made available in the FIFO.

5.5.4.3. Length Based

In variable length Packet mode, PKTParam_Payload_length must be programmed with the maximum length permitted. If received length byte is smaller than this maximum then the packet is accepted and processed, otherwise it is discarded.

Please note that the received length byte, as part of the payload, is not stripped off the packet and is made available in the FIFO.

To disable this function the user should set the value of the PKTParam_Payload_length to the value of the FIFO size selected.

5.5.4.4. CRC Based

The CRC check is enabled by setting bit PKTParam_CRC_on. It is used for checking the integrity of the message.

- On your Tx side a two byte CRC checksum should be calculated on the payload part of the packet and appended to the end of the message.
- On SX1210 (Rx side) the checksum is calculated on the received payload and compared with the two checksum bytes received. The result of the comparison is stored in the PKTParam_CRC_status bit and CRC_OK IRQ source.

By default, if the CRC check fails then the FIFO is automatically cleared and no interrupt is generated. This filtering function can be disabled via PKTParam_CRC_autocl_r bit and in this case, even if CRC fails, the FIFO is not cleared and only Payload_ready interrupt goes high. Please note that in both cases, the two CRC checksum bytes are stripped off by the packet handler and only the payload is made available in the FIFO.

The CRC is based on the CCITT polynomial as shown in Figure 36. This implementation also detects errors due to leading and trailing zeros.

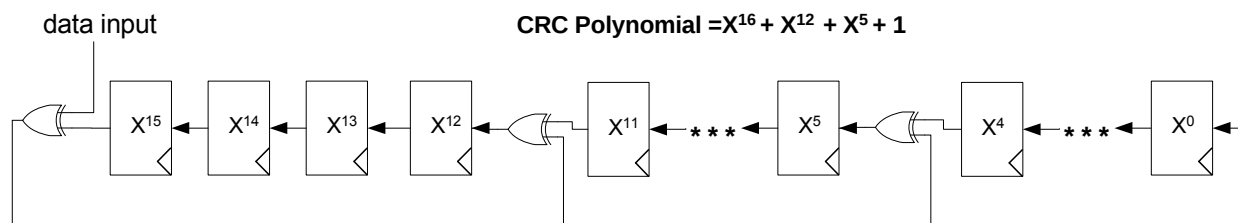


Figure 36: CRC Implementation

5.5.5. DC-Free Data Mechanisms

Two techniques are supported by the SX1210 packet handler: Manchester decoding and data whitening. Please note that only one of the two methods should be enabled at a time.

5.5.5.1. Manchester Decoding

Manchester decoding is enabled by setting bit PKTParam_Manchester_on and can only be used in Packet mode.

The NRZ data to Manchester codes '1' as "10" and '0' as "01".

In this case, the maximum chip rate is the maximum bit rate given in the specifications section and the actual bit rate is half the chip rate.

Manchester decoding is only applied to the payload and CRC checksum while preamble and Sync word are kept NRZ. However, the chip rate from preamble to CRC is the same and defined by MCPParam_BR (Chip Rate = Bit Rate NRZ = 2 x Bit Rate Manchester).

Manchester decoding is thus made transparent for the user, who still retrieves NRZ data from the FIFO.

	1/BR ...Sync								1/BR Payload...										
RF chips @ BR	...	1	1	1	0	1	0	0	1	0	0	1	0	1	1	0	1	0	...
User/NRZ bits	...	1	1	1	0	1	0	0	1	0	0	1	0	1	1	0	1	0	...
Manchester OFF	...	1	1	1	0	1	0	0	1	0	0	1	0	1	1	0	1	0	...
User/NRZ bits	...	1	1	1	0	1	0	0	1	0	0	1	0	1	1	0	1	0	...
Manchester ON	...	1	1	1	0	1	0	0	1	0	0	1	0	1	1	0	1	0	...

Figure 37: Manchester Decoding

5.5.5.2. Data Dewhitening

Another technique called whitening or scrambling is widely used for randomizing the user data before radio transmission. The data is whitened using a random sequence on the Tx side and de-whitened on the SX1210 (Rx side) using the same sequence. Comparing to Manchester technique it has the advantage of keeping NRZ data rate i.e. actual bit rate is not halved.

SX1210 supported whitening algorithm is given in Figure 38. This figure provides you with the random sequence to be X-ORed with the actual payload.

The de-whitening process is enabled by setting bit PKTParam_Whitening_on. The data is de-whitened by the SX1210 receiver side by XORing with the same random sequence as the Tx.

Payload de-whitening is thus made transparent for the user, who still retrieves NRZ data from the FIFO.

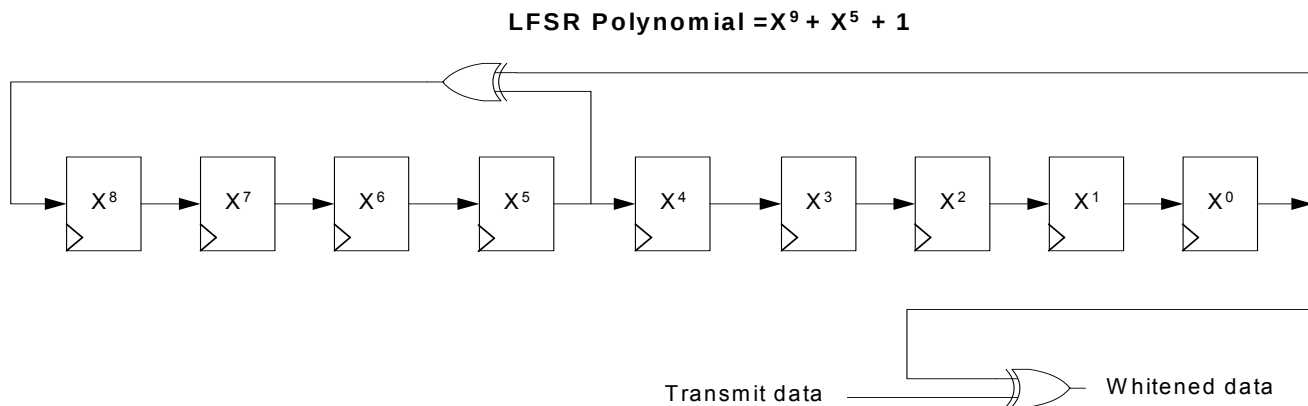


Figure 38: Data Whitening Implementation

5.5.6. Interrupt Signal Mapping

Tables below give the description of the interrupts available in Packet mode.

Table 19: Interrupt Mapping in Rx and Stby in Packet Mode

	Rx_stby_irq_x	Rx	Stby
IRQ_0	00 (d)	Payload_ready	-
	01	Write_byte	-
	10	/Fifoempty	/Fifoempty
	11	Sync or Adrs_match*	-
IRQ_1	00 (d)	CRC_OK	-
	01	Fifofull	Fifofull
	10	RSSI	-
	11	Fifo_threshold	Fifo_threshold

*The latter if Address filtering is enabled

5.5.7. uC Connections

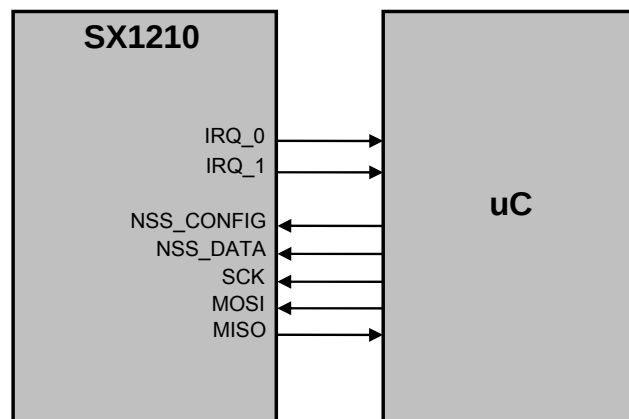


Figure 39: uC Connections in Packet Mode

Note that depending upon the application, some uC connections may not be needed:

- IRQ_0: if none of the relevant IRQ sources are used. In this case, leave floating.

- IRQ_1: if none of the relevant IRQ sources are used. In this case, leave floating.

In addition, DATA pin (unused in packet mode) should be pulled-up to VDD through a 100 k Ω resistor. Please refer to Table 11 for the SX1210's pin configuration.

5.5.8. Packet Mode Example

- Configure all data processing related registers listed below appropriately. In this example we assume CRC is enabled with autoclear on.

Table 20: Relevant Configuration Registers in Packet Mode (data processing related only)

		Description
MCPParam	Data_mode_x	Defines data operation mode (→Packet)
	Fifo_size	Defines FIFO size
	Fifo_thresh	Defines FIFO threshold
IRQParam	Rx_stby_irq_0	Defines IRQ_0 source in Rx & Stby modes
	Rx_stby_irq_1	Defines IRQ_1 source in Rx & Stby modes
RXParam	Sync_size	Defines Sync word size
	Sync_tol	Defines the error tolerance on Sync word detection
SYNCPParam	Sync_value	Defines Sync word value
PKTPParam	Manchester_on	Enables Manchester decoding
	Payload_length	Length in fixed format, max length in variable format
	Node_adrs	Defines node address for address filtering
	Pkt_format	Defines packet format (fixed or variable length)
	Whitening_on	Enables de-whitening process
	CRC_on	Enables CRC calculation/check
	Adrs_filt	Enables and defines address filtering
	CRC_autoclr	Enables FIFO autoclear if CRC failed

Rx Mode:

- Program Rx/Stby interrupts: IRQ_0 mapped to /Fifoempty (Rx_stby_irq_0=10) and IRQ_1 mapped to CRC_OK (Rx_stby_irq_1=00)
- Go to Rx (note that Rx is not ready immediately, see section 7.3.1)
- Wait for CRC_OK interrupt
- Go to Stby
- Read payload bytes from FIFO until /Fifoempty goes low.
- Go to Sleep mode

5.5.9. Additional Information

It is not possible to receive multiple packets. Once a packet has been received and filled into the FIFO all its content needs to be read i.e. the FIFO must be empty for a new packet reception to be initiated.

The Payload_ready interrupt goes high when the last payload byte is available in the FIFO and remains high until all its data are read. Similar behavior is applicable to Adrs_match and CRC_OK interrupts.

The CRC result is available in the CRC_status bit as soon as the CRC_successful and Payload_ready interrupt sources are triggered. In Rx mode, CRC_status is cleared when the complete payload has been read from the FIFO. If the payload is read in Stby mode, then CRC_status is cleared when the user goes back to Rx mode and a new Sync word is detected.

The Fifo_fill_method and Fifo_fill bits don't have any meaning in the Packet mode and should be set to their default values only.

6. Configuration and Status Registers

6.1. General Description

Table 21 sums-up the control and status registers of the SX1210:

Table 21: Registers List

Name	Size	Address	Description
MCPParam	13 x 8	0 - 12	Main parameters
IRQParam	3 x 8	13 - 15	Interrupt registers
RXParam	6 x 8	16 - 21	Receiver parameters
SYNCParm	4 x 8	22 - 25	Pattern
Reserved	1 x 8	26	Do not change default value : "01111110"
OSCParm	1 x 8	27	Crystal oscillator parameters
PKTParm	4 x 8	28 - 31	Packet handler parameters

6.2. Main Configuration Register - MCPParam

The detailed description of the MCPParam register is given in Table 22.

Table 22: MCPParam Register Description

Name	Bits	Address (d)	RW	Description
Chip_mode	7-5	0	r/w	Transceiver mode: 000 → sleep mode - Sleep 001 → stand-by mode - Stby (d) 010 → frequency synthesizer mode - FS 011 → receive mode - Rx
Freq_band	4-3	0	r/w	Frequency band: 00 → 902 – 915 MHz 01 → 915 – 928 MHz (d) 10 → 950 – 960 MHz or 863 - 870 MHz (Application Circuit dependant)
VCO_trim	2-1	0	r/w	Fine VCO trimming: 00 → Vtune determined by tank inductors values (d) 01 → Vtune + 60 mV typ. 10 → Vtune + 120 mV typ. 11 → Vtune + 180 mV typ.
RPS_select	0	0	r/w	Selection between the two sets of frequency dividers of the PLL, Ri/Pi/Si 0 → R1/P1/S1 selected(d) 1 → R2/P2/S2 selected
Modul_select	7-6	1	r/w	Modulation type: 01 → OOK 10 → FSK (d)
Data_mode_0	5	1	r/w	Data operation mode LSB (refer to Data_Mode_1 (Bit 2 Addr 1)
OOK_thresh_type	4-3	1	r/w	OOK demodulator threshold type: 00 → fixed threshold mode 01 → peak mode (d) 10 → average mode 11 → reserved

Data_mode_1	2	1	r/w	Data operation mode's MSB. Cf. Data_mode_0 (Bit 5 Addr 1)		
				Data_mode_1 Bit 2 addr 1	Data_mode_0 Bit 5 addr 1	Data Operation Mode
				0	0	Continuous (d)
				0	1	Buffered
				1	x	Packet
IF_gain	1-0	1	r/w	Gain on the IF chain: 00 → maximal gain (0dB) (d) 01 → -4.5 dB 10 → -9dB 11 → -13.5 dB		
Freq_dev	7-0	2	r/w	Single side frequency deviation: $Fdev = \frac{f_{XTAL}}{32 \cdot (D + 1)}, 0 \leq D \leq 255$, where D is the value in the register. (d): D = "00000011" => Fdev = 100 kHz		
Res	7	3	r/w	Reserved (d): "0"		
BR	6-0	3	r/w	Bit Rate = $\frac{f_{XTAL}}{64 \cdot (C + 1)}, 0 \leq C \leq 127$, where C is the value in the register. (d): C = "00001111" => Bit Rate = 25 kb/s NRZ		
OOK_floor_thresh	7-0	4	r/w	Floor threshold in OOK Rx mode. By default 6 dB. (d): "00001100" assuming 0.5 dB RSSI step		
Fifo_size	7:6	5	r/w	FIFO size selection: 00 → 16 bytes (d) 01 → 32 bytes 10 → 48 bytes 11 → 64 bytes		
Fifo_thresh	5-0	5	r/w	FIFO threshold for interrupt source (Cf section 5.2.2.3) (d): B = "001111"		
R1	7-0	6	r/w	R counter, active when RPS_select="0" (d): 77h; default values of R1, P1, S1 generate 915.0 MHz in FSK mode		
P1	7-0	7	r/w	P counter, active when RPS_select="0" (d): 64h; default values of R1, P1, S1 generate 915.0 MHz in FSK mode		
S1	7-0	8	r/w	S counter, active when RPS_select="0" (d): 32h; default values of R1, P1, S1 generate 915.0 MHz in FSK mode		
R2	7-0	9	r/w	R counter, active when RPS_select="1" (d): 74h; default values of R2, P2, S2 generate 920.0 MHz in FSK mode		
P2	7-0	10	r/w	P counter, active when RPS_select="1" (d): 62h; default values of R2, P2, S2 generate 920.0 MHz in FSK mode		
S2	7-0	11	r/w	S counter, active when RPS_select="1" (d): 32h; default values of R2, P2, S2 generate 920.0 MHz in FSK mode		
Res	7-5	12	r/w	Reserved (d): "00111000"		

6.3. Interrupt Configuration Parameters - IRQParam

The detailed description of the IRQParam register is given in Table 23.

Table 23: IRQParam Register Description

Name	Bits	Address (d)	RW	Description
Rx_stby_irq_0	7-6	13	r/w	IRQ_0 source in Rx and Standby modes: If Data_mode(1:0) = 00 (Continuous mode): 00 → Sync (d) 01 → RSSI 10 → Sync 11 → Sync If Data_mode(1:0) = 01 (Buffered mode): 00 → - (d) 01 → Write_byte 10 → /Fifoempty* 11 → Sync If Data_mode(1:0) = 1x (Packet mode): 00 → Payload_ready (d) 01 → Write_byte 10 → /Fifoempty* 11 → Sync or Adrs_match (the latter if address filtering is enabled) *also available in Standby mode (Cf sections 5.4.3 and 5.5.6)
Rx_stby_irq_1	5-4	13	r/w	IRQ_1 source in Rx and Standby modes: If Data_mode(1:0) = 00 (Continuous mode): xx → DCLK If Data_mode(1:0) = 01 (Buffered mode): 00 → - (d) 01 → Fifofull* 10 → RSSI 11 → Fifo_threshold* If Data_mode(1:0) = 1x (Packet mode): 00 → CRC_ok (d) 01 → Fifofull* 10 → RSSI 11 → Fifo_threshold* *also available in Standby mode (Cf sections 5.4.3 and 5.5.6)
Fifofull	2	13	r	Fifofull IRQ source Goes high when FIFO is full.
/Fifoempty	1	13	r	/Fifoempty IRQ source Goes low when FIFO is empty
Fifo_overrun_clr	0	13	r/w/c	Goes high when an overrun error occurred. Writing a 1 clears flag and FIFO
Fifo_fill_method	7	14	r/w	FIFO filling method (Buffered mode only): 0 → Automatically starts when a sync word is detected (d) 1 → Manually controlled by Fifo_fill
Fifo_fill	6	14	r/w/c	FIFO filling status/control (Buffered mode only): If Fifo_fill_method = '0': (d) Goes high when FIFO is being filled (sync word has been detected) Writing '1' clears the bit and waits for a new sync word (if Fifo_overrun_clr=0)

				If Fifo_fill_method = '1': 0 → Stop filling the FIFO 1 → Start filling the FIFO
Res	5	14	r	
Res	4-3	14	r/w	(d): "00"
RSSI_irq	2	14	r/w/ c	RSSI IRQ source: Goes high when a signal above RSSI_irq_thresh is detected Writing '1' clears the bit
PLL_locked	1	14	r/w/ c	PLL status: 0 → not locked 1 → locked Writing a '1' clears the bit
PLL_lock_en	0	14	r/w	PLL_lock detect flag mapped to pin 23: 0 → Lock detect disabled, pin 23 is High-Z 1 → Lock detect enabled(d)
RSSI_irq_thresh	7-0	15		RSSI threshold for interrupt (coded as RSSI) (d): "00000000"

6.4. Receiver Configuration parameters - RXParam

The detailed description of the RXParam register is given in Table 24.

Table 24: RXParam Register Description

Name	Bits	Address (d)	RW	Description
PassiveFilt	7-4	16	r/w	Typical single sideband bandwidth of the passive low-pass filter. PassiveFilt = 0000 → 65 kHz 0001 → 82 kHz 0010 → 109 kHz 0011 → 137 kHz 0100 → 157 kHz 0101 → 184 kHz 0110 → 211 kHz 0111 → 234 kHz 1000 → 262 kHz 1001 → 321 kHz 1010 → 378 kHz (d) 1011 → 414 kHz 1100 → 458 kHz 1101 → 514 kHz 1110 → 676 kHz 1111 → 987 kHz
ButterFilt	3-0	16	r/w	Sets the receiver bandwidth. For BW information please refer to sections 3.3.5 (FSK) and 3.3.6 (OOK). $f_c = f_0 + 200kHz \cdot \frac{f_{xtal} MHz}{12.8MHz} \cdot \frac{1 + Val(ButterFilt)}{8}$ (d): "0011" => $f_c = 200$ kHz
PolypFilt_center	7-4	17	r/w	Central frequency of the polyphase filter (100kHz recommended): $f_0 = 200kHz \cdot \frac{F_{xtal} MHz}{12.8MHz} \cdot \frac{1 + Val(PolypFilt_center)}{8}$ (d): "0011" => $f_0 = 100$ kHz
Res	3-0	17	r/w	Reserved (d): "1000"
PolypFilt_on	7	18	r/w	Enable of the polyphase filter, in OOK Rx mode: 0 → off (d) 1 → on
Bitsync_off	6	18	r/w	Bit synchronizer: control in Continuous Rx mode: 0 → on (d) 1 → off
Sync_on	5	18	r/w	Sync word recognition: 0 → off (d) 1 → on
Sync_size	4-3	18	r/w	Sync word size: 00 → 8 bits 01 → 16 bits 10 → 24 bits 11 → 32 bits (d)
Sync_tol	2-1	18	r/w	Number of errors tolerated in the Sync word recognition: 00 → 0 error (d) 01 → 1 error 10 → 2 errors 11 → 3 errors
Res	0	18	r/w	Reserved (d): "0"

Name	Bits	Address (d)	RW	Description
Res	7-0	19	r/w	Reserved (d): "00000111"
RSSI_val	7-0	20	r	RSSI output, 0.5 dB / bit Note: READ-ONLY (not to be written)
OOK_thresh_step	7-5	21	r/w	Size of each decrement of the RSSI threshold in the OOK demodulator 000 → 0.5 dB (d) 100 → 3.0 dB 001 → 1.0 dB 101 → 4.0 dB 010 → 1.5 dB 110 → 5.0 dB 011 → 2.0 dB 111 → 6.0 dB
OOK_thresh_dec_period	4-2	21	r/w	Period of decrement of the RSSI threshold in the OOK demodulator: 000 → once in each chip period (d) 001 → once in 2 chip periods 010 → once in 4 chip periods 011 → once in 8 chip periods 100 → twice in each chip period 101 → 4 times in each chip period 110 → 8 times in each chip period 111 → 16 times in each chip period
OOK_avg_thresh_cutoff	1-0	21	r/w	Cutoff frequency of the averaging for the average mode of the OOK threshold in demodulator 00 → $f_C \approx BR / 8.\pi$ (d) 01 → Reserved 10 → Reserved 11 → $f_C \approx BR / 32.\pi$

6.5. Sync Word Parameters - SYNCParam

The detailed description of the SYNCParam register is given in Table 25.

Table 25: SYNCParam Register Description

Name	Bits	Address (d)	RW	Description
Sync_value(31:24)	7-0	22	r/w	1 st Byte of Sync word (d): "00000000"
Sync_value(23:16)	7-0	23		2 nd Byte of Sync word (only used if Sync_size ≠ 00) (d): "00000000"
Sync_value(15:8)	7-0	24		3 rd Byte of Sync word (only used if Sync_size = 1x) (d): "00000000"
Sync_value(7:0)	7-0	25		4 th Byte of Sync word (only used if Sync_size = 11) (d): "00000000"

6.6. Oscillator Parameters - OSCParam

The detailed description of the OSCParam register is given in Table 26.

Table 26: OSCParam Register Description

Name	Bits	Address (d)	RW	Description
Clkout_on	7	27	r/w	Clkout control 0 → Disabled 1 → Enabled, Clk frequency set by Clkout_freq (d)
Clkout_freq	6-2	27	r/w	Frequency of the signal provided on CLKOUT: $f_{clkout} = f_{xtal}$ if Clkout_freq = "00000" $f_{clkout} = \frac{f_{xtal}}{2 \cdot Clkout_freq}$ otherwise (d): 01111 (= 427 kHz)
Res	1-0	27	r/w	Reserved (d): "00"

6.7. Packet Handling Parameters – PKTParam

The detailed description of the PKTParam register is given in Table 27.

Table 27: PKTParam Register Description

Name	Bits	Address (d)	RW	Description
Manchester_on	7	28	r/w	Enable Manchester decoding: 0 → off (d) 1 → on
Payload_length	6-0	28	r/w	If Pkt_format=0, payload length. If Pkt_format=1, max length (d): "0000000"
Node_adrs	7-0	29	r/w	Node's local address for filtering of received packets. (d): 00h
Pkt_format	7	30	r/w	Packet format: 0 → fixed length (d) 1 → variable length
Res	6-5	30	r/w	(d) : "10"
Whitening_on	4	30	r/w	Dewhitening process: 0 → off (d) 1 → on
CRC_on	3	30	r/w	CRC calculation/check: 0 → off 1 → on (d)
Adrs_filt	2-1	30	r/w	Address filtering of received packets: 00 → off (d) 01 → Node_adrs accepted, else rejected. 10 → Node_adrs & 0x00 accepted, else rejected. 11 → Node_adrs & 0x00 & 0xFF accepted, else rejected.
CRC_status	0	30	r	CRC check result for current packet (READ ONLY): 0 → Fail 1 → Pass
CRC_autoclr	7	31	r/w	FIFO auto clear if CRC failed for current packet: 0 → on (d) 1 → off
Res	6-0	31	r/w	Reserved (d): "0000000" recommended to set to "1000000"

7. Application Information

7.1. Crystal Resonator Specification

Table 28 shows the crystal resonator specification for the crystal reference oscillator circuit of the SX1210. This specification covers the full range of operation of the SX1210 and is employed in the reference design (see section 7.5.3).

Table 28: Crystal Resonator Specification

Name	Description	Min.	Typ.	Max.	Unit
Fxtal	Nominal frequency	9	12.800	15	MHz
Cload	Load capacitance for Fxtal	10	15	16.5	pF
Rm	Motional resistance	-	-	100	ohms
Co	Shunt capacitance	1	-	7	pF
ΔF_{xtal}	Calibration tolerance at 25+/-3°C	-15	-	+15	ppm
$\Delta F_{xtal}(\Delta T)$	Stability over temperature range [-40°C ; +85°C]	-20	-	+20	ppm
$\Delta F_{xtal}(\Delta t)$	Ageing tolerance in first 5 years	-2	-	+2	ppm/year

Note that the initial frequency tolerance, temperature stability and ageing performance should be chosen in accordance with the target operating temperature range and the receiver bandwidth selected.

7.2. Software for Frequency Calculation

The R1, P1, S1, and R2, P2, S2 dividers are configured over the SPI interface and programmed by 8 bits each, at addresses 6 to 11. The frequency pairs may hence be switched in a single SPI cycle.

7.2.1. GUI

To aid the user with calculating appropriate R, P and S values, software is available to perform the frequency calculation. The SX1210 PLL frequency Calculator Software can be downloaded from the Semtech website.

7.2.2. .dll for Automatic Production Bench

The Dynamically Linked Library (DLL) used by the software to perform these calculations is also provided, free of charge, to users, for inclusion in automatic production testing. Key benefits of this are:

- No hand trimming of the reference frequency required: the actual reference frequency of the Device Under Test (DUT) can be easily measured (e.g. from the CLKOUT output of the SX1210) and the tool will calculate the best frequencies to compensate for the crystal initial error.
- Channel plans can be calculated and stored in the application's memory, then adapted to the actual crystal oscillator frequency.

7.3. Switching Times and Procedures

As an ultra-low power device, the SX1210 can be configured for low minimum average power consumption. To minimize consumption the following optimized transitions between modes are shown.

7.3.1. Optimized Receive Cycle

The lowest-power Rx cycle is the following:

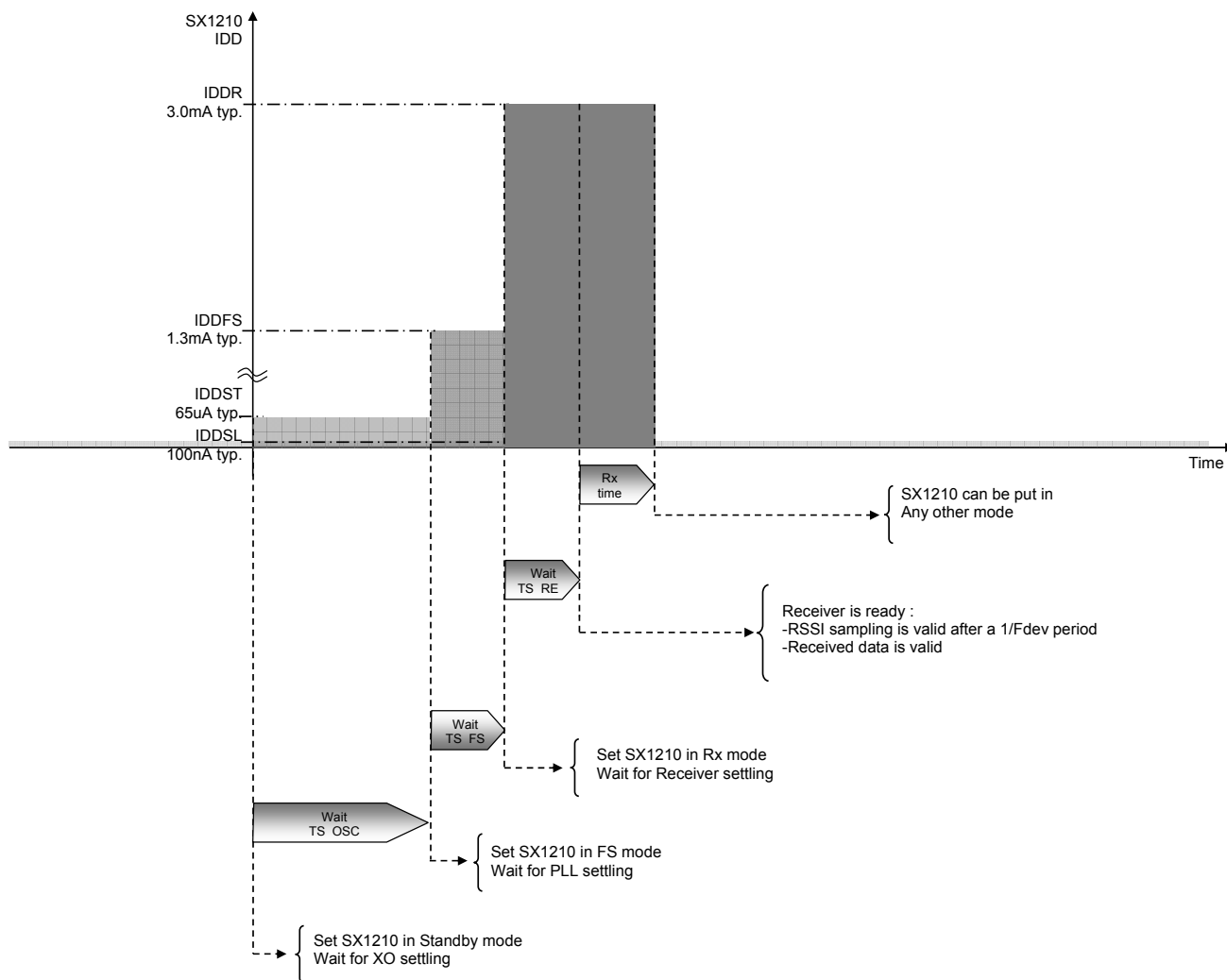


Figure 40: Optimized Rx Cycle

Note: If the lock detect indicator is available on an external interrupt pin of the companion uC, it can be used to optimize TS_FS, without having to wait the maximum specified TS_FS.

7.3.2. Receiver Frequency Hop Optimized Cycle

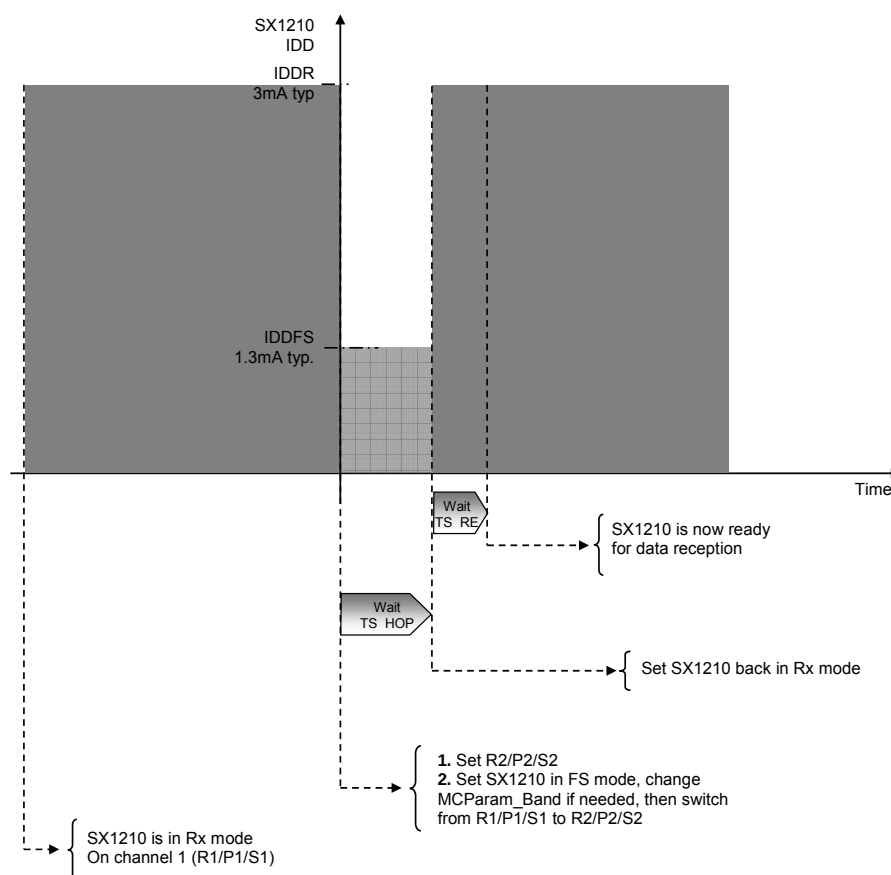


Figure 41: Rx Hop Cycle

Note: it is also possible to move from one channel to the other one without having to switch off the receiver. This method is faster, and overall draws more current. For timing information, please refer to TS_RE_HOP on Table 7.

7.4. Reset of the Chip

A power-on reset of the SX1210 is triggered at power up. Additionally, a manual reset can be issued by controlling pin 13.

7.4.1. POR

If the application requires the disconnection of VDD from the SX1210, despite of the extremely low Sleep Mode current, the user should wait for 10 ms from of the end of the POR cycle before commencing communications over the SPI bus. Pin 13 (TEST8) should be left floating during the POR sequence.

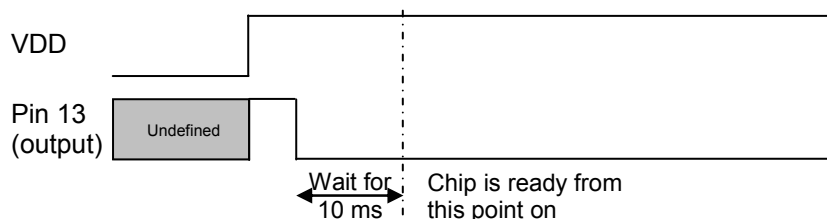


Figure 42: POR Timing Diagram

Please note that any CLKOUT activity can also be used to detect that the chip is ready.

7.4.2. Manual Reset

A manual reset of the SX1210 is possible even for applications in which VDD cannot be physically disconnected. Pin 13 should be pulled high for a hundred microseconds, and then released. The user should then wait for 5 ms before using the chip.

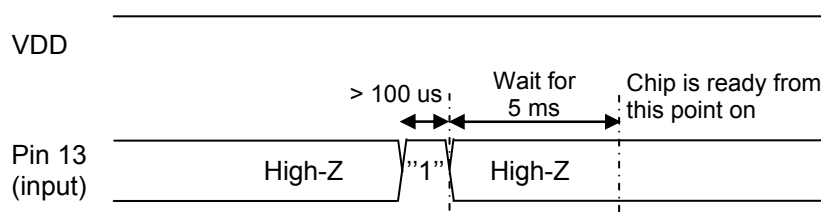


Figure 43: Manual Reset Timing Diagram

Please note that while pin 13 is driven high, an over current consumption of up to ten milliamps can be seen on VDD.

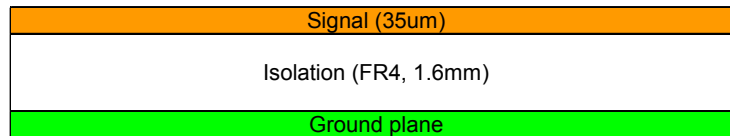


Figure 45: Reference Design's Stackup

The layout itself is illustrated in Figure 46. Please contact Semtech for gerber files.

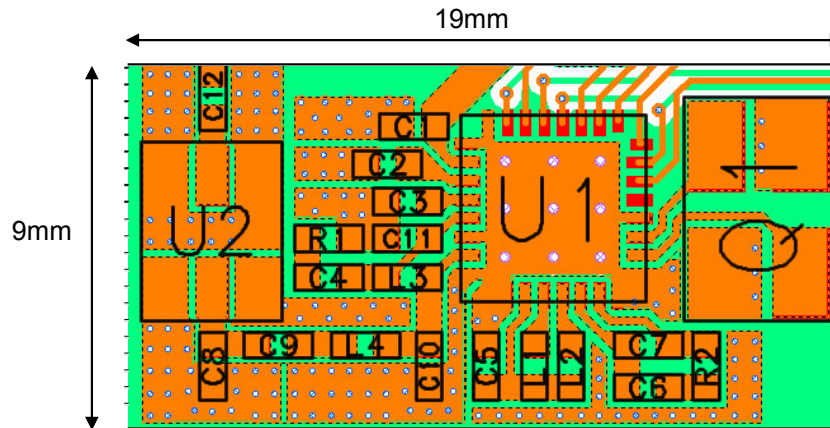


Figure 46: Reference Design Layout (top view)

7.5.3. Bill Of Material

Table 29: Reference Design BOM

Ref	Value		Tol (+/-)	Techno	Size	Comment
	868MHz	915MHz				
U1	SX1210		-	Transceiver IC	TQFN-32	-
Q1	12.8 MHz		15 ppm at 25°C 20 ppm over -40/+85°C 2ppm/year max	AT-cut	5.0*3.2 mm	Fundamental, Cload=15 pF
R2	6.8 kΩ		1%	-	0402	Loop filter
C1	1uF		15%	X5R	0402	VDD decoupling
C2	1uF		15%	X5R	0402	Top regulator decoupling
C3	220 nF		10%	X7R	0402	Digital regulator decoupling
C5	100 nF		10%	X7R	0402	VCO regulator decoupling
C6	10 nF		10%	X7R	0402	Loop Filter
C7	680 pF		5%	NPO	0402	Loop Filter
C9	22 pF		5%	NPO	0402	DC block and L4 adjust
C10	5.4nH		5%	Multilayer	0402	Matching
L1, L2	8.2 nH	6.8 nH	0.2 nH	Wire wound	0402	VCO tank inductors
U2	869 MHz	915 MHz	-	SAW Filter	3.8*3.8 mm	Optional
L4	0R		-	-	0402	-
R1	NC		-	-	0402	-
C4	NC		-	-	0402	-
C8	NC		-	-	0402	-
L3	NC		-	-	0402	-
C11	NC		-	-	0402	-
C12*	47pF		5%	NPO	0402	DC block

Note: for battery powered applications, a high value capacitance should be implemented in parallel with C1 (typically 10 μ F) to offer a low impedance voltage source during startup sequences.

7.5.4. Ordering Information for Tools

The modules described in section 7.5 can be ordered through your Semtech representative for evaluation purpose:

Table 30: Tools Ordering Information

Part Number	Description
SM1211E868	2 layer RF module, 868 MHz band (Transceiver is used to evaluate the receiver)
SM1211E915	2 layer RF module, 915 MHz band (Transceiver is used to evaluate the receiver)
SX1211SK868	Full evaluation kit, including 2 SM1211E868, controller boards, antennas and cables
SX1211SK915	Full evaluation kit, including 2 SM1211E915, controller boards, antennas and cables

7.6. Reference Design Performance

All the measurements visible on section 7.6 typical figures obtained under the following conditions, unless otherwise noted:

- Nominal VDD = 3.3 V
- Tests performed at room temperature: 25°C +/-3°C
- Center frequency 869 MHz or 915 MHz
- {R, P, S} triplets are those calculated by the software described in section 3.2.8.
- All register settings are default, except for those stated in the relevant sub-sections
- Maximum Output Power programmed on Pout tests
- All sensitivities are evaluated in Continuous mode, demodulating a PN15 sequence, BER=0.1%
- FSK sensitivities measured at 25kbps, Fdev=+/-50 kHz
- OOK sensitivities measured at 8kbps, with Fo=100 kHz. IF2 set to 100 kHz.
- On all Adjacent Channel Rejection (ACR), Blocking and Spurious Response Frequency tests, the unwanted signal is unmodulated.
- Bill of Materials as shown in section 7.5.3. In particular, a SAW filter is used (see its performance on section **Error! Reference source not found.**)
- The filter settings described on Table 31 and Table 32 were used for the measurements of section 7.6.5.

Table 31: FSK Rx Filters vs. Bit Rate

Bit Rate	Fdev	Filter Setting Addr 16	Fdev + BR/2	Rx 3 dB BW		Max. drift
				Programmed	Actual	
kbps	+/- kHz	Hex	kHz	kHz	kHz	+/- ppm
100	200	FF	250	400	306	62
66.67	133	E9	166.7	250	214	53
50	100	D6	125	175	158	37
40	80	B5	100	150	137	41
33.33	67	A4	83.3	125	116	36
28.57	57	A3	71.4	100	96	27
25	50	A3	62.5	100	96	37
22.22	44	72	55.6	75	69	15
20	40	72	50	75	69	21
18.18	36	72	45.5	75	69	26
16.67	33	72	41.7	75	69	30
15.38	33	41	41	50	47	7
14.29	33	41	40.5	50	47	7
12.5	33	41	39.6	50	47	8
10	33	41	38.3	50	47	10
5	33	41	35.8	50	47	12
2	33	41	34.3	50	47	14

Table 32: OOK Rx Filters vs. Bit Rate

Bit Rate	$F_0 + BR$	Filter Setting Addr 16	Rx 3 dB BW		Max. drift
			Programmed	Actual	
kbps	kHz	Hex	kHz	kHz	+/- ppm
16.67	117	C1	150	154	41
12.5	113	C1	150	154	46
9.52	110	A0	125	129	22
8	108	A0	125	129	23
4.76	105	A0	125	129	27
2.41	102	A0	125	129	30
1.56	102	A0	125	129	30

7.6.1. Sensitivity Flatness

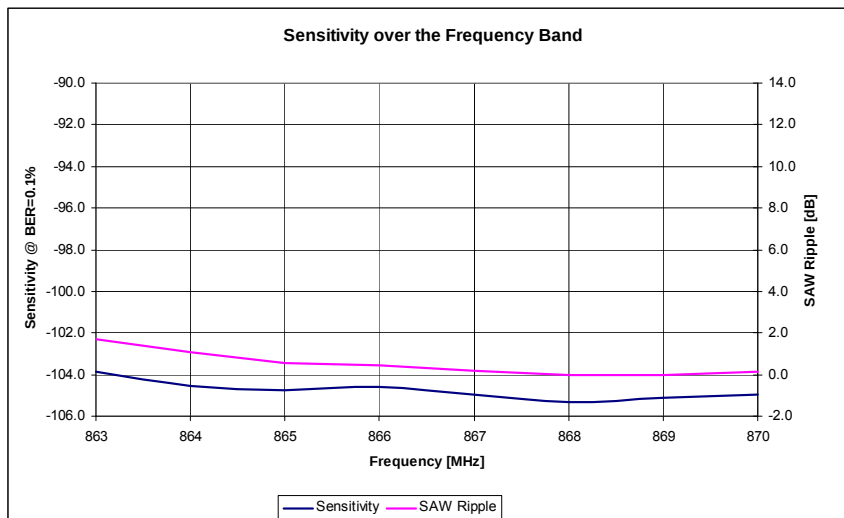


Figure 47: Sensitivity Across the 868 MHz Band

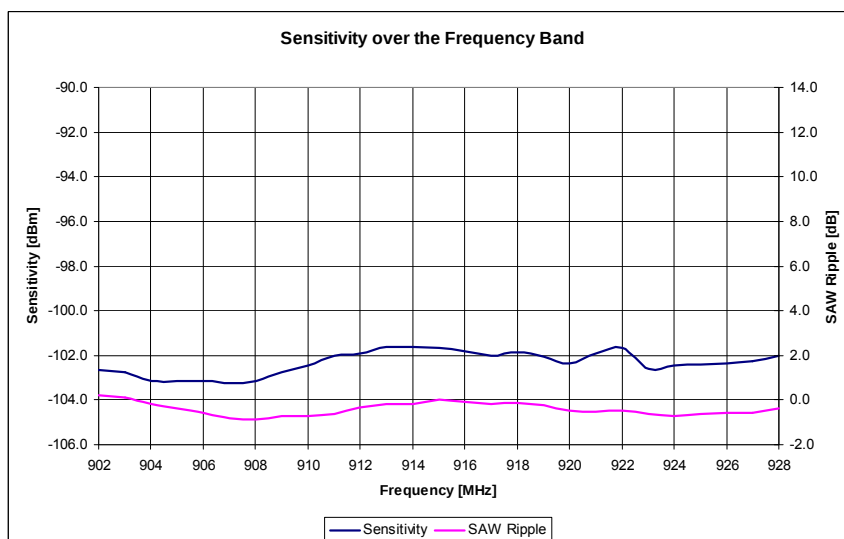


Figure 48: Sensitivity Across the 915 MHz Band

Notes:

- Measured in FSK mode only. OOK sensitivity characteristics will be similar.
- The sensitivity difference along the band remains inside the ripple performance of the SAW filter (the nominal passband of the 869 MHz SAW filter is 868 – 870 MHz)
- The SAW filter ripple response is referenced to its insertion loss at 869 MHz and 915 MHz for each filter.

7.6.2. Sensitivity vs. LO Drift

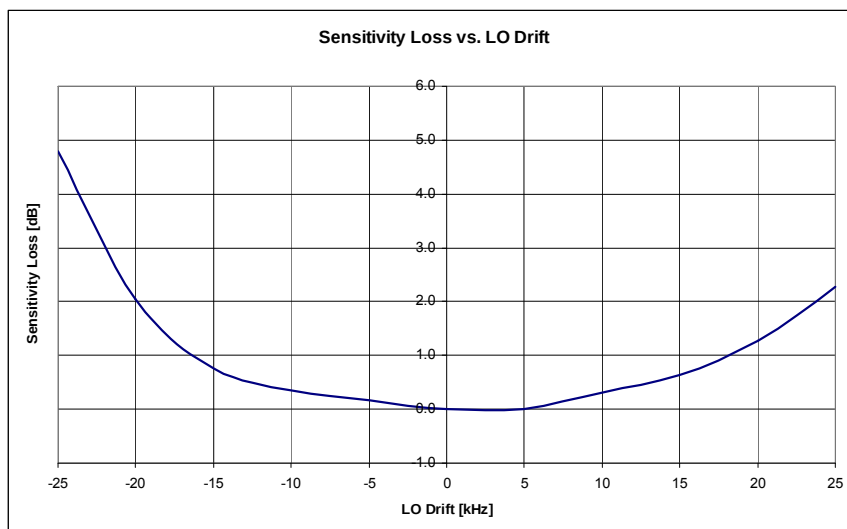


Figure 49: FSK Sensitivity Loss vs. LO Drift

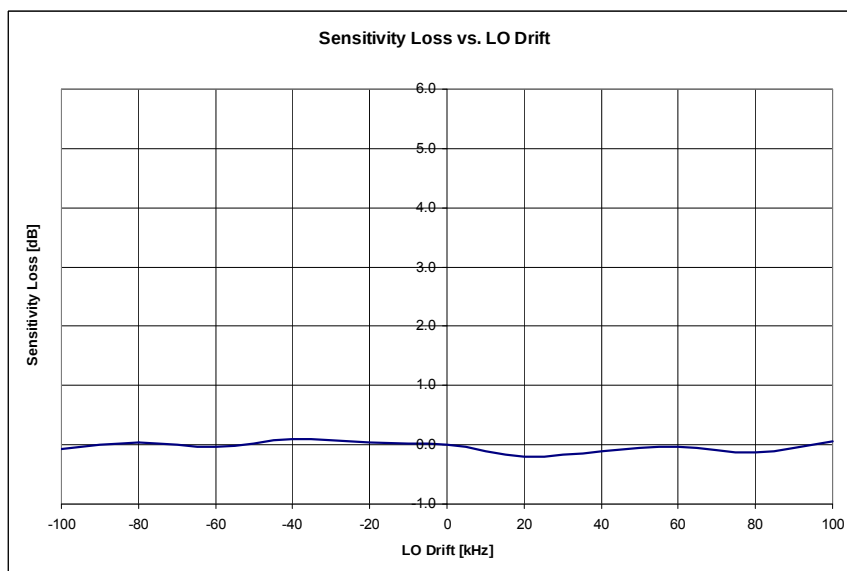


Figure 50: OOK Sensitivity Loss vs. LO Drift

Notes:

- In FSK Mode, the default filter setting ("A3" at address \$16) is kept, leading to $F_c = 96$ kHz typ.
- In OOK Mode, "F3" is set at address \$16, leading to $(F_c - F_o) = 95$ kHz typ.
- The above ensures that the channel filter is wide enough, therefore characterizing the demodulator response, and NOT the filter response.

7.6.3. Sensitivity vs. Receiver BW

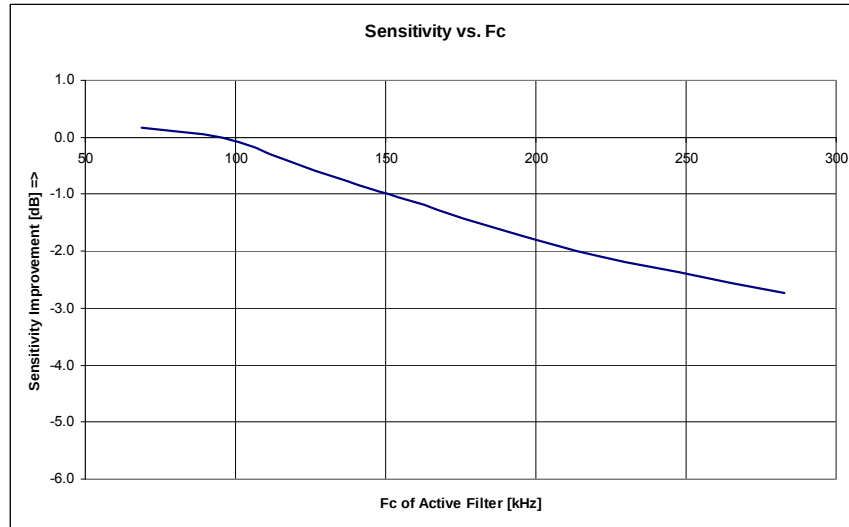


Figure 51: FSK Sensitivity vs. Rx BW

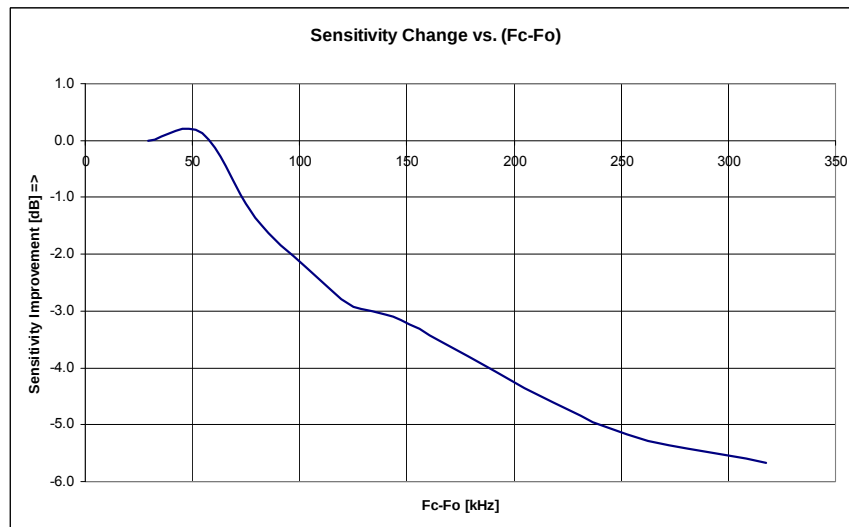


Figure 52: OOK Sensitivity Change vs. Rx BW

7.6.4. Sensitivity Stability over Temperature and Voltage

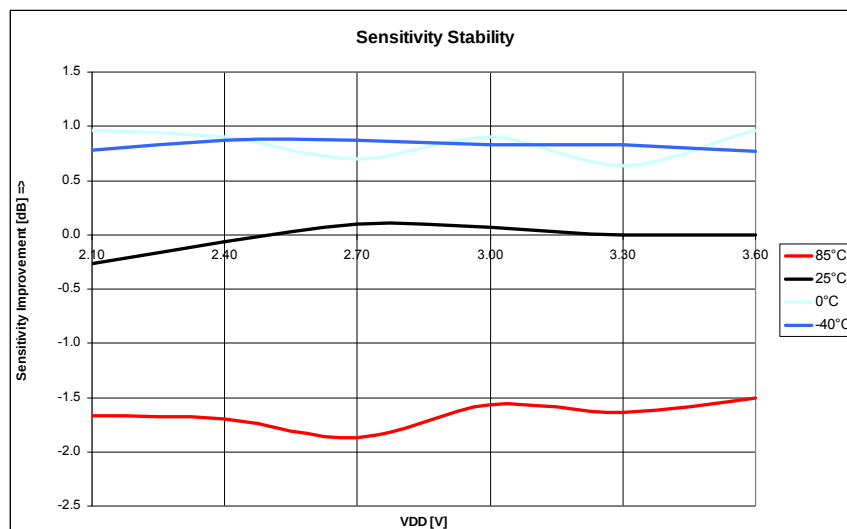


Figure 53: Sensitivity Stability

Note:

- The sensitivity performance is very stable over the VDD range, and the effect of high temperature is minimal.

7.6.5. Sensitivity vs. Bit Rate

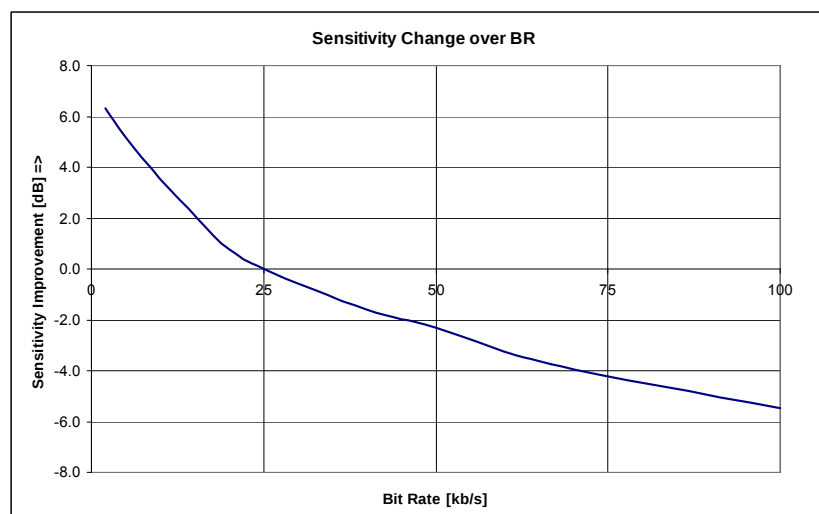


Figure 54: FSK Sensitivity vs. BR

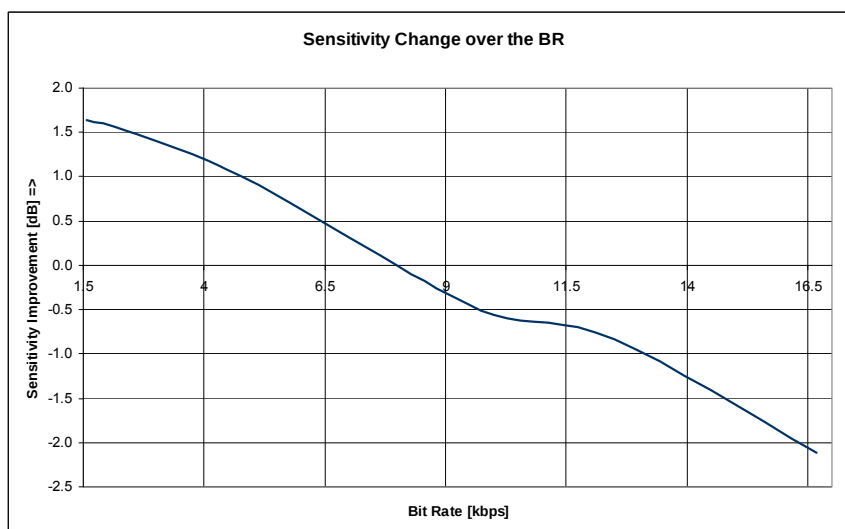


Figure 55: OOK Sensitivity vs. BR

7.6.6. Adjacent Channel Rejection

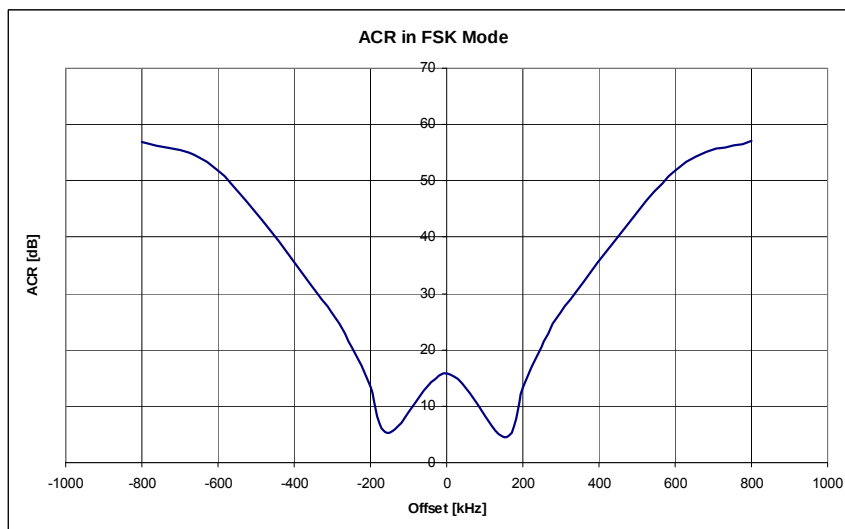


Figure 56: ACR in FSK Mode

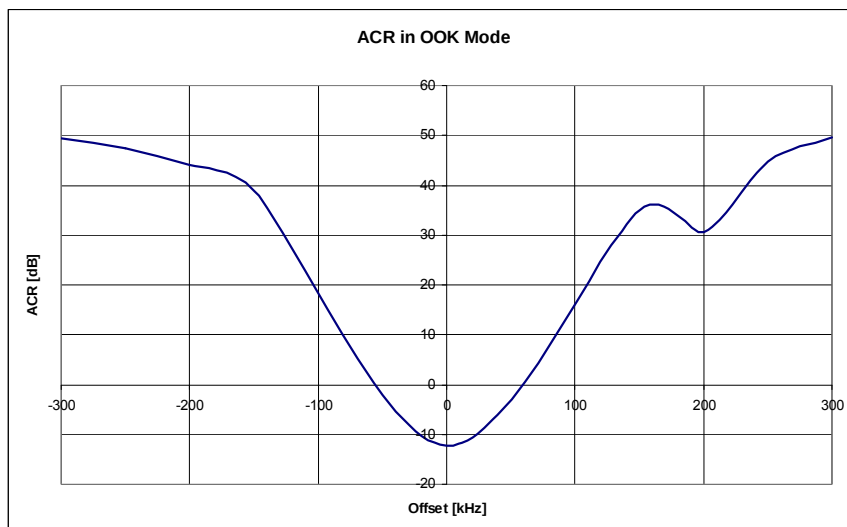


Figure 57: ACR in OOK Mode

Notes:

- In FSK mode, the unwanted signal is unmodulated (as described in the EN 300-220 V2.1.1). Co-Channel Rejection (CCR, Offset = 0kHz) is positive due to the DC cancellation process of the zero-IF architecture
- In OOK mode, the polyphase filter efficiency is limited, thus limiting the adjacent channel rejection at $2 \times F_o$ distance.

8. Packaging Information

8.1. Package Outline Drawing

SX1210 is available in a 32-lead TQFN package as shown in Figure 58 below.

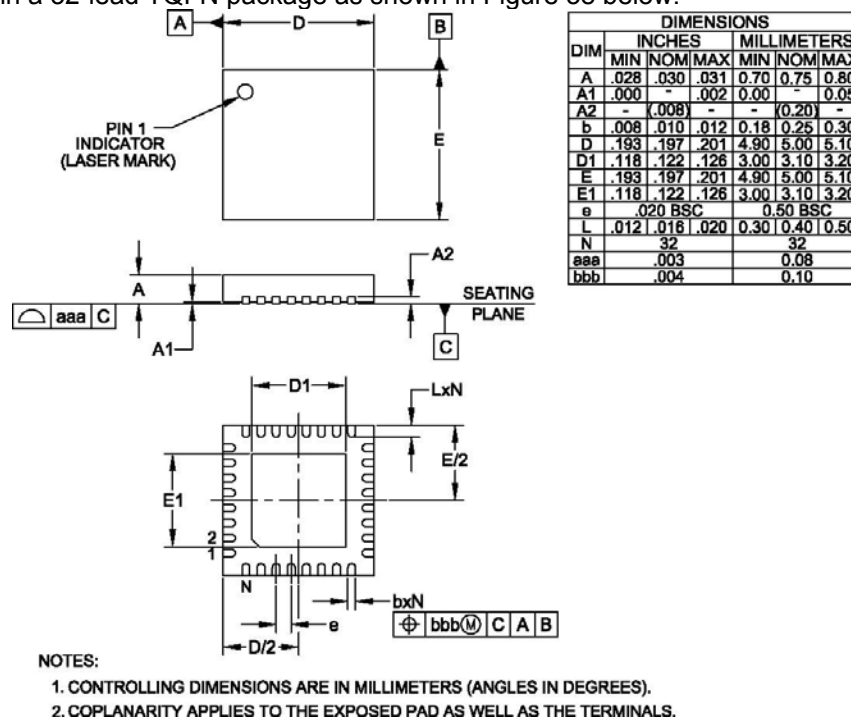


Figure 58: Package Outline Drawing

8.2. PCB Land Pattern

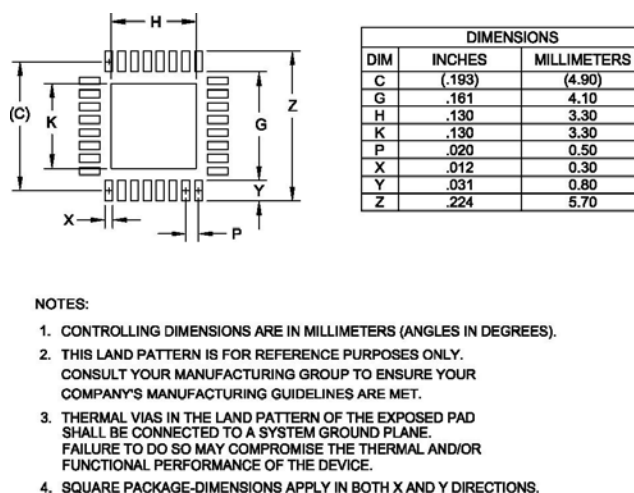
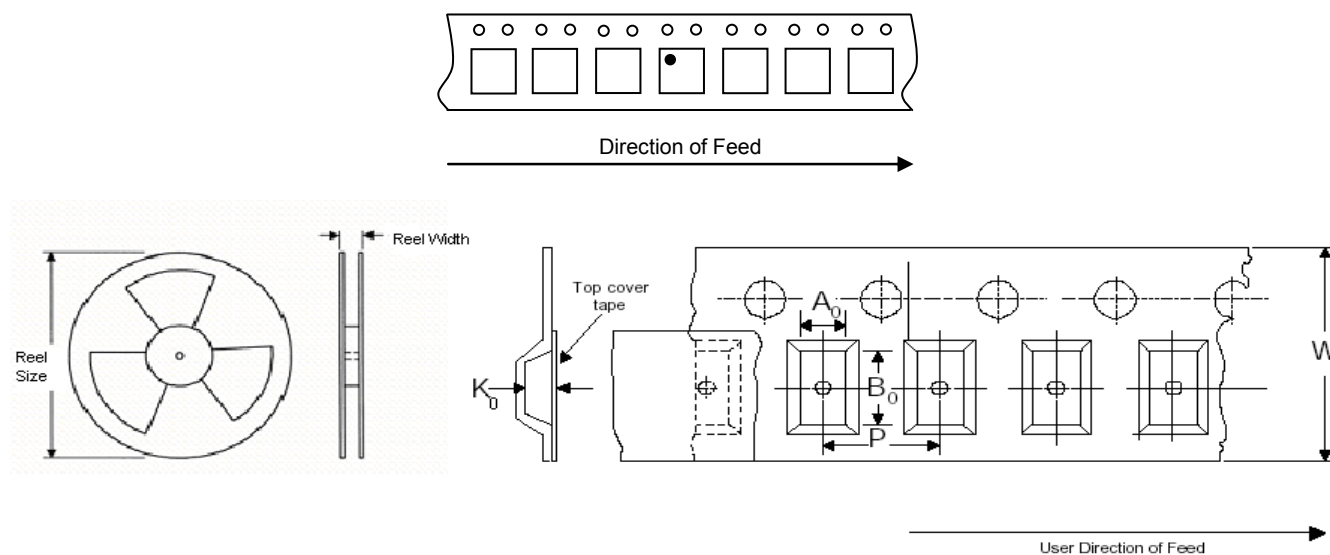


Figure 59: PCB Land Pattern

8.3. Tape & Reel Specification



Carrier Tape				Reel				
Tape Width(W)	Pocket Pitch (P)	Ao/Bo	Ko	Reel Size	Reel Width	Min.Trailer Length	Min. Leader Length	QTY per Reel
12 +/-0.3	8 +/-0.1	5.25 +/-0.2	1.10 +/-0.1	330.2	12.4	400	400	3000

Notes:

*all dimensions in mm

*single sprocket holes

Figure 60: Tape & Reel Dimensions

9. Revision History

▪

10. Contact Information

Semtech Corporation
Advanced Communication and Sensing Products Division
200 Flynn Road, Camarillo, CA 93012
Phone (805) 498-2111 Fax: (805) 498-3804

© Semtech 2008

All rights reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent or other industrial or intellectual property rights. Semtech. assumes no responsibility or liability whatsoever for any failure or unexpected operation resulting from misuse, neglect improper installation, repair or improper handling or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified range.

SEMTECH PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF SEMTECH PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE UNDERTAKEN SOLELY AT THE CUSTOMER'S OWN RISK. Should a customer purchase or use Semtech products for any such unauthorized application, the customer shall indemnify and hold Semtech and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs damages and attorney fees which could arise.