

9-BIT BUFFER

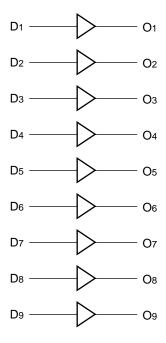
FEATURES

- Max. propagation delay of 700ps
- IEE min. of -55mA
- Extended supply voltage option: VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75k Ω input pull-down resistors
- 70% faster than Fairchild 300K at lower power
- Function and pinout compatible with Fairchild F100K
- Available in 28-pin PLCC package

DESCRIPTION

The SY100S322 is an ultra-fast buffer designed for use in high-performance ECL systems. The device provides nine non-inverting buffers with single-ended outputs. The inputs on the device have $75k\Omega$ pull-down resistors.

BLOCK DIAGRAM

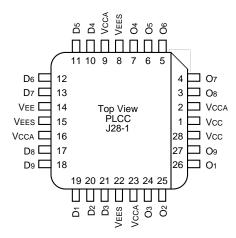


PIN NAMES

Pin	Function					
D1 – D9	Data Inputs					
O1 – O9	Data Outputs					
VEES	VEE Substrate					
VCCA	Vcco for ECL Outputs					

Micrel, Inc. SY100S322

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S322JC	J28-1	Commercial	SY100S322JC	Sn-Pb
SY100S322JCTR ⁽¹⁾	J28-1	Commercial	SY100S322JC	Sn-Pb
SY100S322JZ ⁽²⁾	J28-1	Commercial	SY100S322JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S322JZTR ^(1, 2)	J28-1	Commercial	SY100S322JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

- 1. Tape and Reel.
- 2. Pb-Free package is recommended for new designs.

LOGIC EQUATION

On = Dn, n = 1 to 9

DC ELECTRICAL CHARACTERISTICS

VEE = -4.2V to -5.5V unless otherwise specified, VCC = VCCA = GND

Symbol Parameter		Min.	Тур.	Max.	Unit	Condition
lih	Input HIGH Current	_	_	200	μΑ	VIN = VIH (Max.)
IEE	Power Supply Current	- 55	-41	-25	mA	Inputs Open

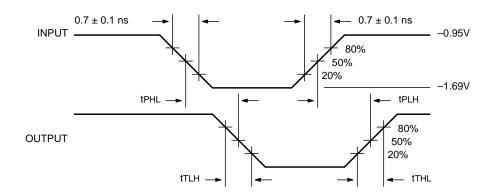
SY100S322

AC ELECTRICAL CHARACTERISTICS

VEE = -4.2V to -5.5V unless otherwise specified, VCC = VCCA = GND

		TA = 0°C		TA = +25°C		TA = +85°C			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Condition
tPLH tPHL	Propagation Delay Data to Output	300	700	300	700	300	700	ps	
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

TIMING DIAGRAM



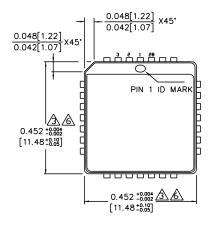
Propagation Delay and Transition Times

Note:

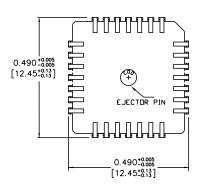
 \mbox{VEE} = $-4.2\mbox{V}$ to $-5.5\mbox{V}$ unless otherwise specified, \mbox{Vcc} = \mbox{Vcca} = \mbox{GND}

SY100S322 Micrel, Inc.

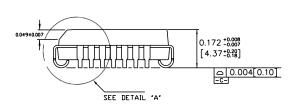
28-PIN PLCC (J28-1)



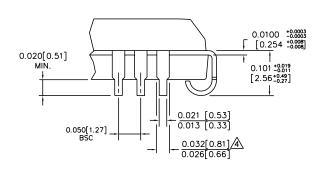
TOP VIEW



BOTTOM VIEW



SIDE VIEW



DETAIL "A"

NOTES:

DIMENSIONS ARE IN INCHES [MM].
CONTROLLING DIMENSION: INCHES.
DIMENSION DOES NOT INCLUDE MOLD FLASH
OR PROTRUSIONS, EITHER OF WHICH SHALL NOT
EXCEED 0.008 [0.203].
LEAD DIMENSION DOES NOT INCLUDE DAMBAR
PROTRUSION.

MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN

PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. A

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