



## SY88053CL

### 1.0625G to 12.5G Limiting Post Amplifier with Programmable Decision Threshold

Revision 1.0

## General Description

The SY88053CL limiting post amplifier is designed for use in fiber-optic receivers for multi-rate applications from 1.0625Gbps to 12.5Gbps.

The SY88053CL contains a high-bandwidth, high-sensitivity input stage with user-programmable, wide-range SD assert/LOS de-assert threshold levels, which enables optimized system reach. Typically, 4dB of electrical hysteresis is provided to minimize LOS or SD chattering caused by noisy input signals. A logic level control pin is provided to enable user selection of an open-collector, TTL-compatible LOS or SD status indication signal with an external 5k $\Omega$  to 10k $\Omega$  pull-up resistor.

The SY88053CL provides fast SD assert and LOS de-assert times over the entire differential input voltage range of 5mV<sub>PP</sub> to 1800mV<sub>PP</sub>.

The SY88053CL input stage also provides a user-adjustable decision threshold circuit to optimize BER in noisy applications such as WDM, where EDFA and Raman amplifiers contribute uneven noise levels. By applying an external control voltage, the decision threshold can typically be adjusted from 30% to 70% from the nominal 50% threshold when the circuit is disabled.

The SY88053CL provides integrated 50 $\Omega$  input and output impedances to optimize the high-speed signal paths and reduce component count. The post amplifier outputs have user-selectable polarity inversion control to simplify PCB layout. A TTL-compatible JAM input is provided to enable a SQUELCH function by feeding back the LOS or SD signal. The JAM input disables only the post amplifier output.

The SY88053CL operates from a single +3.3V power supply, over temperatures ranging from -40°C to +85°C.

Datasheets and support documentation are available on Micrel's web site at: [www.micrel.com](http://www.micrel.com).

## Features

- Multi-rate operation from 1.0625Gbps to 12.5Gbps
- Adjustable decision threshold level for offset compensation or BER optimization
- Wide differential input range (5mV<sub>PP</sub> to 1800mV<sub>PP</sub>)
- Wide SD de-assert or LOS assert threshold range
  - 3mV<sub>PP</sub> to 30mV<sub>PP</sub>
  - 4dB typical electrical hysteresis
- Fast SD assert and LOS de-assert times
  - 75ns typical; 120ns maximum
- Selectable LOS or SD status signal indicator
- Selectable RXOUT+/RXOUT- polarity inversion
- TTL-compatible JAM input with internal pull-up
- Low-noise CML data inputs with integrated 50 $\Omega$  termination impedance to internal reference V<sub>REF</sub>
- Low-noise CML data outputs with integrated 50 $\Omega$  termination impedance
  - 25ps typical rise/fall times
- Wide range power supply: 3.3V  $\pm$ 10%
- Industrial temperature range: -40°C to +85°C
- Available in a tiny 3mm x 3mm QFN package

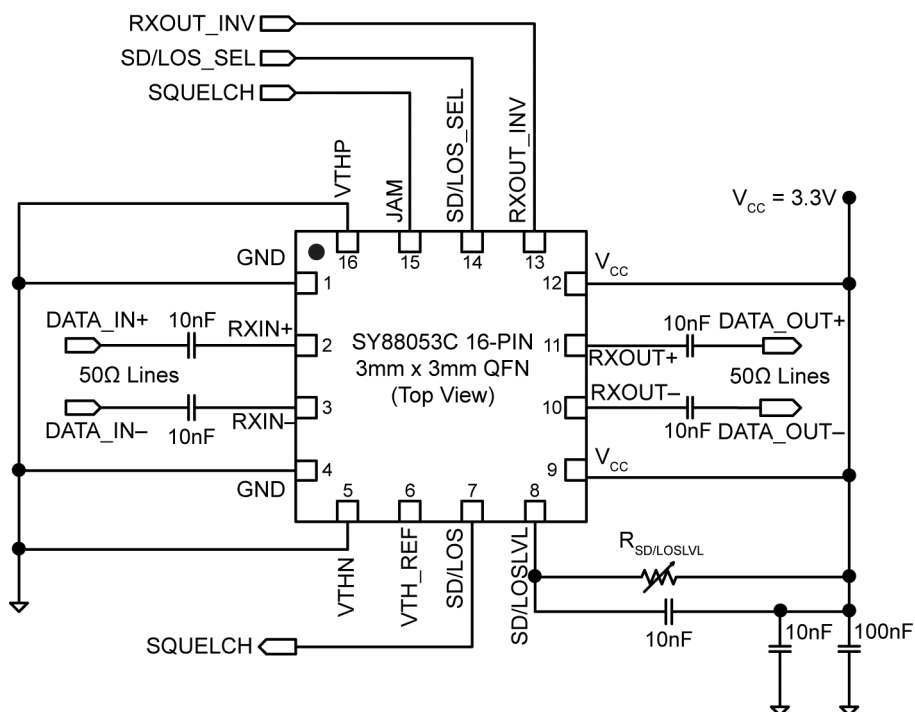
## Applications

- Asymmetrical/Symmetrical 10GEPON
- Asymmetrical/Symmetrical XGPON
- 10Gigabit Ethernet
- 8Gbps and 10Gbps Fibre Channel
- SONET OC192; SDH STM64
- WDM/DWDM systems

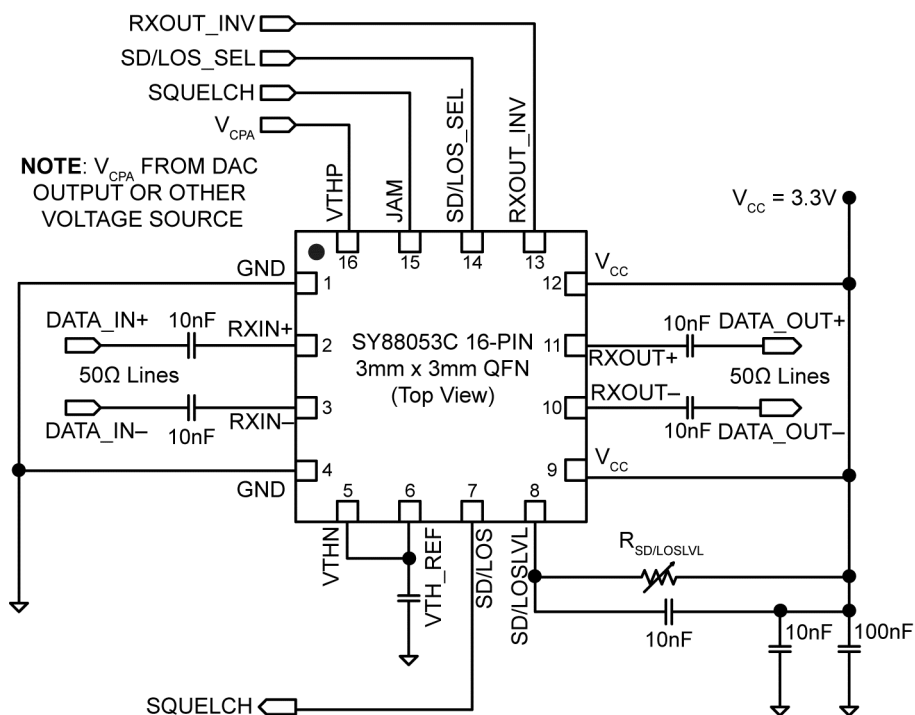
## Markets

- PON/FTTx
- Datacom/Enterprise
- Storage area networks
- High-performance computing
- Telecom
- 8G+ Optical transceivers

## Typical Application Circuit – Fixed Decision Threshold



## Typical Application Circuit – Adjustable Decision Threshold



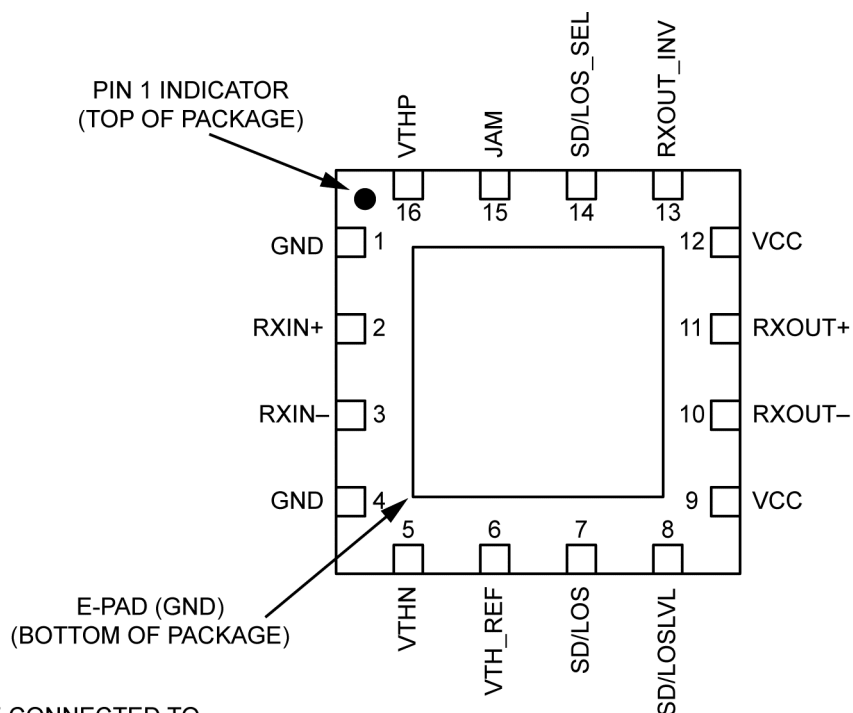
## Ordering Information

| Part Number                   | Package Type     | Operating Range | Package Marking                      | Lead Finish    |
|-------------------------------|------------------|-----------------|--------------------------------------|----------------|
| SY88053CLMG                   | 3mm x 3mm QFN-16 | Industrial      | 053C with Pb-Free bar line indicator | NiPdAu Pb-Free |
| SY88053CLMG TR <sup>(1)</sup> | 3mm x 3mm QFN-16 | Industrial      | 053C with Pb-Free bar line indicator | NiPdAu Pb-Free |

**Note:**

1. Tape and reel.

## Pin Configuration



**NOTE:**

E-PAD MUST BE CONNECTED TO THE PCB NEGATIVE POWER SUPPLY PLANE USING THE RECOMMENDED VIA ARRAY

**16-Pin 3mm x 3mm QFN  
(Top View)**

## Pin Description

| Pin # | Pin Name   | Pin Type                    | Functional Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------|------------|-----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1     | GND        | Negative Supply Rail        | Negative supply rail. Connect to the PCB negative power supply plane that is also connected to the ePAD.                                                                                                                                                                                                                                                                                                                                                                                        |
| 2     | RXIN+      | High-Speed Data Input       | Differential noninverting data input. LVPECL/CML compatible. AC-coupled with 100nF (high-frequency, low-ESR capacitor is recommended). Internally terminated with 50Ω to $V_{CC} - 1.2V$ . AC-coupled only.                                                                                                                                                                                                                                                                                     |
| 3     | RXIN-      | High-Speed Data Input       | Differential inverting data input. LVPECL/CML-compatible. AC-coupled with 100nF (high-frequency, low-ESR capacitor is recommended). Internally terminated by 50Ω to $V_{CC} - 1.2V$ . AC-coupled only.                                                                                                                                                                                                                                                                                          |
| 4     | GND        | Negative Supply Rail        | Negative supply rail. Connect to the PCB negative power supply plane that is also connected to the ePAD.                                                                                                                                                                                                                                                                                                                                                                                        |
| 5     | VTHN       | Analog Voltage Input        | Analog control input. Connect to VTH_REF for crossing threshold adjustment using VTHP (pin 16). Connect to GND to disable crossing point adjustment capability.                                                                                                                                                                                                                                                                                                                                 |
| 6     | VTH_REF    | Analog Current Output       | Reference voltage. 1.25V reference with respect to GND for crossing point decision threshold adjustment.                                                                                                                                                                                                                                                                                                                                                                                        |
| 7     | SD/LOS     | Open Collector Logic Output | Output status indicator. Loss of signal (LOS) or signal detect (SD) open collector output externally terminated with 5kΩ to 10kΩ resistor to $V_{CC}$ . TTL-compatible logic levels.<br><br>LOS = High when RXIN+/RXIN- amplitude falls below the threshold set at the SD/LOSLVL pin.<br><br>SD = Low when RXIN+/RXIN- amplitude falls below the threshold set at the SD/LOSLVL pin.                                                                                                            |
| 8     | SD/LOSLVL  | Analog Input                | Analog control input. Sets the trigger threshold for the LOS or SD status indicator signals.<br><br>If SD/LOS_SEL = High (LOS selected), connect a resistor from the SD/LOSLVL pin (loss of signal threshold level) to $V_{CC}$ to adjust the LOS_Assert threshold for the RXIN+/RXIN- data inputs.<br><br>If SD/LOS_SEL = Low (SD selected), connect a resistor from the SD/LOSLVL pin (signal select level) to $V_{CC}$ to adjust the SD_de-assert threshold for the RXIN+/RXIN- data inputs. |
| 9, 12 | $V_{CC}$   | Positive Supply Rail        | Positive power supply input. Bypass with a 0.1μF capacitor in parallel with a 0.01μF low-ESR capacitor to GND as close as possible to the $V_{CC}$ pin.                                                                                                                                                                                                                                                                                                                                         |
| 10    | RXOUT-     | High-Speed Data Output      | Differential inverting data output (default). CML-compatible and internally terminated by 50Ω to $V_{CC}$ . Can be AC or DC-coupled to downstream devices. Can be inverted using the RXOUT_INV control pin.                                                                                                                                                                                                                                                                                     |
| 11    | RXOUT+     | High-Speed Data Output      | Differential noninverting data output (default). CML-compatible and internally terminated by 50Ω to $V_{CC}$ . Can be AC or DC-coupled to downstream devices. Can be inverted using the RXOUT_INV control pin.                                                                                                                                                                                                                                                                                  |
| 13    | RXOUT_INV  | Logic Level Input           | Input control signal. TTL-compatible logic input signal to invert the polarity of the RXOUT+/- signals. Internal ~18kΩ pull-up to $V_{CC}$ .<br><br>Default = High (NC): Pin10 = RXOUT- and pin11 = RXOUT+<br>RXOUT_INV = Low: Pin10 = RXOUT+ and pin11 = RXOUT-.                                                                                                                                                                                                                               |
| 14    | SD/LOS_SEL | Logic Level Input           | Input control signal. TTL-compatible logic input signal to select LOS or SD as the output signal. Internal ~18kΩ pull-up to $V_{CC}$ .<br><br>Default = High (NC): LOS selected – normal operation<br>LOS/SD_SEL = Low: SD selected and JAM operation is inverted                                                                                                                                                                                                                               |

| Pin # | Pin Name | Pin Type             | Functional Description                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|----------|----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | JAM      | Logic Level Input    | Input control signal. TTL-compatible input signal that enables or disables the RXOUT+/- output signals. Internal 27k $\Omega$ pull-up resistor to V <sub>CC</sub> . Can be connected to SD/LOS to form a SQUELCH function.<br>When SD/LOS_SEL = High<br>Default = High and RXOUT+/- outputs are disabled.<br>Low = RXOUT+ and RXOUT- outputs are enabled<br>Operation is inverted when SD/LOS_SEL = Low and SD is selected.   |
| 16    | VTHP     | Analog Voltage Input | Analog control voltage input that typically adjusts the crossing point threshold from 30% to 70%.<br>Threshold crossing adjustment control. Apply a DC-control voltage from 0V to 2.4V to adjust the crossing point. VTHN (pin 6) must be connected to VTH_REF (pin 7). Nominal 50% midpoint decision threshold occurs with VTHP = 1.25V. Connect to ground to disable decision threshold (crossing point) adjust capability. |
| ePAD  | GND      | Negative Supply Rail | Exposed thermal pad. Must be soldered to PCB plane connected to the negative supply rail. The recommended via array is needed to remove heat from the device.                                                                                                                                                                                                                                                                 |

**Absolute Maximum Ratings<sup>(2)</sup>**

|                                   |                                    |
|-----------------------------------|------------------------------------|
| Supply Voltage ( $V_{CC}$ )       | 0V to +4.0V                        |
| Input Voltage (RXIN+, RXIN–)      | $V_{CC} - 1.5V$ to $V_{CC}$        |
| CML Output Voltage ( $V_{OUT}$ )  | $V_{CC} - 1.0V$ to $V_{CC} + 0.5V$ |
| $V_{VTH\_REF}$ Current            | –800 $\mu$ A to +500 $\mu$ A       |
| JAM Voltage                       | 0 to $V_{CC}$                      |
| SD/LOSLVL Voltage                 | $V_{CC} - 1.3V$ to $V_{CC}$        |
| Lead Temperature (soldering, 20s) | 260°C                              |
| Storage Temperature ( $T_s$ )     | –65°C to +150°C                    |

**Operating Ratings<sup>(3)</sup>**

|                                           |                  |
|-------------------------------------------|------------------|
| Supply Voltage ( $V_{CC}$ )               | +3.0V to +3.6V   |
| Ambient Temperature ( $T_A$ )             | –40°C to +85°C   |
| Junction Temperature ( $T_J$ )            | –40°C to +125°C  |
| Package Thermal Resistance <sup>(4)</sup> | 3mm x 3mm QFN-16 |
| ( $\theta_{JA}$ ) Still-air               | 60°C/W           |
| ( $\psi_{JB}$ )                           | 33°C/W           |

**DC Electrical Characteristics**

$V_{CC} = 3.0$  to  $3.6V$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ , typical values at  $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$ .

| Symbol         | Parameter                               | Condition                 | Min.             | Typ.             | Max.             | Units    |
|----------------|-----------------------------------------|---------------------------|------------------|------------------|------------------|----------|
| $I_{CC}$       | Power Supply Current                    | Note 5                    |                  | 58               | 75               | mA       |
| SD/LOSLVL      | SD or LOS Threshold Voltage             |                           | $V_{CC} - 1.3$   |                  | $V_{CC}$         | V        |
| $V_{OH}$       | RXOUT+/RXOUT–<br>High Voltage           |                           | $V_{CC} - 0.020$ | $V_{CC} - 0.005$ | $V_{CC}$         | V        |
| $V_{OL}$       | RXOUT+/RXOUT–<br>Low Voltage            |                           | $V_{CC} - 0.400$ | $V_{CC} - 0.350$ | $V_{CC} - 0.300$ | V        |
| $V_{OFFSET}$   | Differential Output Offset              | VTHP and VTHN tied to GND |                  |                  | $\pm 80$         | mV       |
| $V_{VTH\_REF}$ | Decision Threshold<br>Reference Voltage |                           |                  | 1.25             |                  | V        |
| $Z_0$          | Single-Ended Output<br>Impedance        |                           | 45               | 50               | 55               | $\Omega$ |
| $Z_I$          | Single-Ended Input<br>Impedance         |                           | 45               | 50               | 55               | $\Omega$ |

**Notes:**

- Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this datasheet. Exposure to absolute maximum ratings conditions may affect device reliability.
- The datasheet limits are not guaranteed if the device is operated beyond the recommended operating conditions.
- Package thermal resistance assumes that the exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB.  $\psi_{JB}$  and  $\theta_{JA}$  assumes still air and a 4-layer PCB, unless otherwise stated. It also assumes that the recommended via pattern and via sizes on the PCB are used.
- Outputs RXOUT+ and RXOUT– are loaded with external 50 $\Omega$  loads and the outputs are enabled.

## TTL DC Electrical Characteristics

$V_{CC} = 3.0$  to  $3.6V$ ;  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , typical values at  $V_{CC} = 3.3V$ ,  $T_A = 25^{\circ}C$ .

| Symbol              | Parameter                                     | Condition                                                                                            | Min. | Typ. | Max. | Units   |
|---------------------|-----------------------------------------------|------------------------------------------------------------------------------------------------------|------|------|------|---------|
| CPA <sub>LOW</sub>  | Output Signal Crossing Range Lower Limit      | V <sub>THN</sub> connected to V <sub>TH_REF</sub> and 0V to 2.4V applied to V <sub>THP</sub> .       | 30   | 40   |      | %       |
| CPA <sub>HIGH</sub> | Output signal Crossing Range Upper Limit      | $10 \leq V_{ID} \leq 60mV_{PP}$ , see <a href="#">"Crossing Point Adjustment Waveforms."</a> Note 6. |      | 60   | 70   | %       |
| V <sub>IH</sub>     | Input High Voltage                            | JAM, RXOUT_INV, SD/LOS_SEL                                                                           | 2.0  |      |      | V       |
| V <sub>IL</sub>     | Input Low Voltage                             | JAM, RXOUT_INV, SD/LOS_SEL                                                                           |      |      | 0.8  | V       |
| I <sub>IH</sub>     | JAM, RXOUT_INV, SD/LOS_SEL Input High Current | V <sub>IN</sub> = 2.7V                                                                               |      |      | 20   | $\mu A$ |
|                     |                                               | V <sub>IN</sub> = V <sub>CC</sub>                                                                    |      |      | 100  |         |
| I <sub>IL</sub>     | JAM, RXOUT_INV, SD/LOS_SEL Input Low Current  | V <sub>IN</sub> = 0.4V                                                                               | -0.3 |      |      | mA      |
| V <sub>OH</sub>     | SD or LOS Output High Level                   | Sourcing 100 $\mu A$                                                                                 | 2.4  |      |      | V       |
| V <sub>OL</sub>     | SD or LOS Output Low Level                    | Sinking 2mA                                                                                          |      |      | 0.4  | V       |

**Note:**

6. Crossing point adjust functionality is limited to small input amplitude swing levels, as noted. Crossing point adjust range is reduced outside of the noted input amplitude swing levels.

## AC Electrical Characteristics

$V_{CC} = 3.3V \pm 10\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ . Typical values at  $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$ ;  $R_{LOAD} = 50\Omega$  to  $V_{CC}$ .

| Symbol                                             | Parameter                                                      | Condition                          | Min.             | Typ.             | Max.             | Units            |
|----------------------------------------------------|----------------------------------------------------------------|------------------------------------|------------------|------------------|------------------|------------------|
| $V_{OH}$                                           | RXOUT+, RXOUT– High Voltage                                    |                                    | $V_{CC} - 0.020$ | $V_{CC} - 0.005$ | $V_{CC}$         | V                |
| $V_{OL}$                                           | RXOUT+, RXOUT– Low Voltage                                     |                                    | $V_{CC} - 0.400$ | $V_{CC} - 0.350$ | $V_{CC} - 0.300$ | V                |
| $t_r, t_f$                                         | Output Rise/Fall Time<br>(20% to 80%)                          | Note 7                             |                  | 25               | 40               | ps               |
| $t_{JITTER}$                                       | Deterministic                                                  | Note 8                             |                  | 10               |                  | ps               |
|                                                    | Random                                                         | Note 9                             |                  | 1                |                  |                  |
| $V_{ID\_11.3G}$                                    | Differential Input Voltage Swing                               | Note 10. See Figure 1.             | 5                |                  | 1800             | mV <sub>PP</sub> |
| $V_{ID\_12.5G}$                                    | Differential Input Voltage Swing                               | Note 11. See Figure 1.             | 10               |                  | 1800             | mV <sub>PP</sub> |
| $V_{OD}$                                           | Differential Output Voltage Swing                              | Note 7                             | 600              | 700              | 800              | mV <sub>PP</sub> |
| $t_{LOS\_D}; t_{LOS\_A}$<br>$t_{SD\_D}; t_{SD\_A}$ | LOS De-assert, LOS Assert Time<br>SD De-assert, SD Assert Time | Note 12                            |                  | 75               | 120              | ns               |
| $LOS_{AL\_20k}$                                    | Low LOS Assert Level                                           | $R_{LOSLVL} = 20k\Omega$ , Note 13 |                  | 3                |                  | mV <sub>PP</sub> |
| $LOS_{DL\_20k}$                                    | Low LOS De-assert Level                                        | $R_{LOSLVL} = 20k\Omega$ , Note 13 |                  | 5                |                  | mV <sub>PP</sub> |
| $HYS_{L\_20k}$                                     | Low LOS Hysteresis                                             | $R_{LOSLVL} = 20k\Omega$ , Note 14 | 2                | 4.4              | 6                | dB               |
| $LOS_{AM\_10k}$                                    | Medium LOS Assert Level                                        | $R_{LOSLVL} = 10k\Omega$ , Note 13 |                  | 4.5              |                  | mV <sub>PP</sub> |
| $LOS_{DM\_10k}$                                    | Medium LOS De-assert Level                                     | $R_{LOSLVL} = 10k\Omega$ , Note 13 |                  | 7.3              |                  | mV <sub>PP</sub> |
| $HYS_{M\_10k}$                                     | Medium LOS Hysteresis                                          | $R_{LOSLVL} = 10k\Omega$ , Note 14 | 2                | 4.1              | 6                | dB               |
| $LOS_{AH1\_1k}$                                    | High1 LOS Assert Level                                         | $R_{LOSLVL} = 1k\Omega$ , Note 13  |                  | 18.6             |                  | mV <sub>PP</sub> |
| $LOS_{DH1\_1k}$                                    | High1 LOS De-assert Level                                      | $R_{LOSLVL} = 1k\Omega$ , Note 13  |                  | 28.3             |                  | mV <sub>PP</sub> |
| $HYS_{H1\_1k}$                                     | High1 LOS Hysteresis                                           | $R_{LOSLVL} = 1k\Omega$ , Note 14  | 2                | 3.6              | 6                | dB               |
| $LOS_{AH2\_100}$                                   | High2 LOS Assert Level                                         | $R_{LOSLVL} = 100\Omega$ , Note 13 |                  | 29.7             |                  | mV <sub>PP</sub> |
| $LOS_{DH2\_100}$                                   | High2 LOS De-assert Level                                      | $R_{LOSLVL} = 100\Omega$ , Note 13 |                  | 44.6             |                  | mV <sub>PP</sub> |
| $HYS_{H2\_100}$                                    | High2 LOS Hysteresis                                           | $R_{LOSLVL} = 100\Omega$ , Note 14 | 2                | 3.5              | 6                | dB               |
| $A_{V(Diff)\_053C}$                                | Differential Voltage Gain                                      |                                    |                  | 44               |                  | dB               |
| $S_{21\_053C}$                                     | Single-Ended Small-Signal Gain                                 |                                    | 32               | 38               |                  | dB               |

### Note:

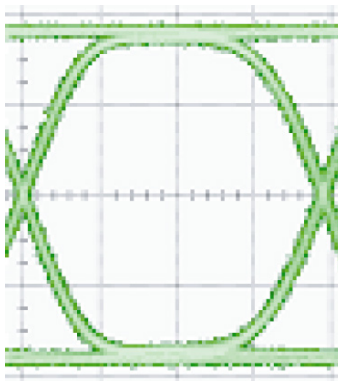
- Amplifier is in limiting mode. Input is a 200MHz square wave.
- Deterministic jitter is measured using 10Gbps K28.5 pattern,  $V_{ID} = 20mV_{PP}$ .
- Random jitter is measured using 10Gbps K28.7 pattern,  $V_{ID} = 20mV_{PP}$ .
- Differential input swing amplitude for data rates up to 11.3Gbps.
- Differential input swing amplitude for data rates between 11.3Gbps and 12.5Gbps.
- In real world applications, the LOS de-assert/assert time can be strongly influenced by the RC time constant of the AC-coupling capacitor and the 50 $\Omega$  input termination. To keep this time low, use a decoupling capacitor with the lowest value that is allowed by the data rate and the number of consecutive identical bits in the application (typical values are in the range of 0.001 $\mu F$  to 0.1 $\mu F$ ).
- See "Typical Operating Characteristics" for a graph showing how to choose a particular  $R_{LOSLVL}$  for a particular LOS assert and its associated de-assert amplitude.
- This specification defines electrical hysteresis as 20log (LOS de-assert/LOS assert). The ratio between optical hysteresis and electrical hysteresis is found to vary between 1.5 and 2, depending on the level of received optical power and ROSA characteristics.



## Crossing Point Adjustment Waveforms

### Waveform 1: Nominal Crossing Point Adjustment (50% Decision Threshold) – 20mV<sub>PP</sub> Signal Input

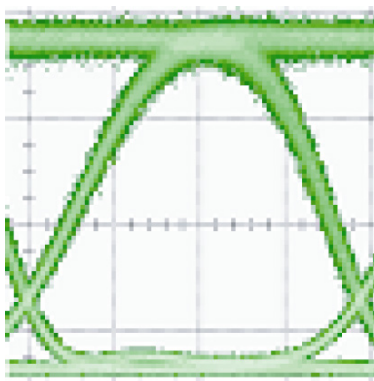
(V<sub>THN</sub> is tied to V<sub>TH\_REF</sub>; V<sub>THP</sub> = 1.25V)



### Waveform 2: Minimum Crossing Point Adjustment (~30% Decision Threshold) – 20mV<sub>PP</sub> Signal Input

V<sub>THN</sub> is tied to V<sub>TH\_REF</sub>; V<sub>THP</sub> is approximately 0.75V

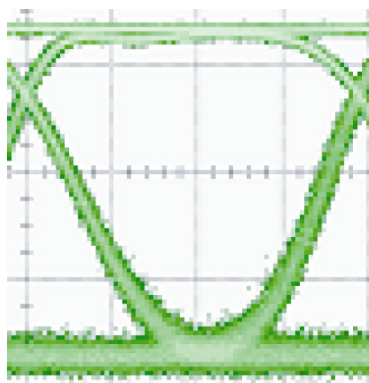
**Note:** Although the crossing point adjustment circuit has sufficient range to move the decision point threshold to 20%, it is recommended that the minimum adjustment be limited to ~30%.



### Waveform 3: Minimum Crossing Point Adjustment (~70% Decision Threshold) – 20mV<sub>PP</sub> Signal Input

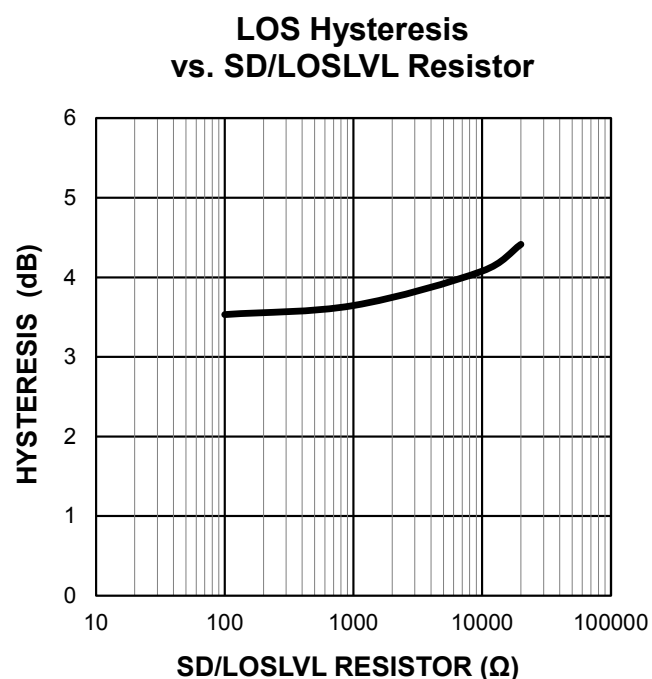
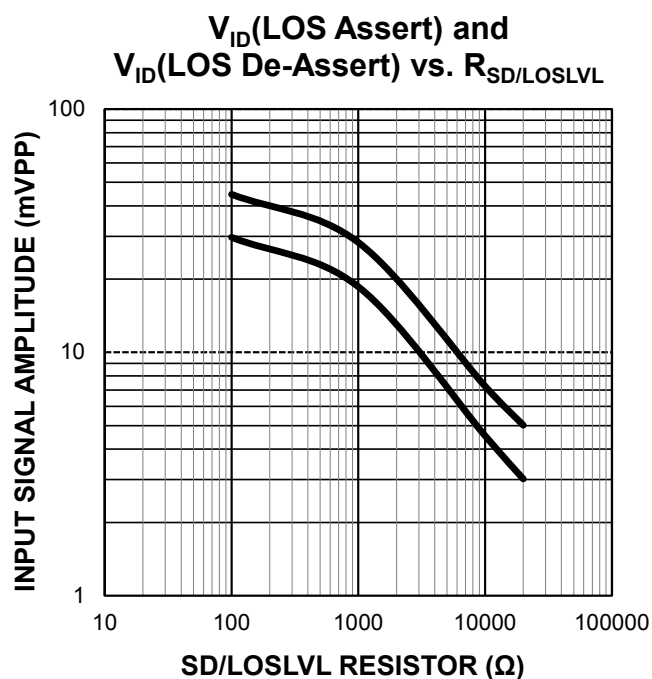
V<sub>THN</sub> is tied to V<sub>TH\_REF</sub>; V<sub>THP</sub> is approximately 1.75V

**Note:** Although the crossing point adjustment circuit has sufficient range to move the decision point threshold to 80%, it is recommended that the maximum adjustment be limited to ~70%.

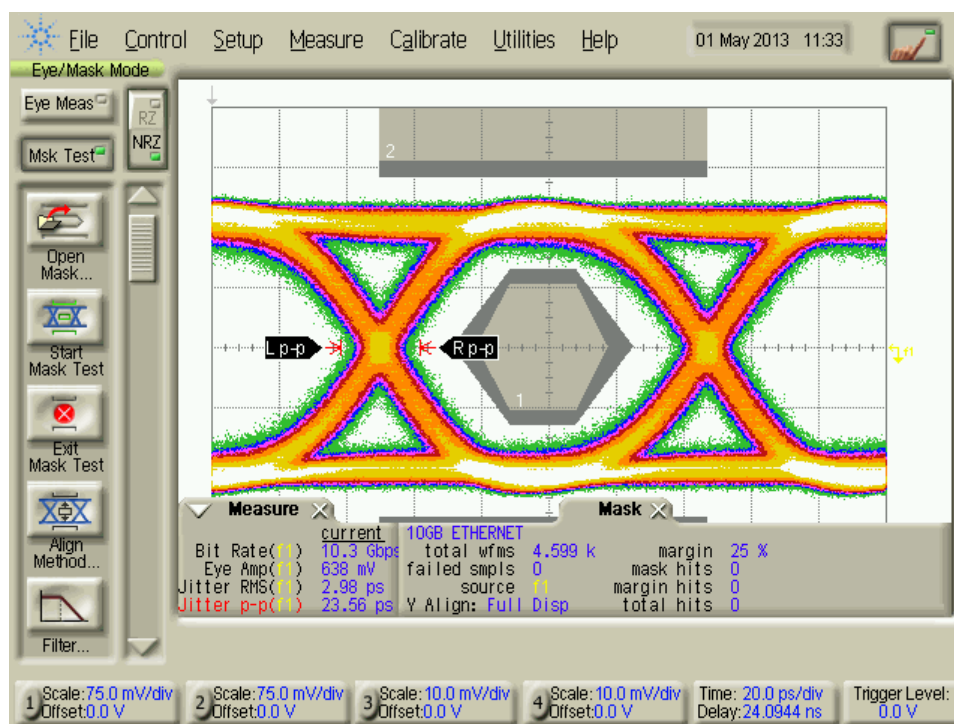


## Typical Operating Characteristics

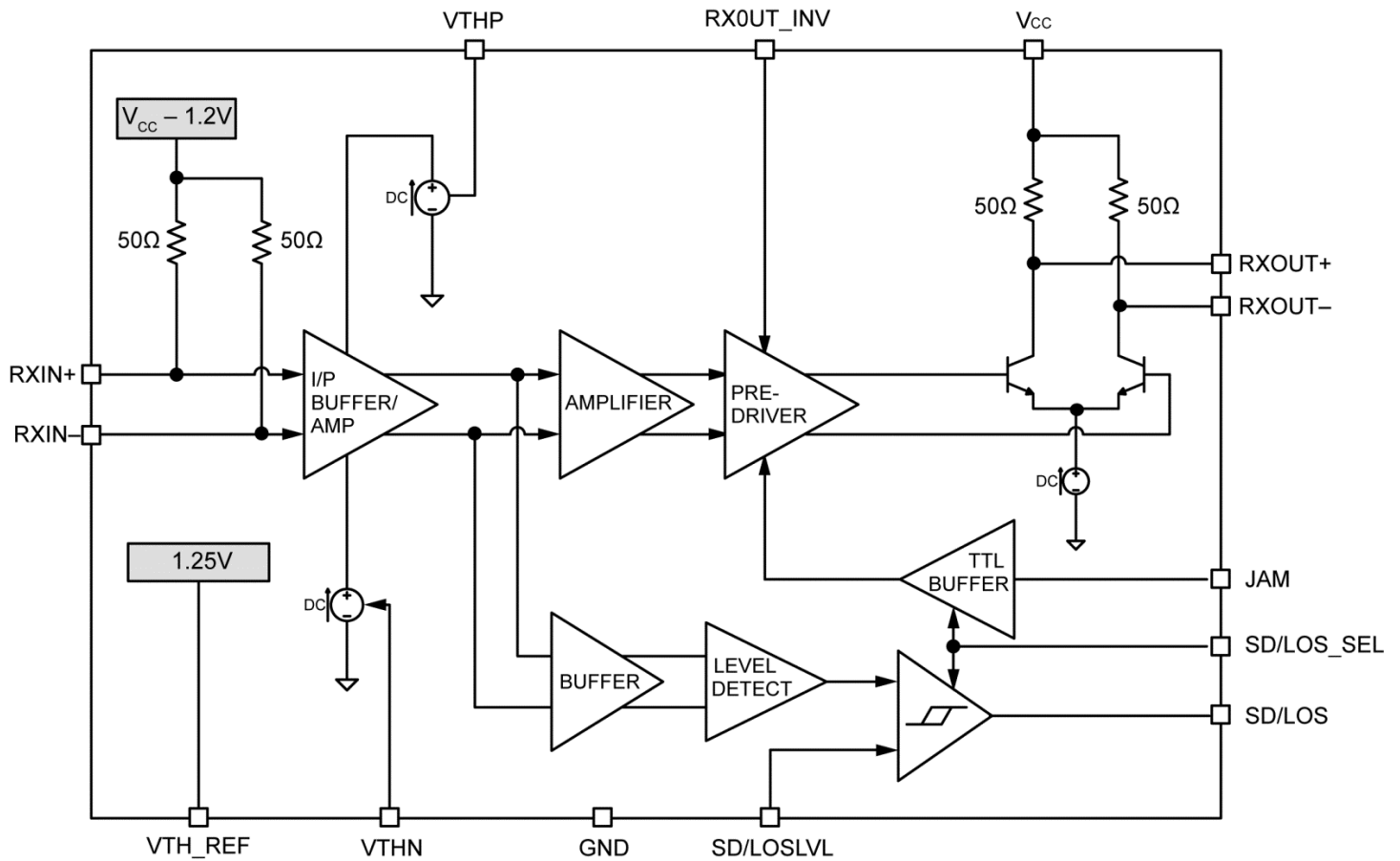
$V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$ ,  $R_{LOAD} = 50\Omega$  to  $V_{CC}$ , unless otherwise stated.



Typical Linear Mode 10.3G Output with 5mV<sub>PP</sub> Differential Input Signal



### Functional Block Diagram



## Functional Description

The SY88053CL is a high-sensitivity, high-bandwidth limiting post amplifier. It operates from a single +3.3V power supply across the entire industrial temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

Signals with data rates from 1.0625Gbps to 12.5Gbps and amplitudes as small as  $5\text{mV}_{\text{pp}}$  are supported. Figure 1 shows the allowed input voltage swing.

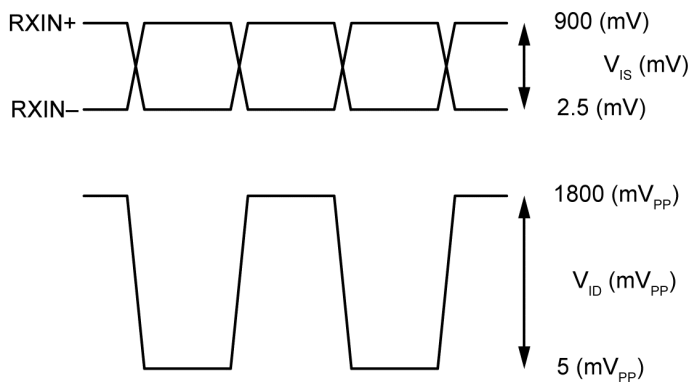


Figure 1.  $V_{\text{IS}}$  and  $V_{\text{ID}}$  Definition

The SY88053CL has a selectable SD or LOS status output signal that can be fed back to the JAM input to perform the SQUELCH function for output stability if there is no signal at the input. SD/LOSLVL sets the sensitivity of the input amplitude detection.

In applications where the noise is not evenly distributed between the high and the low levels of the signal, such as links using EDFA amplifiers, the zero crossing point (decision threshold) of the signal can be adjusted, using the VTHN and VTHP pins to optimize the performance of the link.

### Input Amplifier/Buffer

Figure 2 shows a simplified schematic of the input stage. The high sensitivity of the input amplifier allows signals as small as  $5\text{mV}_{\text{pp}}$  to be detected and amplified. The input amplifier allows input signals as large as  $1800\text{mV}_{\text{pp}}$ . Input signals are amplified with a typical 44dB differential voltage gain. The user will need to select the appropriate AC coupling capacitor value for their application.

### Output Buffer

The SY88053CL CML output buffer is designed to drive  $50\Omega$  impedance transmission lines and is internally terminated with  $50\Omega$  to  $V_{\text{CC}}$ . Figure 3 shows a simplified schematic of the output stage. The user will need to select the appropriate AC coupling capacitor value for their application.

## Signal Detect / Loss of Signal

The SY88053CL generates a user-selectable (SD/LOS\_SEL pin) signal detect (SD) or loss of signal (LOS) open-collector TTL output, as shown in Figure 4. LOS is used to determine whether the input amplitude is too small to be considered as a valid input. LOS asserts high if the input amplitude falls below the threshold set by SD/LOSLVL and de-asserts low otherwise. LOS can be fed back to the JAM input to perform the SQUELCH function and to maintain output stability under a LOS condition. JAM de-asserts the true output signal low without removing the input signals. Typically, 4dB LOS hysteresis is provided to prevent chattering.

When SD/LOSLVL is used to select the SD output on the SD/LOS pin, SD is asserted when the differential input signal amplitude exceeds the level set by the SD/LOSLVL resistor. The JAM operation is inverted when SD is selected.

### Signal Detect / Loss of Signal Level Setting

A programmable SD/LOS level set pin (SD/LOSLVL) sets the threshold of the input amplitude detection. Connecting an external resistor between  $V_{\text{CC}}$  and SD/LOSLVL sets the threshold voltage. This voltage ranges from  $V_{\text{CC}}$  to  $V_{\text{CC}} - 1.3\text{V}$ . The external resistor creates a voltage divider between  $V_{\text{CC}}$  and  $V_{\text{CC}} - 1.3\text{V}$ , as shown in Figure 5.

### Hysteresis

The SY88053CL provides typically 4dB LOS electrical hysteresis, which is defined as  $20\log(V_{\text{IN\_LOS\_De-Assert}} \div V_{\text{IN\_LOS\_Assert}})$ . Because the relationship of the voltage output of the ROSA to optical power at its input is linear, the optical hysteresis is typically half of the electrical hysteresis reported in the datasheet. In practice the ratio between electrical and optical hysteresis is found to be between 1.5 and 1.8. Thus, 4dB electrical hysteresis corresponds to an optical hysteresis within the range of 2dB to 2.4dB.

### Signal Crossing Point Adjustment

To optimize the decision threshold level, and so the BER of the optical link where the noise is unevenly distributed between the high and the low levels, the SY88053CL provides two pins for output signal crossing point adjustment (decision threshold) control.

The output signal crossing can be adjusted by connecting VTHN (pin 5) to VTH\_REF (pin 6), and applying a DC signal at VTHP (pin 16). By varying the DC signal at VTHP from 0V to 2.5V while the input signal to the post amplifier is less than  $60\text{mV}_{\text{pp}}$ , the crossing point of the output signal changes from approximately 30% to 70%, reaching 50% when  $V_{\text{THP}} = V_{\text{TH\_REF}} = 1.25\text{V}$ . If the crossing point control function is not needed, VTHN and VTHP must be connected to GND.

## Functional Circuit Structure

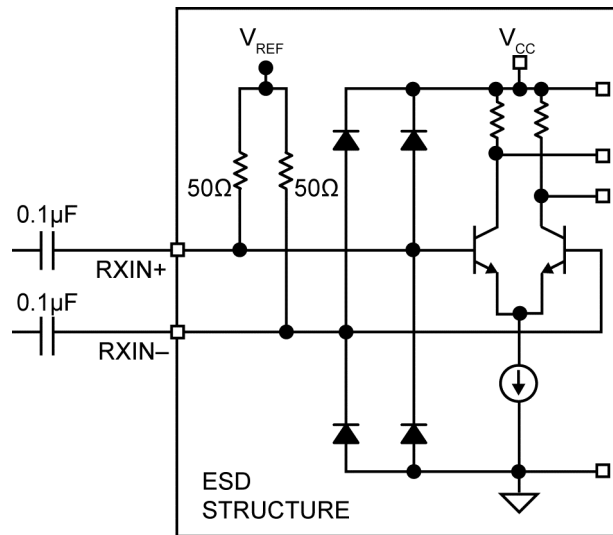


Figure 2. Typical Input Structure

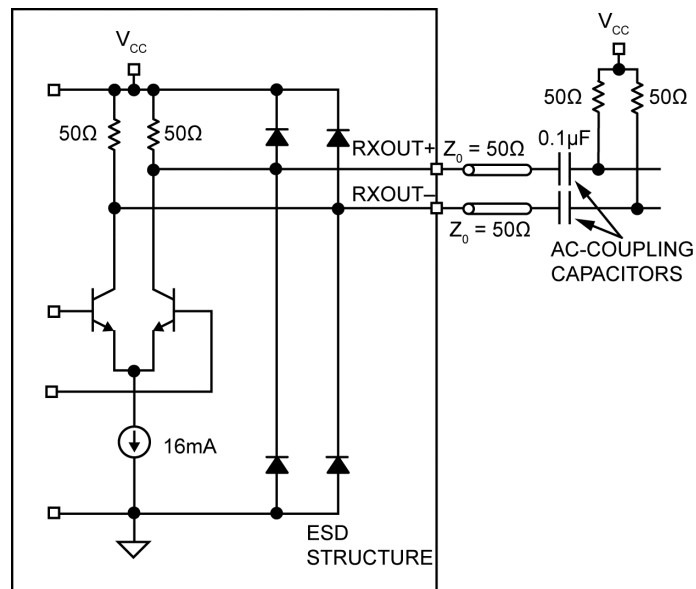


Figure 3. Typical Output Structure

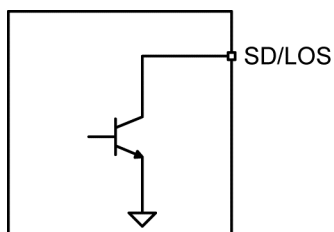


Figure 4. Typical SD/LOS Output Structure

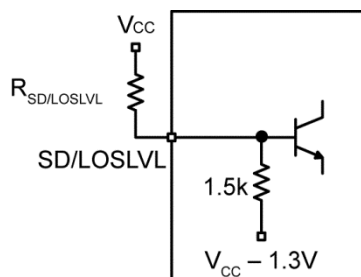
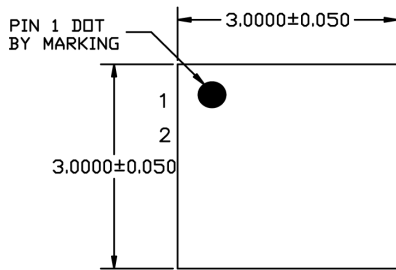


Figure 5. Typical SD/LOSLVL Setting Circuit

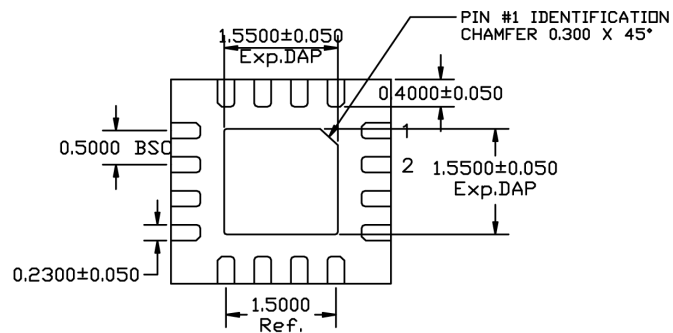
## Related Product and Support Documentation

| Document Number | Title                                                         | Application Note Link                                                                                        |
|-----------------|---------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------|
| AN-45           | Notes on Sensitivity and Hysteresis in Micrel Post Amplifiers | <a href="http://www.micrel.com/_PDF/HBW/App-Notes/an-45.pdf">www.micrel.com/_PDF/HBW/App-Notes/an-45.pdf</a> |

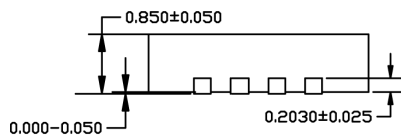
## Package Information<sup>(15)</sup>



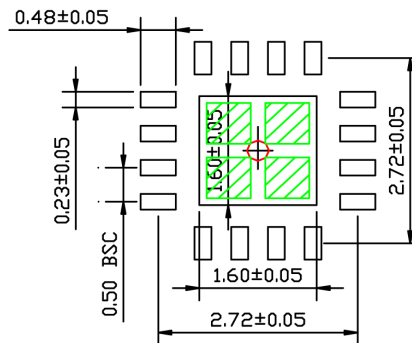
**TOP VIEW**  
NOTE: 1, 2, 3



**BOTTOM VIEW**  
NOTE: 1, 2, 3



**SIDE VIEW**  
NOTE: 1, 2, 3



**RECOMMENDED LAND PATTERN**  
NOTE: 4, 5

- NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
  2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
  3. PIN #1 IS ON TOP WILL BE LASER MARKED
  4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.3MM IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
  5. GREEN RECTANGLES (SHADED AREA) INDICATE SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.60x0.60 MM IN SIZE, 0.20 MM SPACING.

### 16-Pin (3mm x 3mm) QFN-16

#### Note:

15. Package information is correct as of the publication date. For updates and most current information, go to [www.micrel.com](http://www.micrel.com).

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