SY88305BL

3.3V, 3.2Gbps CML Limiting Post Amplifier with Wide Signal-Detect Range

General Description

The SY88305BL low-power limiting post amplifiers are designed for use in fiber-optic receivers. These devices connect to typical transimpedance amplifiers (TIAs). The linear signal output from TIAs can contain significant amounts of noise and may vary in amplitude over time. The SY88305BL quantizes these signals and output CML-level waveforms.

The SY88305BL operates from a single +3.3V power supply, over temperatures ranging from –40°C to +85°C. With their wide bandwidth and high gain, signals with data rates up to 3.2Gbps, and as small as $10mV_{PP}$, can be amplified to drive devices with CML/PECL inputs.

The device generates a Signal Detect (SD) open-collector TTL output. The SD function is optimized to detect a larger and wider input range, as shown in the characteristic curve on Page 6. A programmable signal-detect level set pin (SD_{LVL}) sets the sensitivity of the input amplitude detection.

SD asserts high if the input amplitude rises above the threshold sets by SD_{LVL} and de-asserts low otherwise. The SD output can be fed back to the EN input to maintain stability. Typically, 3.5dB LOS/SD hysteresis is provided to prevent chattering.

Datasheet and support documentation can be found on Micrel's web site at: www.micrel.com.

Features

- Signal Detect circuit optimized to detect a wide input range
- Chatter-free Open-Collector TTL Signal-Detect (SD)
- Single 3.3V power supply
- 155Mbps to 3.2Gbps operation
- Low-noise CML data outputs
- Programmable SD level set (SD_{LVL})
- Available in a tiny 10-pin EPAD-MSOP and 16-pin QFN package

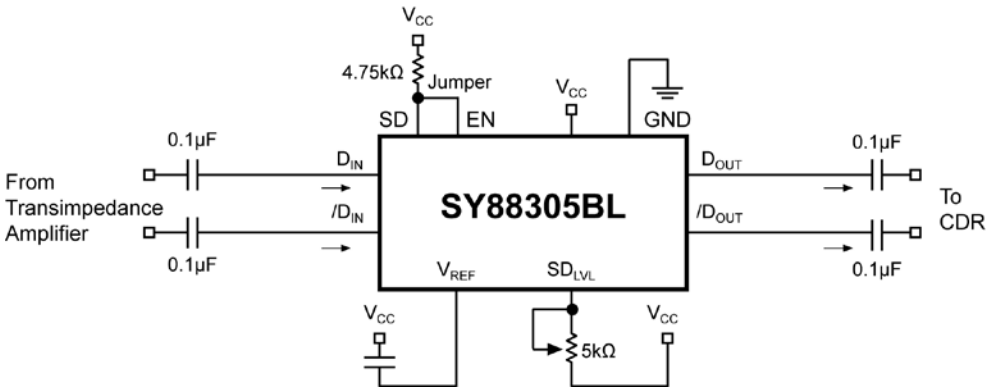
Applications

- PON
- Gigabit Ethernet
- 1X and 2X Fibre Channel
- SONET/SDH: OC-3/12/24/48 – STM 1/4/8/16
- High-gain line driver and line receiver

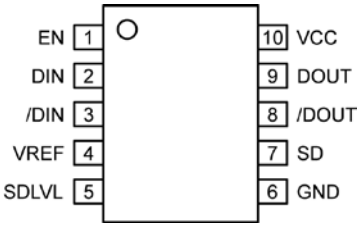
Markets

- FTTX
- Optical transceivers
- Datacom/Telecom
- Low-gain TIA interface
- Long-reach FOM

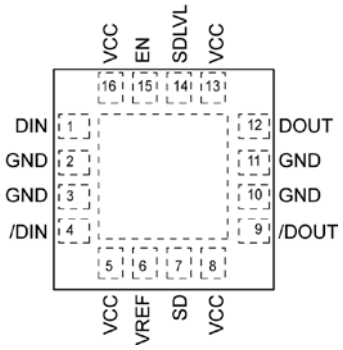
Typical Application



Pin Configuration



10-Pin EPAD-MSOP (K10-2)



16-Pin QFN

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY88305BLEY	K10-2	Industrial	305B with Pb-Free bar line indicator	Matte-Sn Pb-free
SY88305BLEYTR(1)	K10-2	Industrial	305B with Pb-Free bar line indicator	Matte-Sn Pb-free
SY88305BLMG	QFN-16	Industrial	305B with Pb-Free bar line indicator	NiPdAu Pb-free
SY88305BLMGTR(1)	QFN-16	Industrial	305B with Pb-Free bar line indicator	NiPdAu Pb-free

Note:

1. Tape and Reel.

hbwhelp@micrel.com or (408) 955-1690

Pin Description

Pin Number (MSOP)	Pin Number (QFN)	Pin Name	Type	Pin Function
1	15	EN	TTL Input: Default is high.	Enable: De-asserts true data output when LOW.
2	1	DIN	Data Input	True data input with 50Ω termination to V_{REF}.
3	4	/DIN	Data Input	Complementary data input with 50Ω termination to V_{REF}.
4	6	VREF		Reference Voltage: Placing a capacitor here to V_{CC} helps stabilize SD_{LVL}.
5	14	SDLVL	Input	Signal-detect Level Set: A resistor from this pin to V_{CC} sets the threshold for the data input amplitude at which the SD output will be asserted.
6 Exposed Pad	2, 3, 10, 11 Exposed Pad	GND	Ground	Device ground. Exposed pad must be connected to PCB ground plane.
7	7	SD	Open Collector TTL Output	Signal-detect: Asserts high when the data input amplitude rises above the threshold sets by SD_{LVL}. For proper operation, install an external 4.75kΩ pull-up resistor at this output.
8	9	/DOUT	CML Output	Complementary data output.
9	12	DOUT	CML Output	True data output.
10	5, 8, 13, 16	VCC	Power supply	Positive power supply.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... 0V to +4.0V
Input Voltage (DIN, /DIN) ..... 0 to V_{CC}
Output Current (I_{OUT})
  Continuous ..... ±50mA
  Surge ..... ±100mA
/EN Voltage ..... 0 to V_{CC}
V_{REF} Current ..... -800µA to +500µA
 Voltage ..... V_{REF} to V_{CC}
Lead Temperature (soldering, 20sec.) ..... 260°C
Storage Temperature (T_s) ..... -65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{CC}) ..... +3.0V to +3.6V
Ambient Temperature (T_A) ..... –40°C to +85°C
Junction Temperature (T_J) ..... –40°C to +125°C
Junction Thermal Resistance[3]
  EPAD-MSOP
    θ_{JA} (Still-Air) ..... 38°C/W
    ψ_{JB} ..... 22°C/W
  QFN
    θ_{JA} (Still-Air) ..... 61°C/W
    ψ_{JB} ..... 38°C/W

DC Electrical Characteristics

V_{CC} = 3.0V to 3.6V; R_L = 50Ω to V_{CC}; T_A = –40°C to +85°C; typical values at V_{CC} = 3.3V, T_A = 25°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{CC}	Power Supply Current	No output load		38	60	mA
V_{SDLVL}	SD_{LVL} Voltage		V_{REF}		V_{CC}	V
V_{OH}	CML Output HIGH Voltage		V_{CC}-0.020	V_{CC}-0.005	V_{CC}	V
V_{OL}	CML Output LOW Voltage		V_{CC}-0.475	V_{CC}-0.4	V_{CC}-0.350	V
V_{OFFSET}	Differential Output Offset				±80	mV
V_{REF}	Reference Voltage		V_{CC}-1.48	V_{CC}-1.32	V_{CC}-1.16	V
Z_I	Single-Ended Input Impedance		40	50	60	Ω

TTL DC Electrical Characteristics

V_{CC} = 3.0V to 3.6V; T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	EN Input HIGH Voltage		2.0			V
V_{IL}	EN Input LOW Voltage				0.8	V
I_{IH}	EN Input HIGH Current	V_{IN} = 2.7V V_{IN} = V_{CC}			20 100	µA µA
I_{IL}	EN Input LOW Current	V_{IN} = 0.5V	-300			µA
I_{OH}	SD Output Leakage	V_{OH} = 3.6V			100	µA
V_{OL}	SD Output LOW Level	I_{OL} = +4mA			0.5	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Thermal performance assumes the use of a 4-layer PCB. Exposed pad must be soldered (or equivalent) to the device's most negative potential on the PCB.

AC Electrical Characteristics

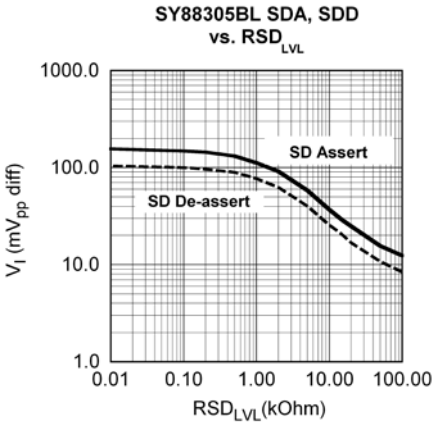
V_{CC} = 3.0V to 3.6V; R_L = 50Ω to V_{CC}; T_A = –40°C to +85°C; typical values at V_{CC} = 3.3V, T_A = +25°C.

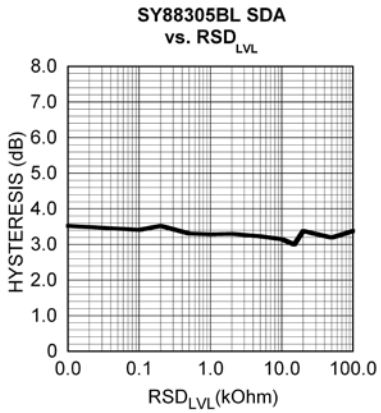
Symbol	Parameter	Condition	Min	Typ	Max	Units
t_r, t_f	Output Rise/Fall Time (20% to 80%)	Note 4		60	120	ps
t_{JITTER}	Deterministic Random	Note 5 Note 6		15 5		ps_{PP} ps_{RMS}
V_{ID}	Differential Input Voltage Swing	Figure 1	10		1800	mV_{PP}
V_{OD}	Differential Output Voltage Swing	$V_{ID} \geq 12mV_{PP}$, Figure 1	700	800	950	mV_{PP}
T_{OFF}	SD Assert Time			2	10	µs
T_{ON}	SD De-assert Time			2	10	µs
SD_{AL}	Low SD Assert Level	R_{SDLVL} = 15kΩ, Note 8		27		mV_{PP}
SD_{DL}	Low SD De-assert Level	R_{SDLVL} = 15kΩ, Note 8		18		mV_{PP}
HYS_L	Low SD/LOS Hysteresis	R_{SDLVL} = 15kΩ, Note 7		3.4		dB
SD_{AM}	Medium SD Assert Level	R_{SDLVL} = 5kΩ, Note 8		53	80	mV_{PP}
SD_{DM}	Medium SD De-assert Level	R_{SDLVL} = 5kΩ, Note 8	21	36		mV_{PP}
HYS_M	Medium SD/LOS Hysteresis	R_{SDLVL} = 5kΩ, Note 7	2	3.5	6	dB
SD_{AH}	High SD Assert Level	R_{SDLVL} = 100Ω, Note 8		137	200	mV_{PP}
SD_{DH}	High SD De-assert Level	R_{SDLVL} = 100Ω, Note 8	70	94		mV_{PP}
HYS_H	High SD/LOS Hysteresis	R_{SDLVL} = 100Ω, Note 7	2	3.5	6	dB
B_{-3dB}	3dB Bandwidth			2		GHz
$A_{V(Diff)}$	Differential Voltage Gain			39		dB
S_{21}	Single-ended Small-Signal Gain		26	33		dB

Notes:

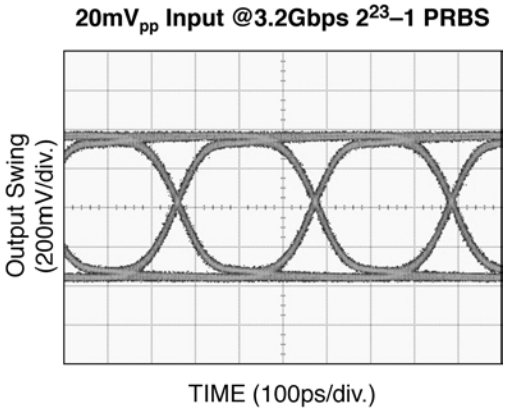
4. Amplifier in limiting mode. Input is a 200MHz, 100mVpp square wave.
5. Deterministic jitter measured using 3.2Gbps K28.5 pattern, $V_{ID} = 10mV_{PP}$.
6. Random jitter measured using 3.2Gbps K28.7 pattern, $V_{ID} = 10mV_{PP}$.
7. This specification defines electrical hysteresis as 20log (LOS De-assert/LOS Assert). The ratio between optical hysteresis and electrical hysteresis is found to vary between 1.5 and 2, depending upon the level of received optical power and ROSA characteristics. Based upon that ratio, the optical hysteresis corresponding to the electrical hysteresis range 2dB-6dB, shown in the AC characteristics table, will be 1dB-3dB Optical Hysteresis.
8. See “Typical Operating Characteristics” for a graph showing how to choose a particular R for a particular LOS assert and its associated de-assert amplitude.

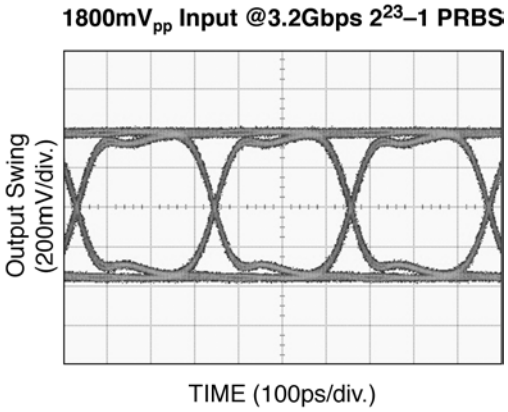
Typical Operating Characteristics



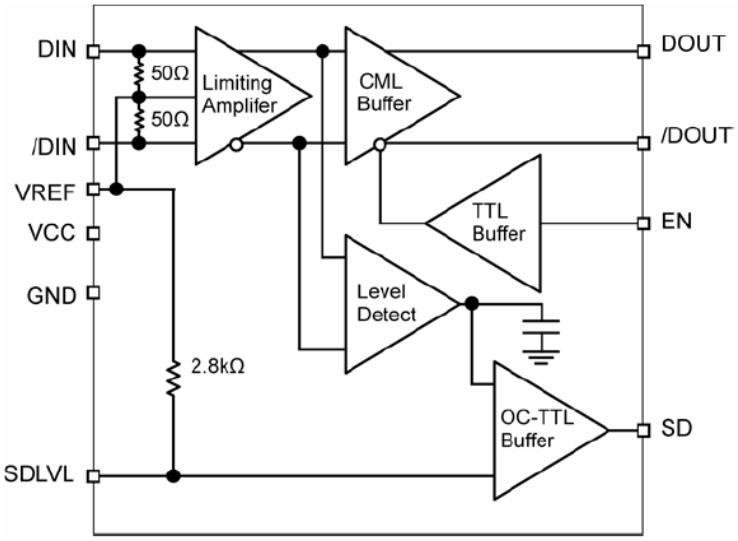


Functional Characteristics





Functional Block Diagram



Detailed Description

The SY88305BL low-power limiting post amplifiers operate from a single +3.3V power supply, over temperatures from –40°C to +85°C. Signals with data rates up to 3.2Gbps and as small as $10mV_{PP}$ can be amplified. Figure 1 shows the allowed input voltage swing. The SY88305BL generates an SD output allowing feedback to EN for output stability. SD_{LVL} sets the sensitivity of the input amplitude detection.

Input Amplifier/Buffer

Figure 2 shows a simplified schematic of the input stage. The high-sensitivity of the input amplifier allows signals as small as $10mV_{PP}$ to be amplified. The input amplifier also allows input signals as large as $1800mV_{PP}$. Input signals below 12mVpp are linearly amplified with a typical 42dB differential voltage gain. Since it is a limiting amplifier, these devices output typically $800mV_{PP}$ voltage-limited waveforms for input signals greater than $12mV_{PP}$. Applications requiring the SY88305BL to operate with strong signals should have the upstream TIA placed as close as possible to the devices' input pins. This ensures the best performance of the device.

Output Buffer

The SY88305BL CML output buffers are designed to drive 50Ω lines. The output buffer requires appropriate termination for proper operation. An external 50Ω resistor to V_{CC} for each output pin provides this. Figure 3 shows a simplified schematic of the output stage.

Signal Detect

The SY88305BL generates a chatter-free SD open-collector TTL output, as shown in Figure 4. SD asserts high if the input amplitude rises above the threshold sets by SD_{LVL} and de-asserts low otherwise. The SD output can be fed back to the EN input to maintain stability

Signal-Detect Level Set

Programmable SD level set pin (SD_{LVL}) sets the threshold of the input amplitude detection. Connecting an external resistor between V_{CC} and SD_{LVL} set the voltage at SD_{LVL}. This voltage ranges from V_{CC} to V_{REF}. The external resistor creates a voltage divider between V_{CC} and V_{REF}, as shown in Figure 5.

Hysteresis

The SY88305BL typically provides 3.5dB SD electrical hysteresis. By definition, a power ratio measured in dB is 10log (power ratio). Power is calculated as V^2_{IN}/R for an electrical signal. Hence, the same ratio can be stated as 20log (voltage ratio). While in linear mode, the electrical voltage input changes linearly with the optical power and therefore, the ratios change linearly. Thus, the optical hysteresis in dB is half the electrical hysteresis in dB given in the datasheet. Since the SY88305BL are electrical devices, this data sheet refers to hysteresis in electrical terms. With 3.5dB SD hysteresis, a voltage factor of 1.5 is required to assert or de-assert SD.

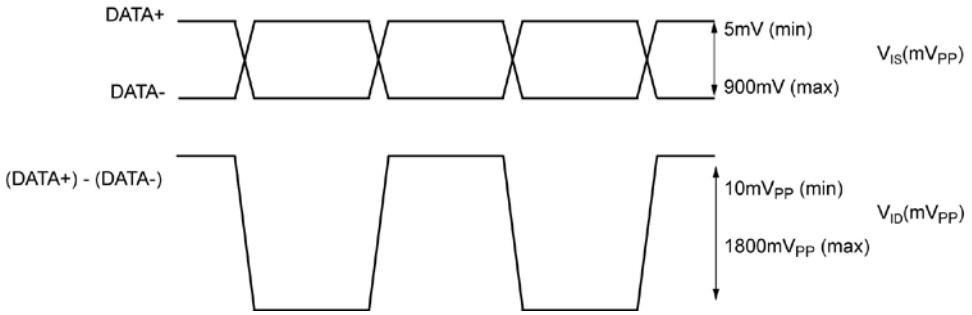


Figure 1. V_{IS} and V_{ID}

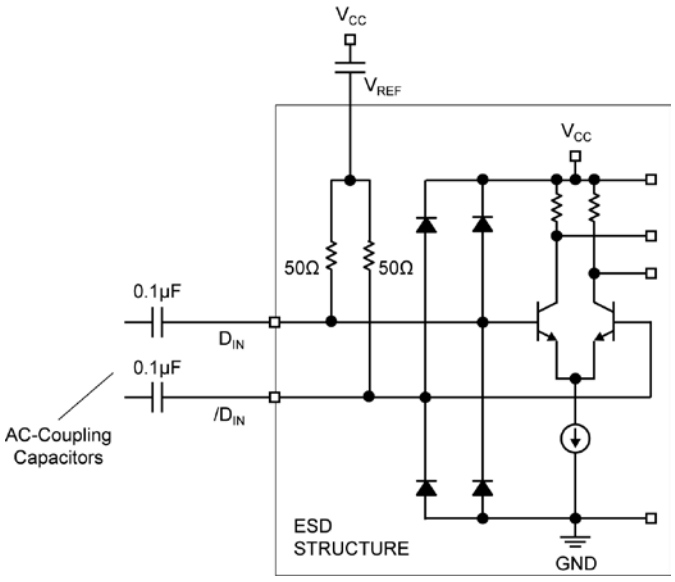


Figure 2. Input Structure

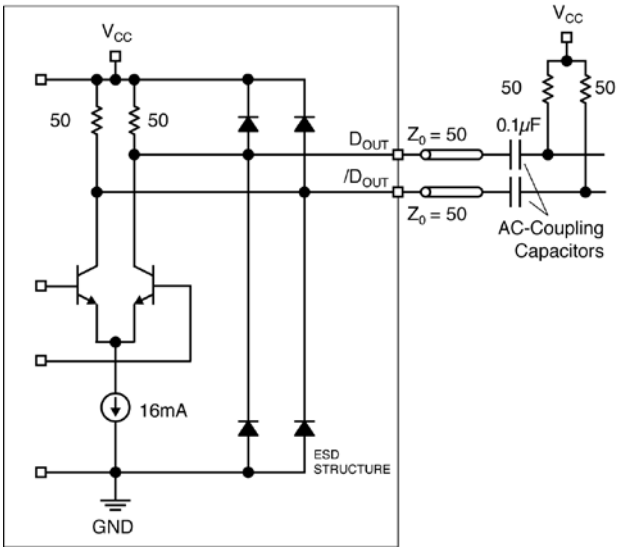


Figure 3. Output Structure

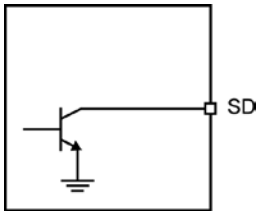


Figure 4. SD Output Structure

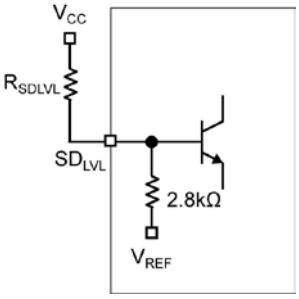
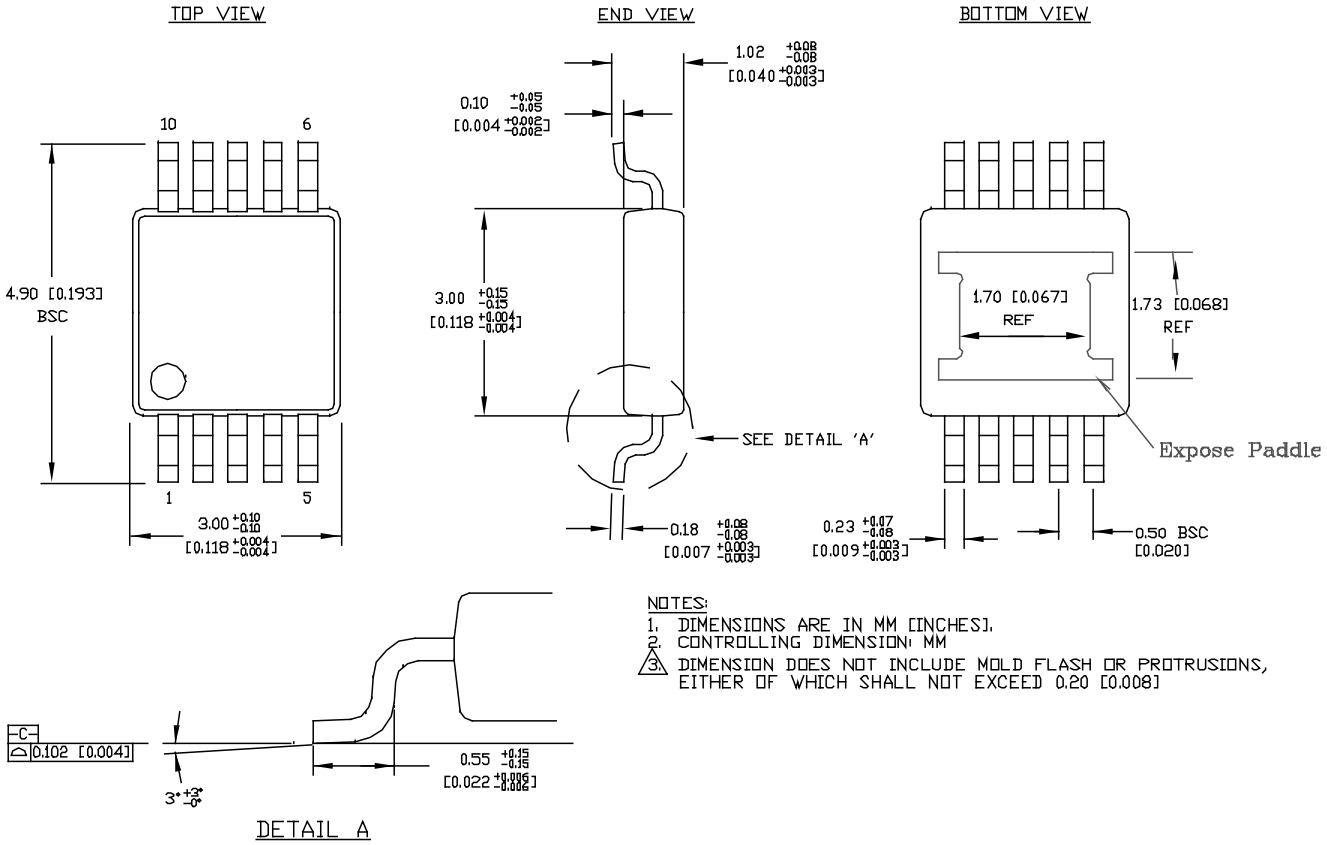
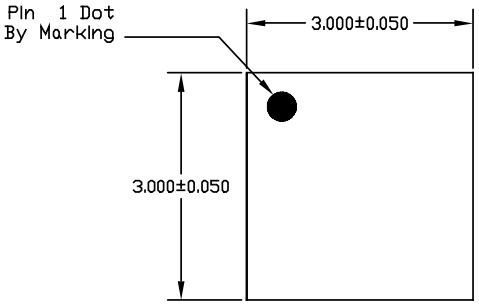


Figure 5. SD_{LVL} Setting Circuit

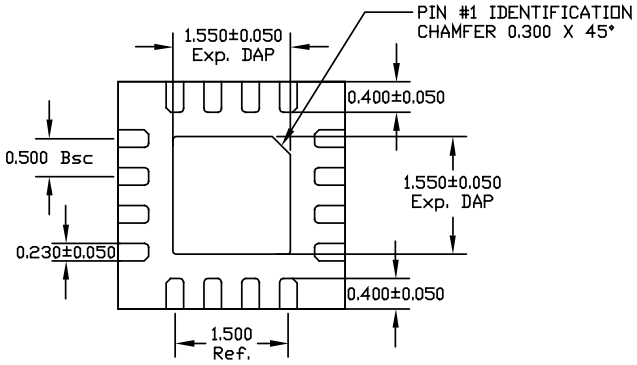
Package Information



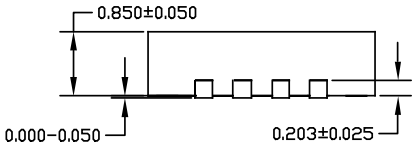
10-Pin EPAD-MSOP (K10-2)



TOP VIEW



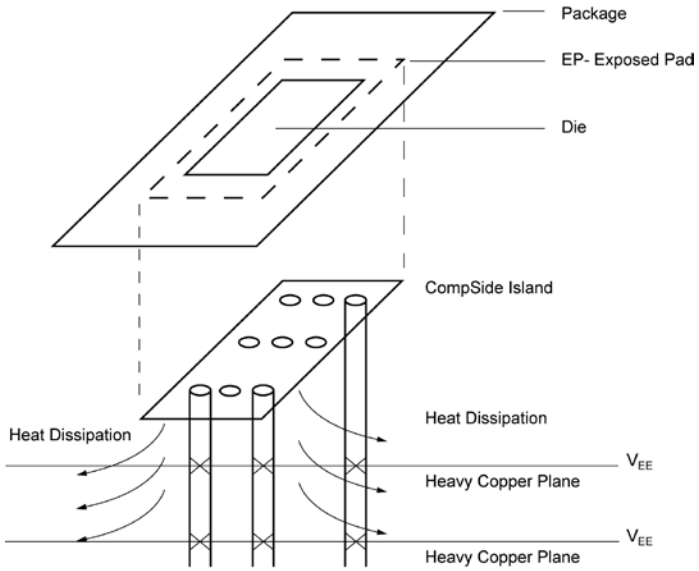
BOTTOM VIEW



SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.

16-Pin QFN



PCB Thermal Consideration for 16-Pin QFN Package
(Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pad must be soldered to a ground for proper thermal management, solder void has to be less than 50% of the epad area.

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