

FEATURES

- Three low-skew LVDS output banks with programmable $\div 1$, $\div 2$ and $\div 4$ divider options
- Three independently programmable output banks
- Guaranteed AC performance over temperature and voltage:
 - Accepts a clock frequency up to 1.5GHz
 - <900ps IN-to-OUT propagation delay
 - <150ps rise/fall time
 - <50ps bank-to-bank phase offset
- Ultra-low jitter design:
 - <1ps_{RMS} random jitter
 - <10ps_{pp} total jitter (clock)
- Patent-pending input termination and VT pin accepts DC- and AC-coupled inputs (CML, PECL, LVDS)
- LVDS-compatible outputs
- CMOS/TTL-compatible output enable (EN) and divider select control
- 2.5V $\pm 5\%$ power supply
- -40°C to $+85^{\circ}\text{C}$ temperature range
- Available in 32-pin (5mm $\times$ 5mm) MLF™ package

APPLICATIONS

- All SONET/SDH applications
- All Fibre Channel applications
- All Gigabit Ethernet applications

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MicroLeadFrame and MLF are trademarks of Amkor Technology, Inc.



Precision Edge®

DESCRIPTION

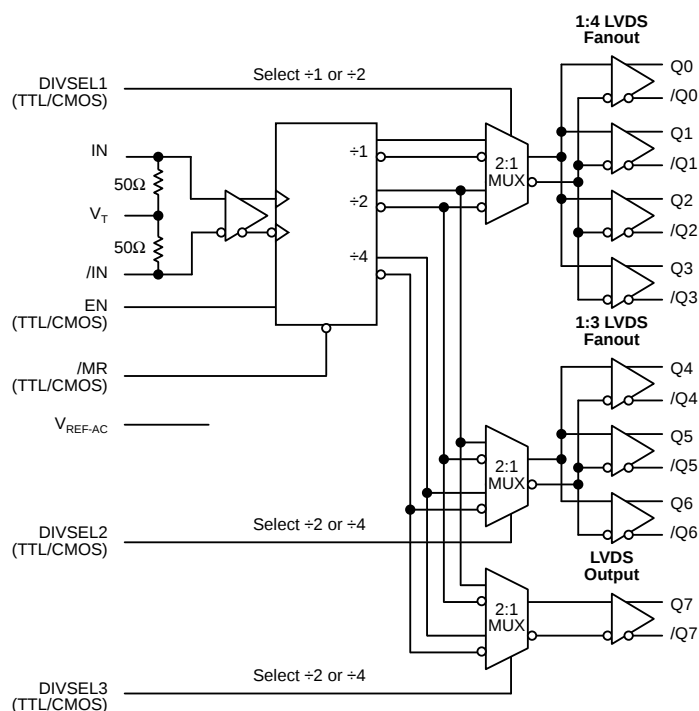
The SY89200U is a 2.5V precision, high-speed, integrated clock divider and LVDS fanout buffer capable of handling clocks up to 1.5GHz. Optimized for communications applications, the three independently controlled output banks are phase matched and can be configured for pass through ($\div 1$), $\div 2$ or $\div 4$ divider ratios.

The differential input includes Micrel's unique, 3-pin input termination architecture that allows the user to interface to any differential signal (AC or DC-coupled) as small as 200mV_{pp} without any level shifting or termination resistor networks in the signal path. The low-skew, low-jitter outputs are LVDS compatible with extremely fast rise/fall times guaranteed to be less than 150ps.

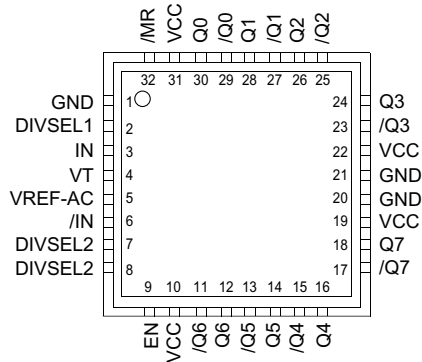
The EN (enable) input guarantees that the $\div 1$, $\div 2$ and $\div 4$ outputs will start from the same state without any runt pulse after an asynchronous master reset (MR) is asserted. This is accomplished by enabling the outputs after a four-clock delay to allow the counters to synchronize.

The SY89200U is part of a Micrel's Precision Edge® product family. All support documentation can be found at Micrel's web site at www.micrel.com.

FUNCTIONAL BLOCK DIAGRAM



PACKAGE/ORDERING INFORMATION



32-Pin MLF™ (MLF-32)

Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89200UMI	MLF-32	Industrial	SY89200U	Sn-Pb
SY89200UMITR ⁽²⁾	MLF-32	Industrial	SY89200U	Sn-Pb
SY89200UMG	MLF-32	Industrial	SY89200U with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY89200UMGTR ⁽²⁾	MLF-32	Industrial	SY89200U with Pb-Free bar-line indicator	Pb-Free NiPdAu

Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_A = 25^\circ\text{C}$, DC electricals only.
2. Tape and Reel.

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
3, 6	IN, /IN	Differential Input: This input pair is the differential signal input to the device. This input accepts AC- or DC-coupled signals as small as 100mV. The input pair internally terminates to a VT pin through 50Ω. Note that these inputs will default to an indeterminate state if left open. Please refer to the "Input Interface Applications" section for more details.
2 7 8	DIVSEL1 DIVSEL2 DIVSEL3	Single-Ended Inputs: These TTL/CMOS inputs select the divide ratio for each of the three banks of outputs. Note that each of these inputs is internally connected to a 25kΩ pull-up resistor and will default to a logic HIGH state if left open. The input switching threshold is $V_{CC}/2$.
4	VT	Input Termination Center-Tap: Each side of the differential input pair terminates to the VT pin. The VT pin provides a center-tap to a termination network for maximum interface flexibility. See "Input Interface Applications" section for more details.
5	VREF-AC	Reference Voltage: This output biases to $V_{CC}-1.2\text{V}$. It is used for AC-coupling inputs IN and /IN. For AC-coupled applications, connect VREF-AC directly to the VT pin. Bypass with 0.01μF low ESR capacitor to V_{CC} . Maximum sink/source capability is 0.5mA.
9	EN	Single-Ended Input: This TTL/CMOS input disables and enables the Q0 – Q7 outputs. This input is internally connected to a 25kΩ pull-up resistor and will default to a logic HIGH state if left open. The input switching threshold is $V_{CC}/2$. For the input enable and disable functional description, refer to Figures 2a through 2c.
30, 29, 28, 27, 26, 25, 24, 23	Q0, /Q0, Q1, /Q1, Q2, /Q2, Q3, /Q3	Bank 1 LVDS differential output pairs controlled by DIVSEL1: LOW, Q0 – Q3 = +1, HIGH, Q0 – Q3 = +2. Unused output pairs should be terminated with 100Ω across the differential pair.
16, 15, 14, 13, 12, 11	Q4, /Q4, Q5, /Q5, Q6, /Q6	Bank 2 LVDS differential output pairs controlled by DIVSEL2: LOW, Q4 – Q6 = +2, HIGH, Q4 – Q6 = +4. Unused output pairs should be terminated with 100Ω across the differential pair.
18, 17	Q7, /Q7	Bank 3 LVDS differential output pair controlled by DIVSEL3: LOW, Q7 = +2, HIGH, Q7 = +4. Unused output pair should be terminated with 100Ω across the differential pair.
32	/MR	Single-Ended Input: This TTL/CMOS-compatible master reset function asynchronously sets Q0 – Q7 outputs LOW, /Q0 – /Q7 outputs HIGH, and holds them in that state as long as /MR remains LOW. This input is internally connected to a 25kΩ pull-up resistor and will default to a logic HIGH state if left open. The input switching threshold is $V_{CC}/2$.
10, 19, 22, 31	VCC	Positive power supply. Bypass with 0.1μF 0.01μF low ESR capacitors.
1, 20, 21	GND, Exposed Pad	Ground and exposed pad must be connected to the same GND plane on the board.

TRUTH TABLE

/MR⁽¹⁾	EN^(2, 3)	DIVSEL1	DIVSEL2	DIVSEL3	Q0 – Q3	Q4 – Q6	Q7
0	X	X	X	X	0	0	0
1	0	X	X	X	0	0	0
1	1	0	0	0	÷1	÷2	÷2
1	1	1	1	1	÷2	÷4	÷4

Notes:

1. /MR asynchronously forces Q0 – Q7 LOW (/Q0 – /Q7 HIGH).
2. EN forces Q0 – Q7 LOW between 2 and 6 input clock cycles after the falling edge of EN. Refer to “Timing Diagram” section.
3. EN synchronously enables the outputs between two and six input clock cycles after the rising edge of EN. Refer to “Timing Diagram” section.

Absolute Maximum Ratings⁽¹⁾

Supply Voltage (V_{CC})	–0.5V to + 4.0V
Input Voltage (V_{IN})	–0.5V to V_{CC}
Termination Current ⁽³⁾	
Source or sink current on V_T	±100mA
Output Current	
Source or sink current on IN, /IN	±50mA
V_{REF_AC} Current ⁽³⁾	
Source or sink current on V_{REF_AC}	±2mA
Lead Temperature (soldering, 20 sec.)	+260°C
Storage Temperature (T_S)	–65°C to +150°C

Operating Ratings⁽²⁾

Supply Voltage (V_{CC})	+2.375V to +2.625V
Ambient Temperature (T_A)	–40°C to +85°C
Package Thermal Resistance ⁽⁴⁾	
MLF™ (θ_{JA})	
Still-Air	35°C/W
MLF™ (Ψ_{JB})	
Junction-to-board	20°C/W

DC ELECTRICAL CHARACTERISTICS

T_A = –40°C to +85°C; Unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply		2.375	2.5	2.625	V
I_{CC}	Power Supply Current	No load, max. V_{CC} ⁽⁶⁾			350	mA
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		80	100	120	Ω
R_{IN}	Input Resistance (IN-to V_T , /IN-to- V_T)		40	50	60	Ω
V_{IH}	Input High Voltage; (IN, /IN)		1.2		V_{CC}	V
V_{IL}	Input Low Voltage; (IN, /IN)		0		$V_{IH}-0.1$	V
V_{IN}	Input Voltage Swing; (IN, /IN)	See Figure 1a.	100		V_{CC}	mV
V_{DIFF_IN}	Differential Input Voltage Swing IN - /IN	See Figure 1b.	200		$2 \times V_{CC}$	mV
V_{REF_AC}	Reference Voltage		$V_{CC}-1.3$	$V_{CC}-1.2$	$V_{CC}-1.1$	V
IN-to- V_T	Voltage from Input to V_T				1.8	V

LVTTTL/CMOS DC ELECTRICAL CHARACTERISTICS⁽⁵⁾

V_{CC} = 2.5V ±5% ; T_A = –40°C to +85°C; Unless otherwise stated

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current		–125		30	μ A
I_{IL}	Input LOW Current				–300	μ A

Notes:

1. Permanent device damage may occur if ratings in the “Absolute Maximum Ratings” section are exceeded. This is a stress rating only and functional operation is not implied for conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Due to the limited drive capability use for input of the same package only.
4. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. Ψ_{JB} uses 4-layer θ_{JA} in still air unless otherwise noted.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6. Includes current through internal 50 Ω pull-ups.

LVDS OUTPUT DC ELECTRICAL CHARACTERISTICS⁽⁷⁾

$V_{CC} = 2.5V \pm 5\%$; $T_A = -40^\circ C$ to $+85^\circ C$; $R_L = 100\Omega$ across Q and /Q, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage; (Q, /Q)	See Figure 5a.			1.475	V
V_{OL}	Output LOW Voltage; (Q, /Q)	See Figure 5a.	0.925			V
V_{OUT}	Output Voltage Swing; (Q, /Q)	See Figure 1a.	250	350		mV
$V_{DIFF-OUT}$	Differential Output Voltage Swing Q - /Q	See Figure 1b.	500	700		mV
V_{OCM}	Output Common Mode Voltage (Q, /Q)	See Figure 5b.	1.125		1.275	V
ΔV_{OCM}	Change in Common Mode Voltage (Q, /Q)	See Figure 5b.	-50		+50	mV

AC ELECTRICAL CHARACTERISTICS⁽⁸⁾

$V_{CC} = 2.5V \pm 5\%$; $T_A = -40^\circ C$ to $+85^\circ C$; $R_L = 100\Omega$ across all outputs (Q and /Q), unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	$V_{OUT} > 200mV$ Clock	1.5			GHz
t_{pd}	Differential Propagation Delay	IN-to-Q	500	700	900	ps
		/MR-to-Q			900	ps
t_{RR}	Reset Recovery Time	/MR(L-H)-to-(L-H)			900	ps
$t_{pd} \text{ Tempco}$	Differential Propagation Delay Temperature Coefficient			115		fs/°C
t_{SKEW}	Within-Bank Skew	Within same fanout bank, Note 9		10	25	ps
	Bank-to-Bank Skew	Same divide setting, Note 10		15	35	ps
	Bank-to-Bank Skew	Different divide setting, Note 10		25	50	ps
	Part-to-Part Skew	Note 11			200	ps
t_{JITTER}	Random Jitter (RJ)	Note 12			1	ps _{RMS}
	Total Jitter (TJ)	Note 13			10	ps _{PP}
	Cycle-to-Cycle Jitter	Note 14			1	ps _{RMS}
t_r, t_f	Rise/Fall Time	20% to 80%, at full output swing.	40	80	150	ps

Notes:

- The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
- Measured with 100mV input swing. See "Timing Diagrams" section for definition of parameters. High-frequency AC-parameters are guaranteed by design and characterization.
- Within-bank is the difference in propagation delays among the outputs within the same bank.
- Bank-to-bank skew is the difference in propagation delays between outputs from different banks. Bank-to-bank skew is also the phase offset between each bank, after MR is applied.
- Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.
- RJ is measured with a K28.7 comma detect character pattern.
- Total jitter definition: with an ideal clock input of frequency $\leq f_{MAX}$, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.
- Cycle-to-cycle jitter definition: The variation of periods between adjacent cycles, $T_n - T_{n-1}$ where T is the time between rising edges of the output signal.

SINGLE ENDED DIFFERENTIAL SWINGS



Figure 1a. Single-Ended Voltage Swing

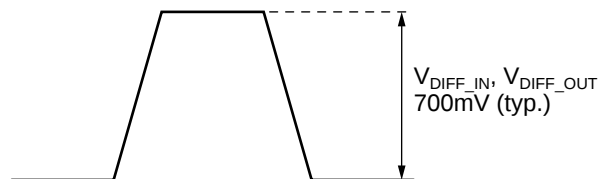


Figure 1a. Differential Voltage Swing

TIMING DIAGRAM

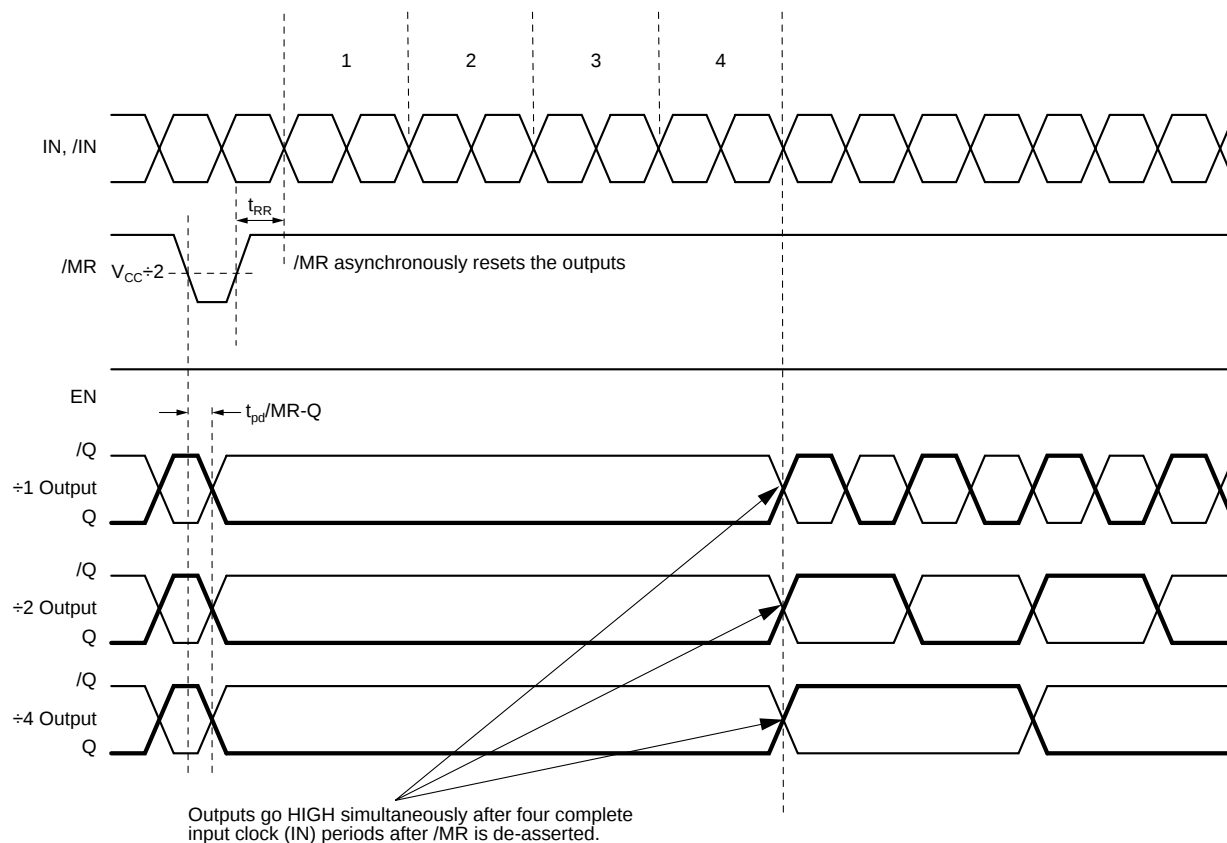


Figure 2a. Reset with Output Enabled

TIMING DIAGRAMS

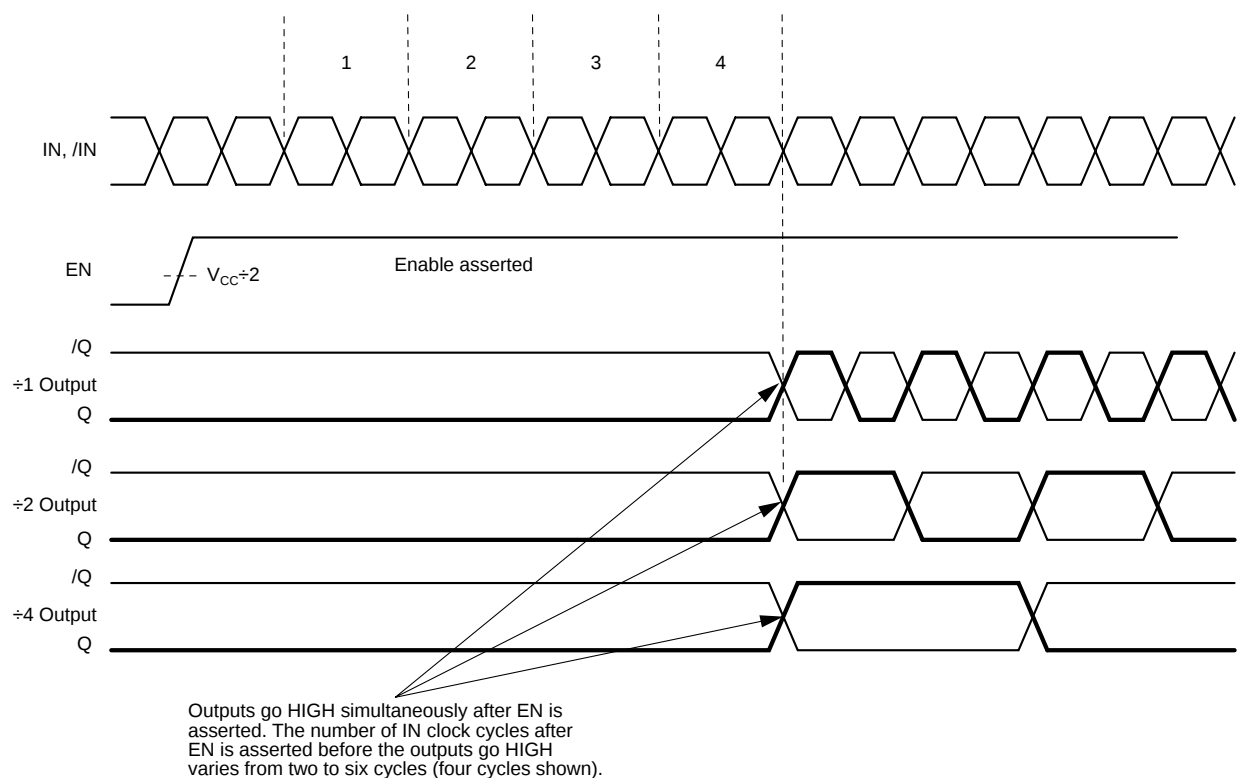


Figure 2b. Enable Timing

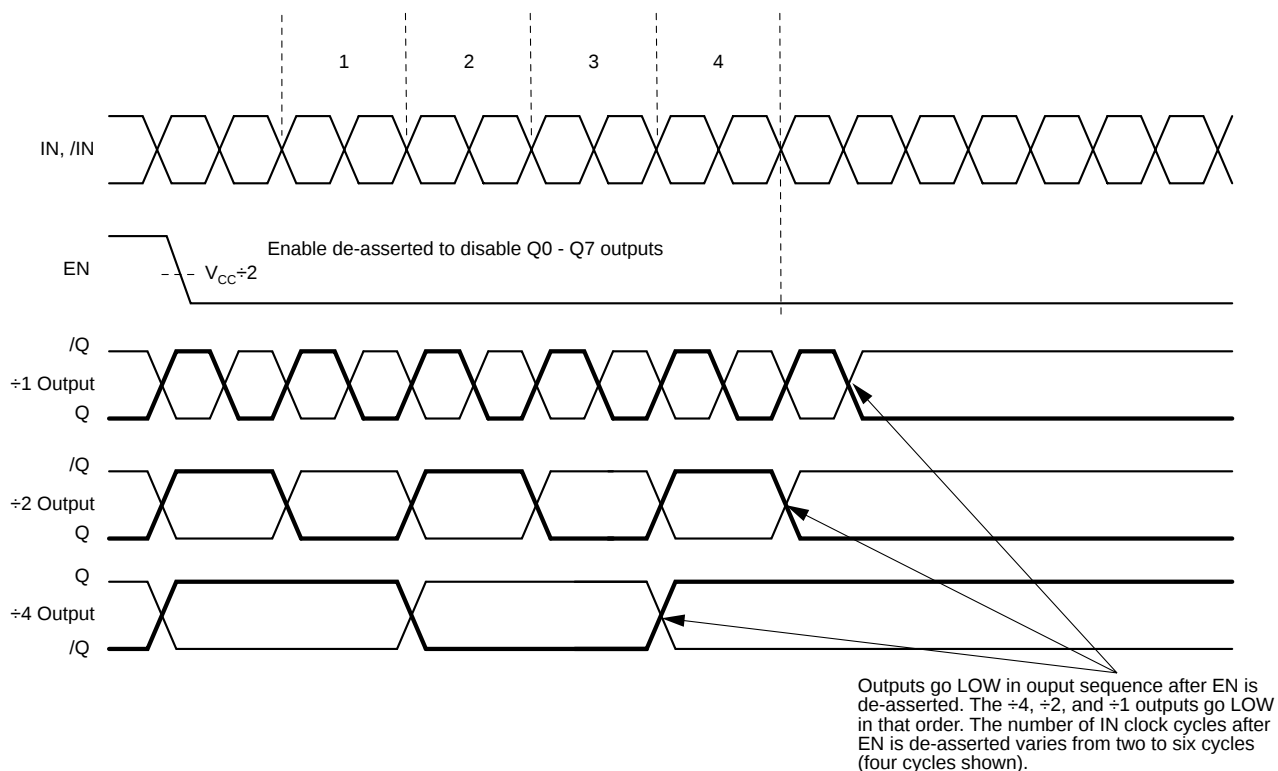
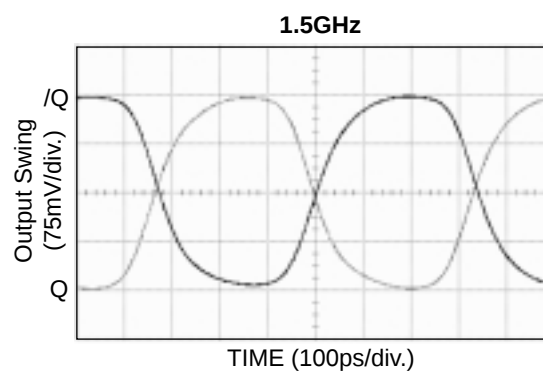
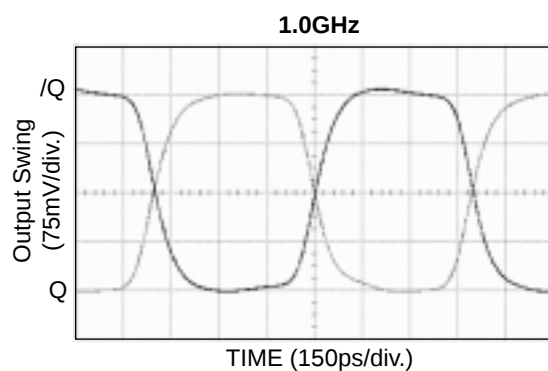
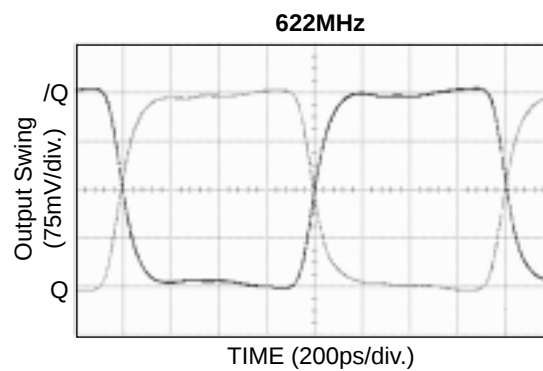
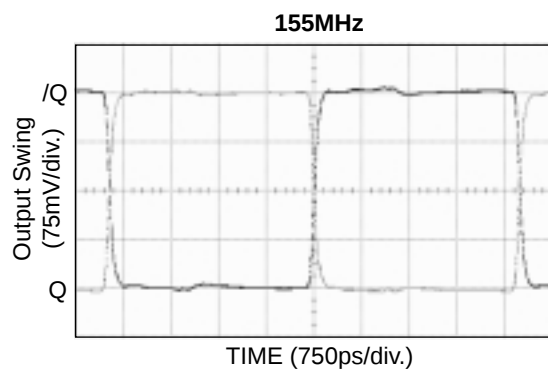


Figure 2c. Disable Timing

TYPICAL OPERATING CHARACTERISTICS

INPUT STAGE INTERNAL TERMINATION

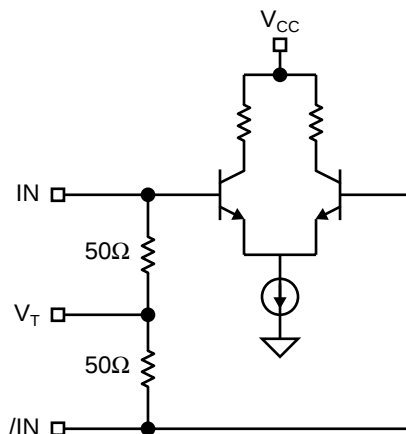


Figure 3. Simplified Differential Input Stage

INPUT INTERFACE APPLICATIONS

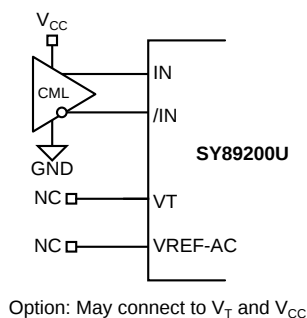


Figure 4a. CML Interface
(DC-Coupled)

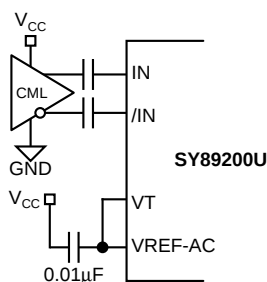


Figure 4b. CML Interface
(AC-Coupled)

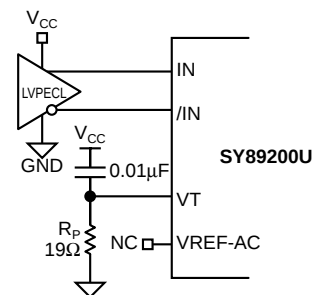


Figure 4c. LVPECL Interface
(DC-Coupled)

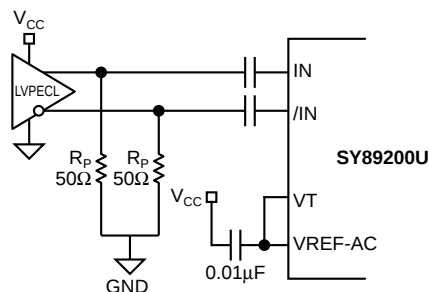


Figure 4d. LVPECL Interface
(AC-Coupled)

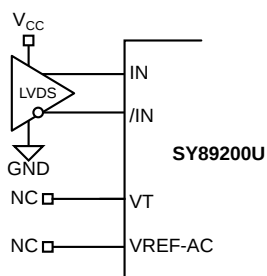


Figure 4e. LVDS Interface

OUTPUT INTERFACE APPLICATIONS

LVDS specifies a small swing of 350mV typical, on a nominal 1.25V common mode above ground. The common mode voltage has tight limits to permit large variations in ground between an LVDS driver and receiver. Also, change in common mode voltage, as a function of data input, is kept to a minimum, to keep EMI low.

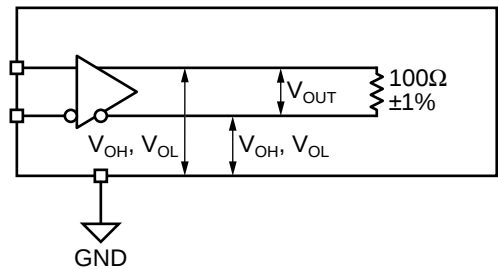


Figure 5a. LVDS Differential Measurement

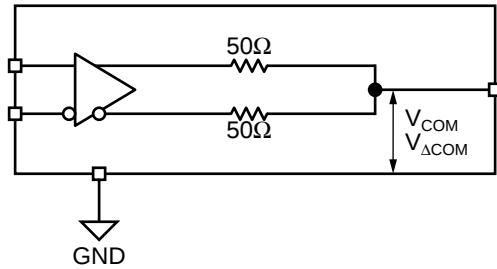


Figure 5b. LVDS Common Mode Measurement

RELATED PRODUCT AND SUPPORT DOCUMENTATION

Part Number	Function	Data Sheet Link
	MLF™ Application Note	www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

Diagram illustrating the pin layout for a 2x2 array. The array is square with a side length of 5.0 BSC. The pins are numbered 1, 2, 3, and 4 in a clockwise direction starting from the top-left pin. The top-left pin is also labeled "PIN #1 ID 0.20 DIA. TYP." with a leader line. The array is divided into four quadrants by dashed center lines. The top-left quadrant is labeled "32".

This diagram illustrates the cross-sectional structure of a power module assembly. At the top, a **Package** is shown with an **EP- Exposed Pad** and a **Die**. Below the package is a **CompSide Island** containing several circular features. The assembly is mounted on a **Heavy Copper Plane**, which is connected to a **V_{EE}** terminal. Arrows indicate **Heat Dissipation** from the package and the copper plane. The bottom of the assembly is another **Heavy Copper Plane**, also connected to a **V_{EE}** terminal.

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

11