



**3.3V 2.5Gbps
ANY INPUT-to-LVPECL
DIFFERENTIAL TRANSLATOR**

**Precision Edge®
SY89327L**

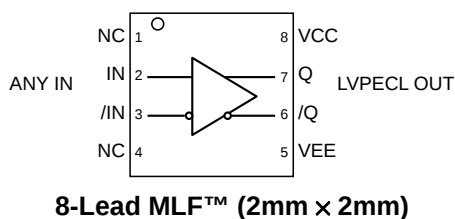
FEATURES

- Input accepts virtually all logic standards:
 - Single-ended: SSTL, TTL, CMOS
 - Differential: LVDS, HSTL, CML
- Guaranteed AC performance over temp and voltage:
 - DC-to >2.5Gbps data rate throughput
 - DC-to >2.5GHz clock f_{MAX}
 - < 400ps In-to-Out t_{pd}
 - < 200ps t_r/t_f
- Ultra-low jitter design:
 - <1ps_{RMS} random jitter
 - <10ps_{pp} deterministic jitter
 - <1ps_{RMS} cycle-to-cycle jitter
 - <10ps_{pp} total jitter (clock)
- Low power: 46mW (typ)
- 100k LVPECL output
- Flow-through pinout and fully differential design
- Power supply 3.3V $\pm 10\%$
- -40°C to +85°C temperature range
- Available in ultra-small 8-lead 2mm x 2mm MLF™ package

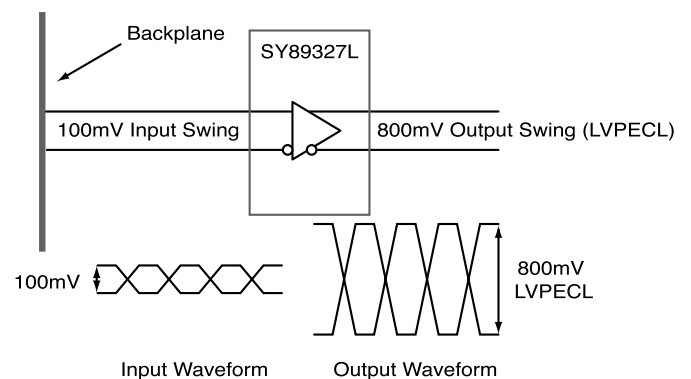
APPLICATIONS

- High-speed logic
- Data communications systems
- Wireless communications systems
- Telecom systems

FUNCTIONAL BLOCK DIAGRAM



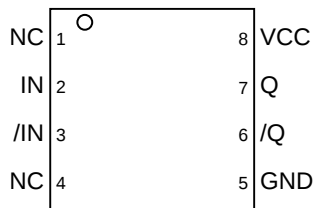
TYPICAL APPLICATIONS CIRCUIT



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MicroLeadFrame and MLF are trademarks of Amkor Technology, Inc.

PACKAGE/ORDERING INFORMATION

Ordering Information



8-Lead MLF™

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89327LMITR	MLF-8	Industrial	327	Sn-Pb
SY89325LMGTR	MLF-8	Industrial	327 with Pb-Free bar-line indicator	Pb-Free NiPdAu

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
2, 3	IN, /IN	Differential inputs: This input is the differential signal input to the device. This input accepts AC- or DC-coupled signals as small as 100mV. External termination is required. Please refer to the "Input Interface Applications" section for more details.
8	VCC	Positive power supply. Bypass with 0.1μF 0.01μF low ESR capacitors.
7, 6	Q, /Q	Differential LVPECL Output: Terminate with 50Ω to V _{CC} -2V. See "Output Interface Applications" section. Output pair is 100k temperature compensated LVPECL compatible.
5	GND, Exposed Pad	Ground: Ground pin and exposed pad must be connected to the same ground plane.
1, 4	NC	No connect.

FUNCTIONAL DESCRIPTION

Establishing Static Logic Inputs

Do not leave unused inputs floating. Tie either the true or complement input to ground. A logic zero is achieved by connecting the complement input to ground with the true input floating. For a TTL input, tie a 2.5kΩ resistor between the complement input and ground. See "Input Interface" section.

Input Levels

LVDS, CML, and HSTL differential signals may be connected directly to the D inputs. Depending on the actual worst case voltage seen, the SY8327L's performance varies as per the following table:

Input Voltage Range	Minimum Voltage Swing	Maximum Translation Speed
0 to 2.4V	100mV	2.5Gbps
0 to V _{CC} +0.3V	200mV	1.25Gbps

For LVDS applications, only point-to-point interfaces are supported. Due to the current required by the input structure shown in Figure 1, multi-drop and multi-point architectures are not supported.

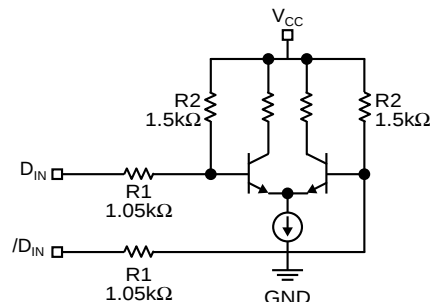


Figure 1. Simplified Input Structure

Absolute Maximum Ratings⁽¹⁾

Supply Voltage (V_{CC})	 -0.5V to + 4.0V
Input Voltage (V_{IN})	 -0.5V to V_{CC}
Input Current	
Source or sink current on I_N , $/I_N$	 ± 50 mA
Lead Temperature (soldering, 20 sec.)	 +260°C
Storage Temperature (T_S)	 -65°C to +150°C

Operating Ratings⁽²⁾

Supply Voltage (V_{CC})	 3.0V to 3.6V
Ambient Temperature (T_A)	 -40°C to +85°C
Package Thermal Resistance ⁽³⁾	
MLF™ (θ_{JA})	
Still-Air	 93°C/W
500lfpm	 87°C/W
MLF™ (Ψ_{JB})	
Junction-to-Board	 32°C/W

DC ELECTRICAL CHARACTERISTICS⁽⁴⁾

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$; unless stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply		3.0	3.3	3.6	V
I_{CC}	Power Supply Current	No load, max. V_{CC} ⁽⁵⁾		28	45	mA

INPUT ELECTRICAL CHARACTERISTICS⁽⁴⁾

$V_{CC} = 3.3\text{V} \pm 10\%$; $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$; $R_L = 50\Omega$ to $V_{CC} - 2\text{V}$, or equivalent, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage	V_{IH} min must be $\geq 1.2\text{V}$			$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage		-0.3			V
V_{IN}	Input Voltage Swing	See Figure 2a, $V_{IH} < 2.4\text{V}$	100			mV
		See Figure 2a, $V_{IH} < V_{CC} + 0.3\text{V}$	200			mV

LVPECL OUTPUT DC ELECTRICAL CHARACTERISTICS⁽⁴⁾

$V_{CC} = 3.3\text{V} \pm 10\%$; $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$; $R_L = 50\Omega$ to $V_{CC} - 2\text{V}$, or equivalent, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OL}	Output HIGH Voltage $Q, /Q$		$V_{CC} - 1.945$		$V_{CC} - 1.695$	V
V_{OH}	Output Common Mode Range $Q, /Q$		$V_{CC} - 1.145$		$V_{CC} - 0.895$	V
V_{OUT}	Output Voltage Swing $Q, /Q$	See Figure 2a	550	800		mV
$V_{DIFF-OUT}$	Differential Output Voltage Swing $Q, /Q$	See Figure 2b	1100	1600		mV _{PP}

Notes:

1. Permanent device damage may occur if the "Absolute Maximum Ratings" are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package Thermal Resistance assumes exposed pad is soldered (or equivalent) to the devices' most negative potential on the PCB. Ψ_{JB} uses 4-layer θ_{JA} in still-air unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

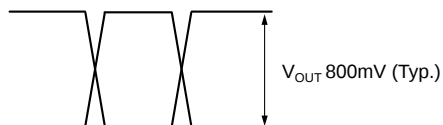
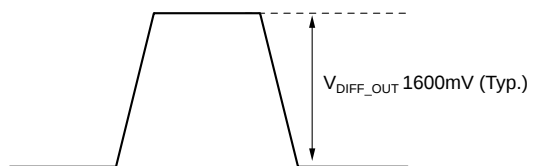
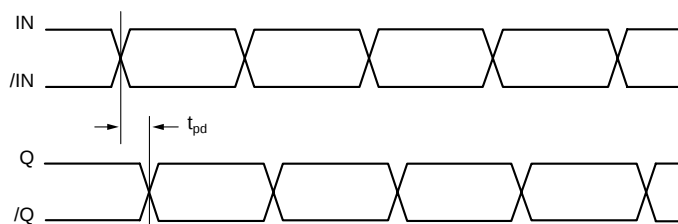
AC ELECTRICAL CHARACTERISTICS (5)

$V_{CC} = 3.3V \pm 10\%$; $T_A = -40^\circ C$ to $+85^\circ C$; $R_L = 50\Omega$ to $V_{CC} - 2V$, or equivalent, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	NRZ Data	2.5			Gbps
		$V_{OUT} \geq 200mV$ Clock		2.5		GHz
t_{pd}	Propagation Delay IN-to-Q, /IN-to-/Q	$V_{IN} \geq 100mV$			400	ps
t_{JITTER}	Random Jitter (RJ)	Note 6			1	ps _{RMS}
	Deterministic Jitter (DJ)	Note 7			10	ps _{PP}
	Total Jitter (TJ)	Note 8			10	ps _{PP}
t_r, t_f	Rise / Fall Time (20% to 80%) Q, /Q	At full output swing			200	ps

Notes:

- See "Timing Diagrams" section for definition of parameters. High frequency AC-parameters are guaranteed by design and characterization.
- RJ is measured with a K28.7 comma detect character pattern, measured at f_{MAX} .
- DJ is measured at 2.5Gbps, with both K28.5 and 2²³-1 PRBS pattern.
- Total jitter definition: with an ideal clock input of frequency $\leq f_{MAX}$, no more than one output edge in 10¹² output edges will deviate by more than the specified peak-to-peak jitter value.

SINGLE-ENDED AND DIFFERENTIAL SWINGS**Figure 2a. Single-Ended Voltage Swing****Figure 2b. Differential Voltage Swing****TIMING DIAGRAM****Figure 3. Timing Diagram**

INPUT INTERFACE APPLICATIONS

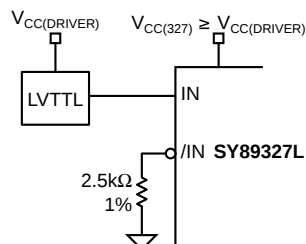


Figure 4. 3.3V "TTL"

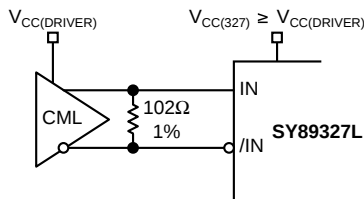


Figure 5. CML-DC Coupled

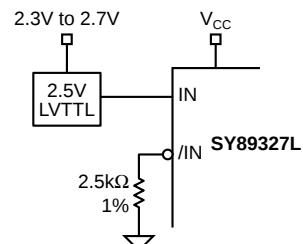


Figure 6. 2.5V "TTL"

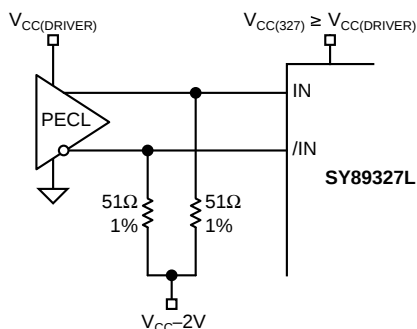


Figure 7. PECL-DC Coupled

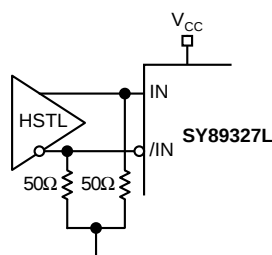


Figure 8. HSTL

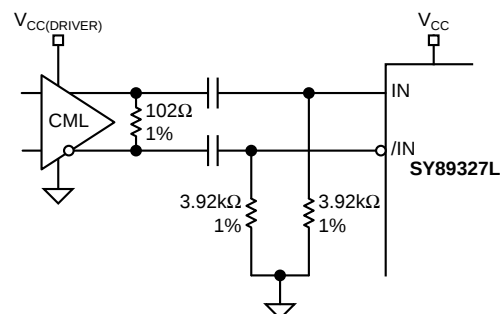
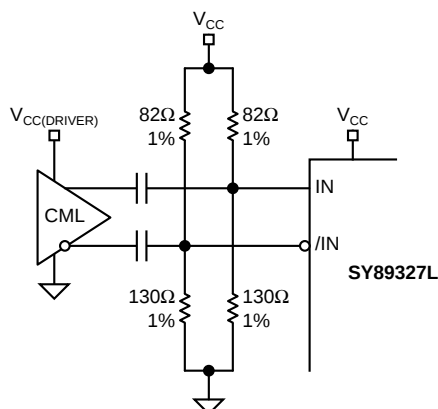
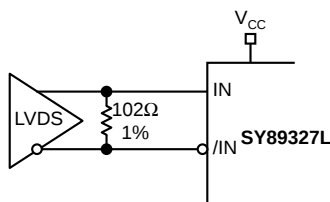
Figure 9. CML-AC Coupled
Short LinesFigure 10. CML-AC Coupled
Long Lines

Figure 11. LVDS

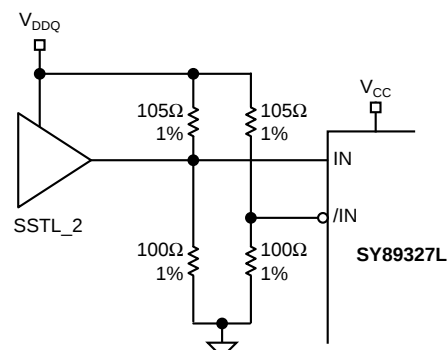


Figure 12. SSTL_2

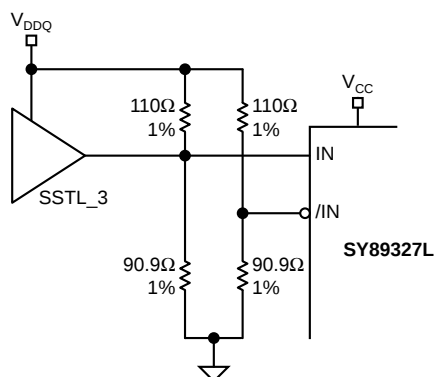
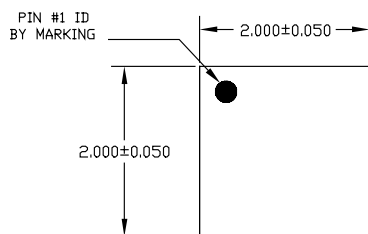


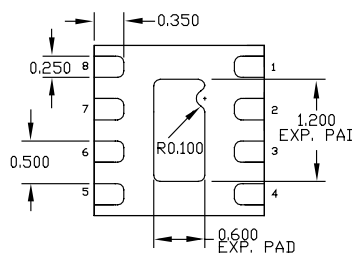
Figure 13. SSTL_3

RELATED PRODUCT AND SUPPORT DOCUMENTATION

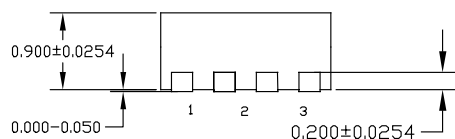
Part Number	Function	Data Sheet Link
SY55857L	3.3V, 2.5Gbps Any Input-to-LVPECL Dual Translator	www.micrel.com/product-info/products/sy55857l.shtml
	MLF™ Application Note	www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

8 LEAD MicroLeadFrame (MLF-8)

TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.

Package Notes:

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA

TEL + 1 (408) 944-0800 FAX + 1 (408) 474-1000 WEB <http://www.micrel.com>

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