



## SY898531L

### Precision Differential 3.3V Low Skew LVPECL 1:9 Fanout Buffer

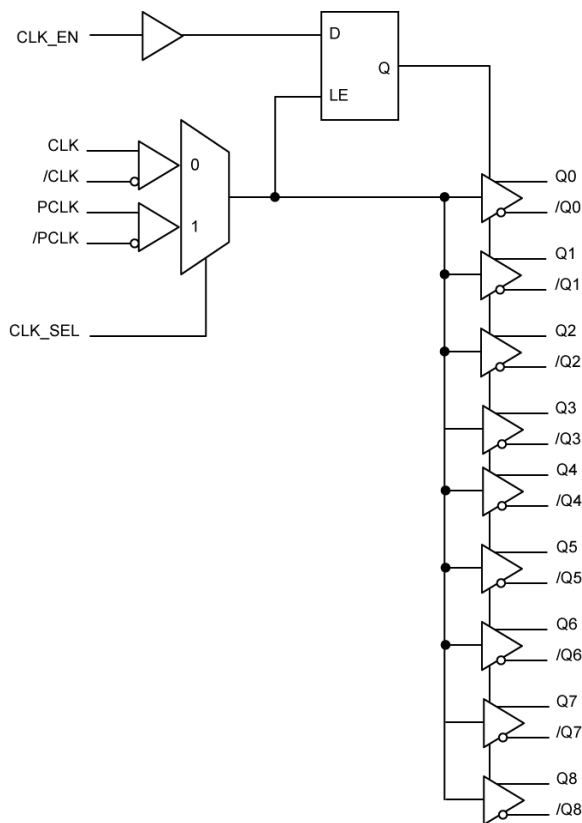
## General Description

The SY898531L is a 3.3V, low skew, 1:9 LVPECL fanout buffer with two selectable clock input pairs. Most standard differential input levels can be applied to the CLK, /CLK pair while LVPECL, CML, or SSTL input levels can be applied to the PCLK, /PCLK pair. To eliminate runt pulses on the outputs during asynchronous assertion/de-assertion of the clock enable pin, the clock enable is synchronized with the input signal.

The SY898531L operates from a 3.3V  $\pm 5\%$  supply and is guaranteed over the full industrial temperature range of 0°C to +70°C. The SY898531L is part of Micrel's high-speed, Precision Edge<sup>®</sup> product line.

Datasheets and support documentation can be found on Micrel's web site at: [www.micrel.com](http://www.micrel.com).

## Functional Block Diagram



Precision Edge<sup>®</sup>

## Features

- Provides nine differential 3.3V LVPECL copies
- Selects between differential CLK, /CLK or LVPECL clock inputs
- CLK, /CLK pair accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL input levels
- PCLK, /PCLK pair accepts LVPECL, CML, SSTL input levels
- Guaranteed AC performance over temperature and supply voltage:
  - 500MHz Maximum output frequency
  - < 2ns Propagation delay (In-to-Q)
  - < 50ps Output skew
  - < 250ps Part-to-part skew
  - Additive phase jitter, RMS: 0.17ps (typical)
- 3.3V  $\pm 5\%$  supply voltage
- 0°C to +70°C temperature operating range
- Available in a 32-pin TQFP package

## Applications

- SONET clock distribution
- Backplane distribution

## Markets

- LAN/WAN
- Enterprise servers
- ATE
- Test and measurement

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Micrel Inc. • 2180 Fortune Drive • San Jose, CA 95131 • USA • tel +1 (408) 944-0800 • fax + 1 (408) 474-1000 • <http://www.micrel.com>

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[hbwhelp@micrel.com](mailto:hbwhelp@micrel.com) or (408) 955-1690

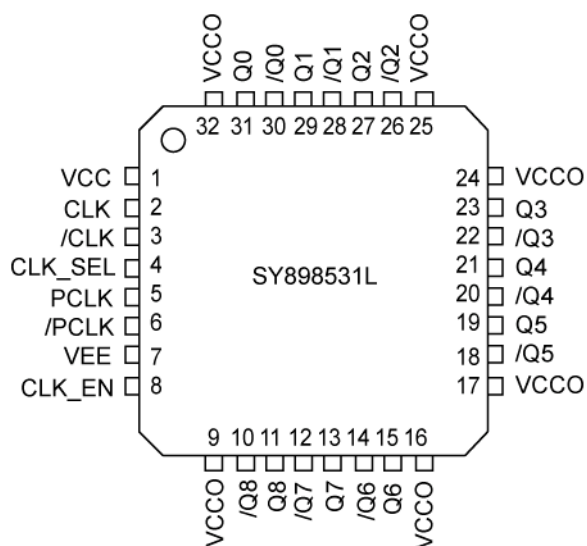
## Ordering Information

| Part Number                  | Package Type | Operating Range | Package Marking                             | Lead Finish       |
|------------------------------|--------------|-----------------|---------------------------------------------|-------------------|
| SY898531LTZ                  | T32-1        | Commercial      | SY898531LTZ with Pb-Free bar-line Indicator | Matte-tin Pb-Free |
| SY898531LTZTR <sup>(2)</sup> | T32-1        | Commercial      | SY898531LTZ with Pb-Free bar-line Indicator | Matte-tin Pb-Free |

**Notes:**

1. Contact factory for die availability. Dice are guaranteed at  $T_A = 25^{\circ}\text{C}$ , DC Electricals Only.
2. Tape and Reel.

## Pin Configuration



32-Pin TQFP (T32-1)

## Pin Description

| Pin Number                                                                             | Pin Name                                                                                        | Pin Function                                                                                                                                                                                                                                                                                                                                                                                                                     |
|----------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7                                                                                      | V <sub>EE</sub>                                                                                 | Ground.                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 8                                                                                      | CLK_EN                                                                                          | Single-Ended Input: This TTL/CMOS input disables and enables the Q0-Q8 outputs. It is internally connected to a 50kΩ pull-up resistor and will default to a logic HIGH state if left open. When disabled, Q goes LOW and /Q goes HIGH. Since CLK_EN is synchronous with the input clock, the outputs will be enabled/disabled following a rising and a falling edge of the input clock. V <sub>TH</sub> = is approximately 1.5V. |
| 4                                                                                      | CLK_SEL                                                                                         | Single-Ended Input: This single-ended TTL/CMOS-compatible input selects the input to the multiplexer. Note that this input is internally connected to a 50kΩ pull-down resistor and will default to logic LOW state if left open. V <sub>TH</sub> = is approximately 1.5V.                                                                                                                                                       |
| 2, 3                                                                                   | CLK, /CLK                                                                                       | Differential Input: This input pair is a differential signal input to the device. This input accepts AC- or DC-coupled signals. CLK is internally connected to a 28kΩ pull-down resistor and will default to a logic LOW state if left open while /CLK is connected to a 50kΩ pull-up resistor and will default to a logic HIGH state if left open. This input pair is selected when CLK_SEL is set to logic LOW.                |
| 5, 6                                                                                   | PCLK, /PCLK                                                                                     | Differential Input: This input pair is a differential signal input to the device. This input accepts AC- or DC-coupled signals. PCLK is internally connected to a 50kΩ pull-down resistor and will default to a logic LOW state if left open while /PCLK is connected to a 50kΩ pull-up resistor and will default to a logic HIGH state if left open. This input pair is selected when CLK_SEL is set to logic HIGH.             |
| 1                                                                                      | V <sub>CC</sub>                                                                                 | Positive Power Supply Pin: Bypass with 0.1μF  0.01μF low ESR capacitor as close to the V <sub>CC</sub> pin as possible.                                                                                                                                                                                                                                                                                                          |
| 9, 16, 17, 24, 25, 32                                                                  | V <sub>CCO</sub>                                                                                | Output Positive Power Supply Pins: Bypass with 0.1μF  0.01μF low ESR capacitors as close to the V <sub>CCO</sub> pins as possible.                                                                                                                                                                                                                                                                                               |
| 30, 31<br>28, 29<br>26, 27<br>22, 23<br>20, 21<br>18, 19<br>14, 15<br>12, 13<br>10, 11 | Q0, /Q0<br>Q1, /Q1<br>Q2, /Q2<br>Q3, /Q3<br>Q4, /Q4<br>Q5, /Q5<br>Q6, /Q6<br>Q7, /Q7<br>Q8, /Q8 | LVPECL Differential Output Pairs: Differential buffered output copies of the selected input signal. The output swing is typically 800mV. Unused output pairs may be left floating with no impact on jitter. These differential LVPECL outputs are a logic function of the CLK, /CLK and PCLK, /PCLK, and CLK_SEL inputs. See "Truth Table" below.                                                                                |

## Truth Table

| Inputs |         |                 | Outputs        |                 |
|--------|---------|-----------------|----------------|-----------------|
| CLK_EN | CLK_SEL | Selected Source | Q0 :Q8         | /Q0:/Q8         |
| 0      | 0       | CLK, /CLK       | Disabled : LOW | Disabled : HIGH |
| 0      | 1       | PCLK, /PCLK     | Disabled : LOW | Disabled : HIGH |
| 1      | 0       | CLK, /CLK       | CLK            | /CLK            |
| 1      | 1       | PCLK, /PCLK     | PCLK           | /PCLK           |

**Absolute Maximum Ratings<sup>(1)</sup>**

Supply Voltage ( $V_{CC}$ ) ..... -0.5V to +4.6V  
 Input Voltage ( $V_{IN}$ ) ..... -0.5V to  $V_{CC}$  +0.5V  
 LVPECL Output Current ( $I_{OUT}$ ) .....  
     Continuous ..... 50mA  
     Surge ..... 100mA  
 Lead Temperature (soldering, 20 sec.) ..... +260°C  
 Storage Temperature ( $T_s$ ) ..... -65°C to 150°C

**Operating Ratings<sup>(2)</sup>**

Supply Voltage ( $V_{CC}$ ) ..... +3.135V to +3.465V  
 Ambient Temperature ( $T_A$ ) ..... 0°C to +70°C  
 Package Thermal Resistance<sup>(3)</sup>  
     TSSOP ( $\theta_{JA}$ ) .....  
     Still-Air ..... 50°C/W

**Power Supply DC Electrical Characteristics<sup>(4)</sup>**

$V_{CC} = V_{CCO} = 3.3V \pm 5\%$ ;  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ , unless otherwise stated.

| Symbol    | Parameter            | Condition             | Min   | Typ | Max   | Units |
|-----------|----------------------|-----------------------|-------|-----|-------|-------|
| $V_{CC}$  | Power Supply         |                       | 3.135 | 3.3 | 3.465 | V     |
| $V_{CCO}$ | Output Power Supply  |                       | 3.135 | 3.3 | 3.465 | V     |
| $I_{EE}$  | Power Supply Current | No load, max $V_{CC}$ |       |     | 80    | mA    |

**LVCMOS/LVTTL DC Electrical Characteristics<sup>(4)</sup>**

$V_{CC} = V_{CCO} = 3.3V \pm 5\%$ ;  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ , unless otherwise stated.

| Symbol   | Parameter          | Condition                                 | Min  | Typ | Max            | Units         |
|----------|--------------------|-------------------------------------------|------|-----|----------------|---------------|
| $V_{IH}$ | Input High Voltage |                                           | 2    |     | $V_{CC} + 0.3$ | V             |
| $V_{IL}$ | Input Low Voltage  |                                           | -0.3 |     | 0.8            | V             |
| $I_{IH}$ | Input High Current | CLK_EN<br>$V_{IN} = V_{CC} = 3.465V$      |      |     | 5              | $\mu\text{A}$ |
|          |                    | CLK_SEL<br>$V_{IN} = V_{CC} = 3.465V$     |      |     | 150            | $\mu\text{A}$ |
| $I_{IL}$ | Input Low Current  | CLK_EN<br>$V_{IN} = 0V, V_{CC} = 3.465V$  | -150 |     |                | $\mu\text{A}$ |
|          |                    | CLK_SEL<br>$V_{IN} = 0V, V_{CC} = 3.465V$ | -5   |     |                | $\mu\text{A}$ |

**Differential DC Electrical Characteristics<sup>(4)</sup>**

$V_{CC} = V_{CCO} = 3.3V \pm 5\%$ ;  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ , unless otherwise stated.

| Symbol    | Parameter                                   | Condition                                | Min            | Typ | Max             | Units         |
|-----------|---------------------------------------------|------------------------------------------|----------------|-----|-----------------|---------------|
| $I_{IH}$  | Input High Current                          | CLK<br>$V_{IN} = V_{CC} = 3.465V$        |                |     | 150             | $\mu\text{A}$ |
|           |                                             | /CLK<br>$V_{IN} = V_{CC} = 3.465V$       |                |     | 5               | $\mu\text{A}$ |
| $I_{IL}$  | Input Low Current                           | CLK<br>$V_{IN} = 0.5V, V_{CC} = 3.465V$  | -5             |     |                 | $\mu\text{A}$ |
|           |                                             | /CLK<br>$V_{IN} = 0.5V, V_{CC} = 3.465V$ | -150           |     |                 | $\mu\text{A}$ |
| $V_{PP}$  | Peak-to-Peak Input Voltage                  |                                          | 0.15           |     | 1.3             | V             |
| $V_{CMR}$ | Common Mode Input Voltage <sup>(5, 6)</sup> |                                          | $V_{EE} + 0.5$ |     | $V_{CC} - 0.85$ | V             |

**Notes:**

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3.  $\theta_{JA}$  value is determined for a 4-layer board in still air unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
5. Maximum input voltage for CLK and /CLK is  $V_{CC} + 0.3V$  for single ended applications.
6.  $V_{IH}$  is defined as the common mode voltage.

## LVPECL DC Electrical Characteristics<sup>(7)</sup>

$V_{CC} = V_{CCO} = 3.3V \pm 5\%$ ;  $T_A = 0^\circ C$  to  $+70^\circ C$ , unless otherwise stated.

| Symbol      | Parameter                                   | Condition                      | Min            | Typ | Max            | Units   |
|-------------|---------------------------------------------|--------------------------------|----------------|-----|----------------|---------|
| $I_{IH}$    | Input High Current PCLK<br>/PCLK            | $V_{IN} = V_{CC} = 3.465V$     |                |     | 150            | $\mu A$ |
|             |                                             | $V_{IN} = V_{CC} = 3.465V$     |                |     | 5              | $\mu A$ |
| $I_{IL}$    | Input Low Current PCLK<br>/PCLK             | $V_{IN} = 0V, V_{CC} = 3.465V$ | -5             |     |                | $\mu A$ |
|             |                                             | $V_{IN} = 0V, V_{CC} = 3.465V$ | -150           |     |                | $\mu A$ |
| $V_{PP}$    | Peak-to-Peak Input Voltage                  |                                | 0.3            |     | 1              | V       |
| $V_{CMR}$   | Common Mode Input Voltage <sup>(8, 9)</sup> |                                | $V_{EE} + 1.5$ |     | $V_{CC}$       | V       |
| $V_{OH}$    | Output High Voltage <sup>(10)</sup>         |                                | $V_{CC} - 1.4$ |     | $V_{CC} - 1.0$ | V       |
| $V_{OL}$    | Output Low Voltage <sup>(10)</sup>          |                                | $V_{CC} - 2.0$ |     | $V_{CC} - 1.7$ | V       |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing           |                                | 0.6            |     | 1.0            | V       |

### Notes:

7. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
8. Maximum input voltage for PCLK and /PCLK is  $V_{CC} + 0.3V$  for single ended applications.
9.  $V_{IH}$  is defined as the common mode voltage.
10.  $50\Omega$  to  $V_{CCO}-2V$  terminated outputs.

## AC Electrical Characteristics<sup>(11)</sup>

$V_{CC} = V_{CCO} = 3.3V \pm 5\%$ ;  $R_L = 50\Omega$  to  $V_{CCO}-2V$ ;  $T_A = 0^\circ C$  to  $+70^\circ C$ , unless otherwise stated.

| Symbol       | Parameter                                             | Condition                      | Min | Typ  | Max | Units             |
|--------------|-------------------------------------------------------|--------------------------------|-----|------|-----|-------------------|
| $f_{MAX}$    | Maximum Operating Frequency                           |                                | 500 |      |     | MHz               |
| $t_{PD}$     | Differential Propagation Delay<br>CLK-to-Q, PCLK-to-Q | $f \leq 250MHz$                | 1   |      | 2   | ns                |
| $t_{SKEW}$   | Output-to-Output Skew <sup>(12)</sup>                 |                                |     |      | 50  | ps                |
|              | Part-to-Part Skew <sup>(13)</sup>                     |                                |     |      | 250 | ps                |
| $t_{JITTER}$ | Additive Phase Jitter <sup>(14)</sup>                 | 155.52MHz,<br>(12KHz to 20MHz) |     | 0.17 |     | ps <sub>RMS</sub> |
| $t_r, t_f$   | Output Rise/Fall Time                                 | 20% to 80% @ 50MHz             | 300 |      | 700 | ps                |
| odc          | Output Duty Cycle                                     |                                | 48  | 50   | 52  | %                 |

### Notes:

11. High-frequency AC-parameters are guaranteed by design and characterization.
12. Output-to-Output skew is measured between two different outputs under identical transitions.
13. Part-to-Part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs. This parameter is defined in accordance with JEDEC Standard 65.
14. Driving only one input clock.

## Timing Diagrams

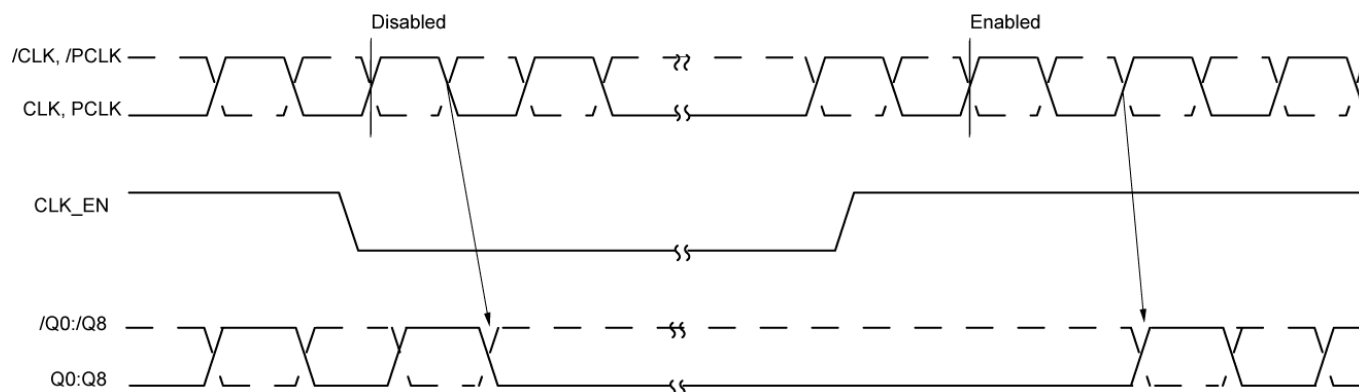


Figure 1a. CLK\_EN Timing Diagram

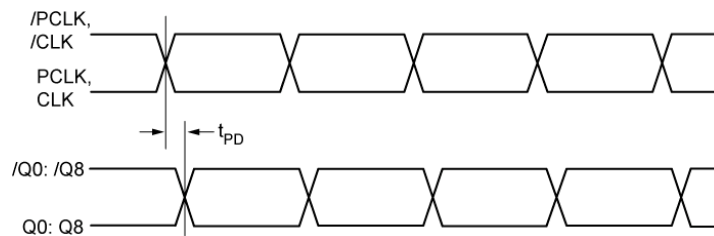


Figure 1b. Propagation Delay

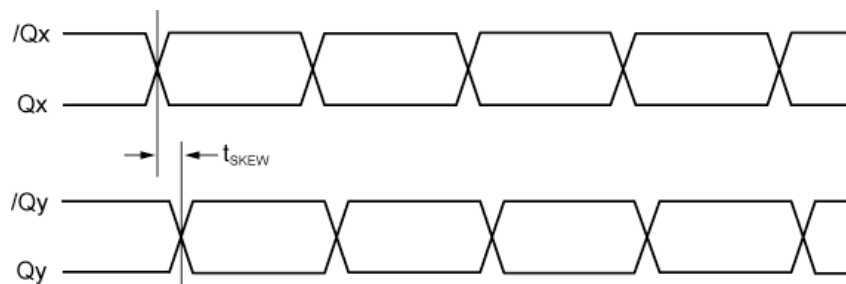
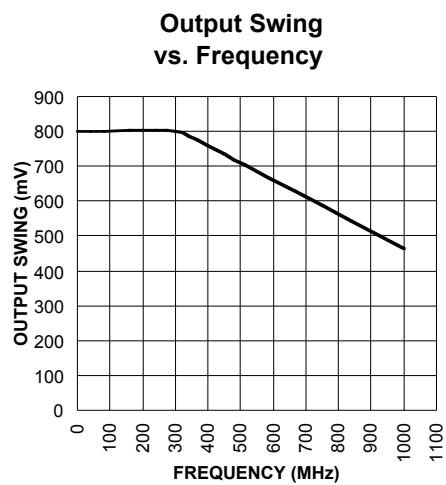


Figure 1c. Output-to-Output Skew

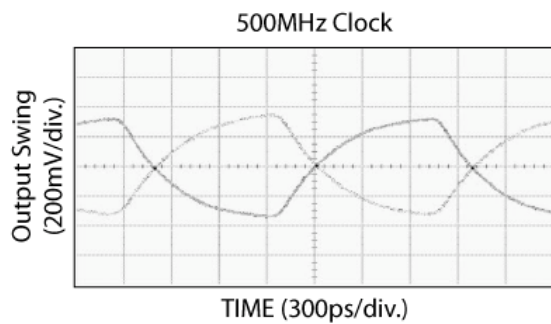
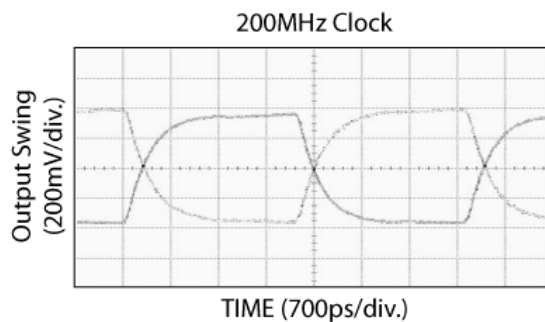
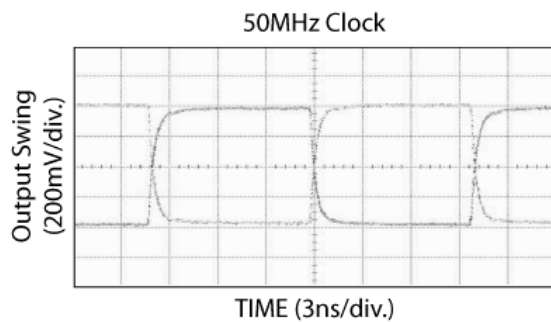
## Typical Operating Characteristics

$V_{CC} = 3.3V$ ,  $V_{EE} = 0V$ ,  $V_{IN} = 800mV$ ,  $R_L = 50\Omega$  to  $V_{CC}-2V$ ;  $T_A = 25^\circ C$ , unless otherwise stated.



## Functional Characteristics

$V_{CC} = 3.3V$ ,  $V_{EE} = 0V$ ,  $V_{IN} = 800mV$ ,  $R_L = 50\Omega$  to  $V_{CC}-2V$ ;  $T_A = 25^\circ C$ , unless otherwise stated



## CLK, /CLK Input Interface Applications

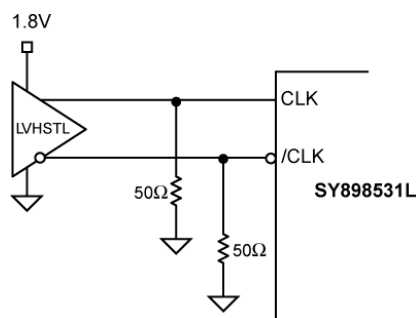


Figure 2a. LVHSTL Interface  
(DC-Coupled)

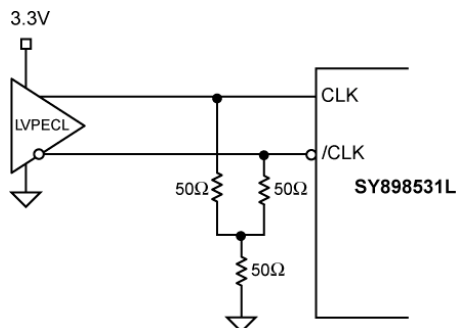


Figure 2b. LVPECL Interface  
(DC-Coupled)

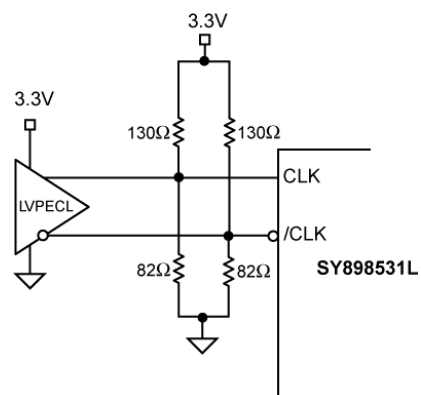


Figure 2c. LVPECL Interface  
(DC-Coupled)

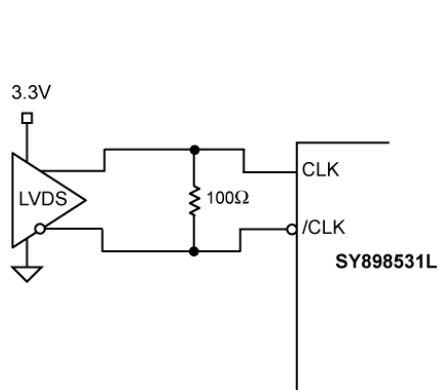


Figure 2d. LVDS Interface  
(DC-Coupled)

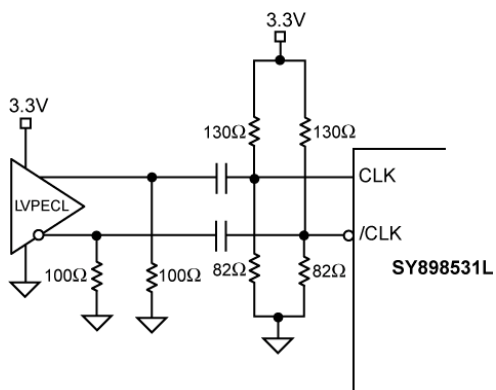


Figure 2e. LVPECL Interface  
(AC-Coupled)

## PCLK, /PCLK Input Interface Applications

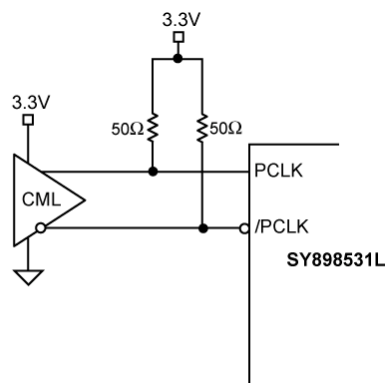


Figure 3a. CML Open Collector Interface (DC-Coupled)

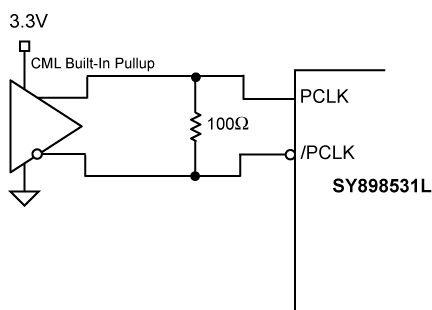


Figure 3b. CML Built-in Pull-up Interface (DC-Coupled)

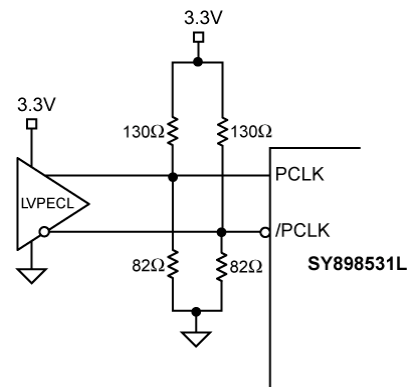


Figure 3c. LVPECL Interface (DC-Coupled)

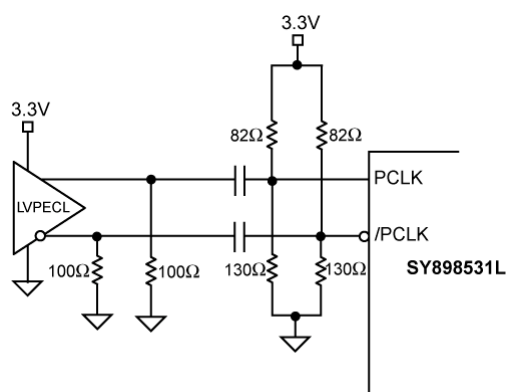


Figure 3d. LVPECL Interface (AC-Coupled)

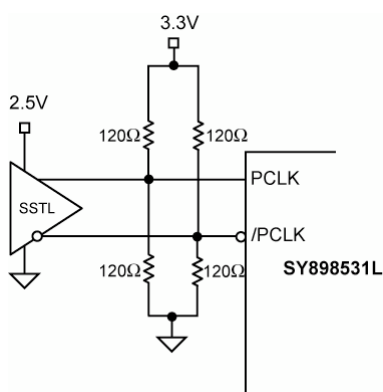


Figure 3e. SSTL Interface (DC-Coupled)

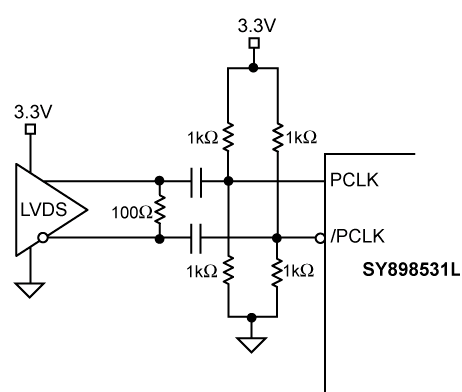
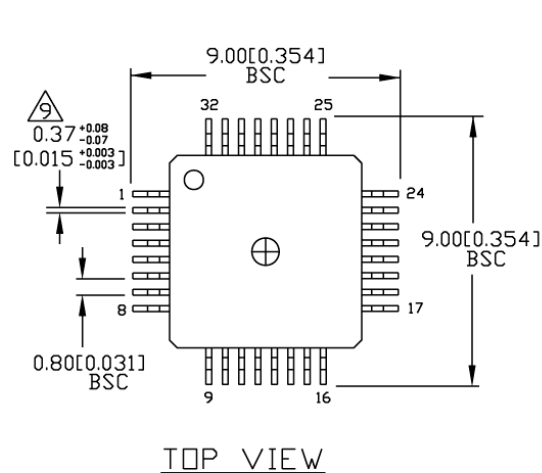
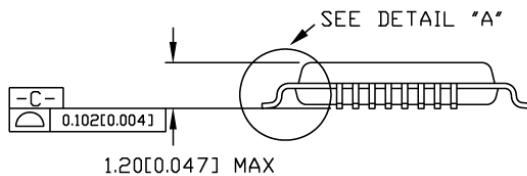


Figure 3f. LVDS Interface (AC-Coupled)

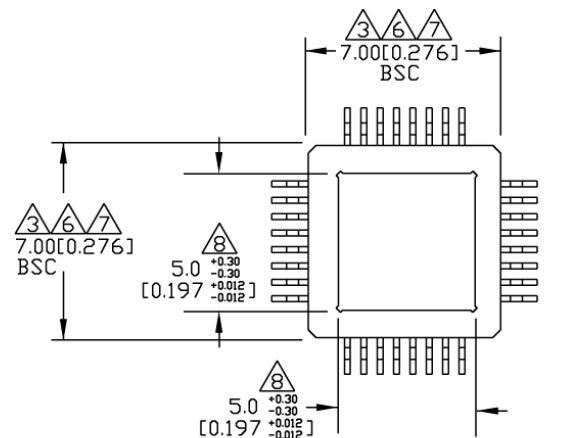
## Package Information



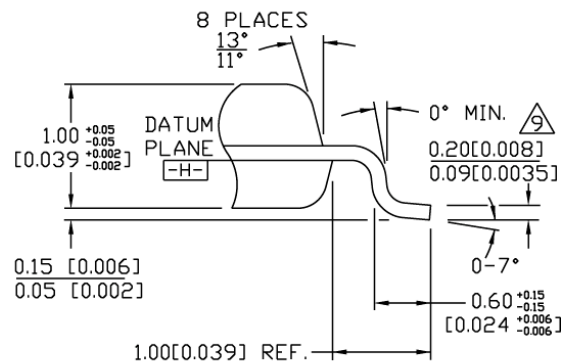
TOP VIEW



SIDE VIEW



BOTTOM VIEW



### NOTES:

1. DIMENSIONS ARE IN MM[INCHES].
2. CONTROLLING DIMENSION: MM.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.254 [0.010].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN.
6. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE [H].
7. PACKAGE TOP DIMENSIONS ARE SMALLER THAN BOTTOM DIMENSIONS AND TOP OF PACKAGE WILL NOT OVERHANG BOTTOM OF PACKAGE.
8. EXPOSED PAD SHALL BE COPLANAR WITH PACKAGE BOTTOM WITHIN 0.05mm
9. EXPOSED PAD: Cu WITH Sn/Pb PLATING
9. DIMENSION INCLUDES LEAD FINISH.

### 32-Pin TQFP (T32-1)

**MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA**

TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB <http://www.micrel.com>

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