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SZA-5044(Z)

4.9GHz to 5.9GHz 5V POWER AMPLIFIER

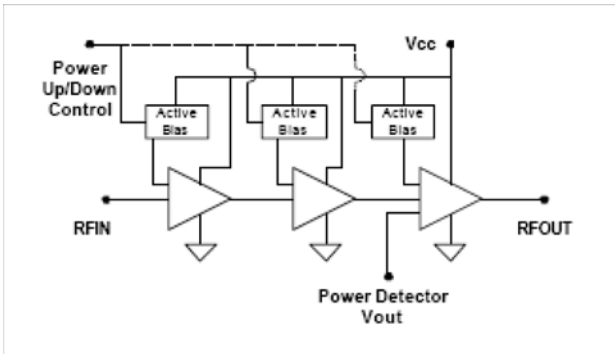
Package: QFN, 4mmx4mm

Product Description

RFMD's SZA-5044 is a high efficiency class AB Heterojunction Bipolar Transistor (HBT) amplifier housed in a low-cost surface-mountable plastic package. This HBT amplifier is made with InGaP on GaAs device technology and fabricated with MOCVD for an ideal combination of low cost and high reliability. This product is specifically designed as a final or driver stage for 802.11a equipment in the 4.9GHz to 5.9GHz band for a 5V supply. Optimized on-chip impedance matching circuitry provides a 50Ω nominal RF input impedance. A single external output matching circuit covers the entire 4.9GHz to 5.9GHz band simultaneously. The external output match allows for load line optimization for other applications or optimized performance over narrower bands. This product is available in a RoHS Compliant and Green package with matte tin finish, designated by the "Z" package suffix.

Optimum Technology Matching® Applied

- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☑ InGaP HBT
- ☐ SiGe BiCMOS
- ☐ Si BiCMOS
- ☐ SiGe HBT
- ☐ GaAs pHEMT
- ☐ Si CMOS
- ☐ Si BJT
- ☐ GaN HEMT
- ☐ RF MEMS



Features

- 802.11a 54Mb/s Class AB Performance P_{OUT}=22dBm at 3% EVM, 5V, 343mA
- High Gain=33dB
- Output Return Loss >11dB for Linear Tune
- On-Chip Output Power Detector
- P_{1dB}=30dBm at 5V
- Simultaneous 4.9GHz to 5.9GHz Performance
- Robust - Survives RF Input Power =+15dBm
- Power Up/Down Control <1ms, V_{PC} 2.9V to 5V

Applications

- 802.11a WLAN, OFDM
- 5.8GHz ISM Band, 802.16 WiMAX

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Frequency of Operation	4900		5900	MHz	
Output Power at 1dB Compression		30.2		dBm	5.15GHz
	27.5	29.0		dBm	5.875GHz
Gain	30.7	32.7	34.7	dB	4.9GHz
		33.0		dB	5.15GHz
	25.7	27.7	29.7	dB	5.875GHz
Output Power		21.0		dBm	3% EVM 802.11a 54Mb/s-5.15GHz
		22.0		dBm	3% EVM 802.11a 54Mb/s-5.875GHz
Noise Figure		6.3		dB	5.875GHz
Third Order Intermod		-39.0	-35.0	dBc	5.875GHz, 18dBm per tone
Worst Case Input Return Loss	8.6	11.6		dB	4.9GHz to 5.875GHz
Worst Case Output Return Loss	9.3	12.3		dB	4.9GHz to 5.875GHz
Output Voltage Range		0.8 to 1.9		V	P_{OUT}=10dBm to 26dBm
V_{CC} Quiescent Current	230	270	310	mA	
Power Up Control Current		1.7		mA	V_{PC}=5V (I_{VPC1}+I_{VPC2}+I_{VPC3})
Off V_{CC} Leakage Current		8	100	uA	V_{PC}=0V
Thermal Resistance (junction-lead		24		°C/W	junction - lead

Test Conditions: Z_O=50Ω, V_{CC}=5V, I_{CQ}=270mA, T_{BP}=25°C

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Absolute Maximum Ratings

Parameter	Rating	Unit
VC3 Collector Bias Current (pin 16)	500	mA
VC2 Collector Bias Current (pin 18)	225	mA
VC1 Collector Bias Current (pin 19)	75	mA
Device Voltage (V_D), No RF drive	7.0	V
Power Dissipation	3.4	W
Operating Lead Temperature (T_L)	-40to+85	°C
RF Input Power for 50Ω RF out load	15	dBm
RF Input Power for 10:1 VSWR RF out load	2	dBm
Storage Temperature Range	-40to+150	°C
Operating Junction Temperature (T_J)	150	°C
ESD Rating - Human Body Model (HBM)	>1000	V

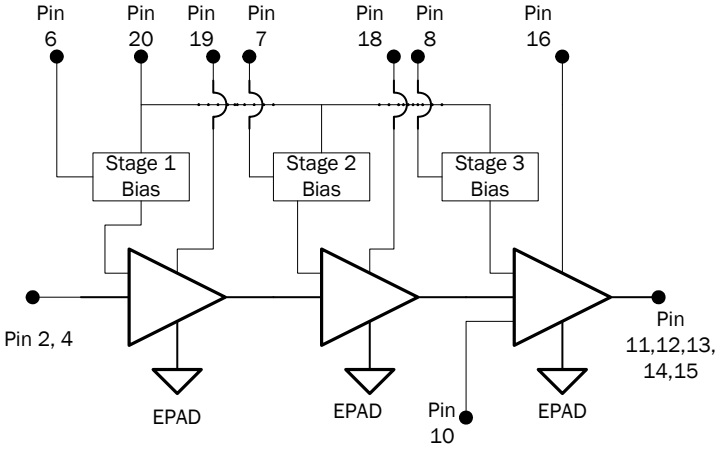
Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation, the device voltage and current must not exceed the maximum operating values specified in the table on page one.
Bias Conditions should also satisfy the following expression:
$I_D V_D < (T_J - T_L)/R_{TH}$, j-l

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

Simplified Device Schematic



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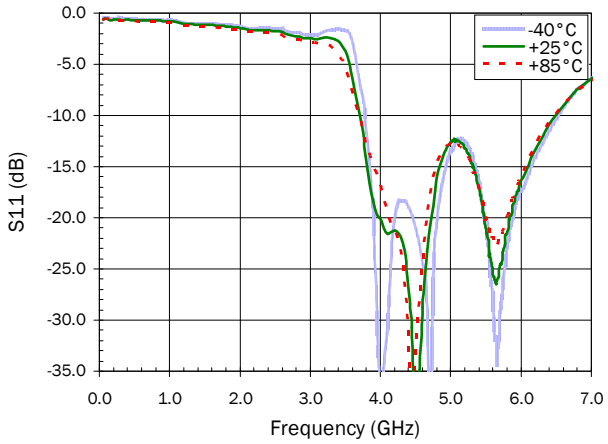
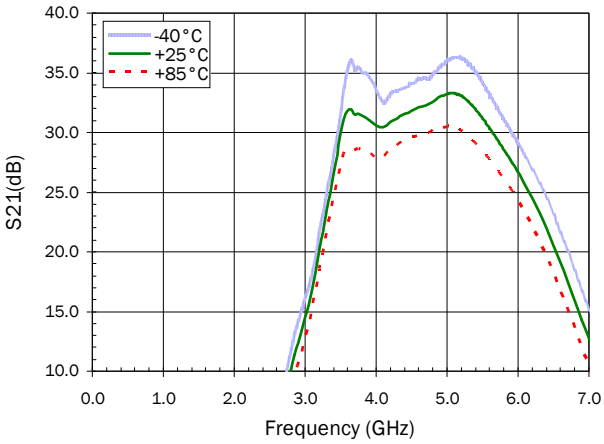
Pin	Function	Description
1, 3, 5, 9, 11, 15, 17	N/C	Pins are not used. May be grounded, left open, or connected to adjacent pin.
6	VPC1	VPC1 is the bias control pin for the stage 1 active bias circuit and can be run from 2.9V to 5V control. An external series resistor is required for proper setting of bias levels depending on control voltage. Refer to the evaluation board schematic for resistor value. To prevent potential damage, do not apply voltage to this pin that is +1V greater than voltage applied to pin 20 (Vbias) unless Vpc supply current capability is less than 10mA.
7	VPC2	VPC2 is the bias control pin for the stage 2 active bias circuit and can be run from 2.9V to 5V control. An external series resistor is required for proper setting of bias levels depending on control voltage. Refer to the evaluation board schematic for resistor value. To prevent potential damage, do not apply voltage to this pin that is +1V greater than voltage applied to pin 20 (Vbias) unless Vpc supply current capability is less than 10 mA.
8	VPC3	VPC3 is the bias control pin for the stage 3 active bias circuit and can be run from 2.9V to 5V control. An external series resistor is required for proper setting of bias levels depending on control voltage. Refer to the evaluation board schematic for resistor value. To prevent potential damage, do not apply voltage to this pin that is +1V greater than voltage applied to pin 20 (Vbias) unless Vpc supply current capability is less than 10mA.
10	VDET	Output power detector voltage. Load with 10K to 100K Ω to ground for best performance.
2, 4	RF IN	RF input pins. This is DC grounded internal to the IC. Do not apply voltage to this pin. All three pins must be used for proper operation.
12, 13, 14	RF OUT	RF output pin. This is also another connection to the 3rd stage collector
16	VC3	3rd stage collector bias pin. Apply 5V to this pin.
18	VC2	2nd stage collector bias pin. Apply 5V to this pin.
19	VC1	1st stage collector bias pin. Apply 5V to this pin.
20	VBIAS	Active bias network VCC. Apply 5V to this pin.
EPAD	GND	Exposed area on the bottom side of the package needs to be soldered to the ground plane of the board for optimum thermal and RF performance. Several vias should be located under the EPAD as shown in the recommended land pattern (page 5).

4.9GHz to 5.9GHz Evaluation Board Data (V_{BIAS}=5.0V, I_Q=270mA)

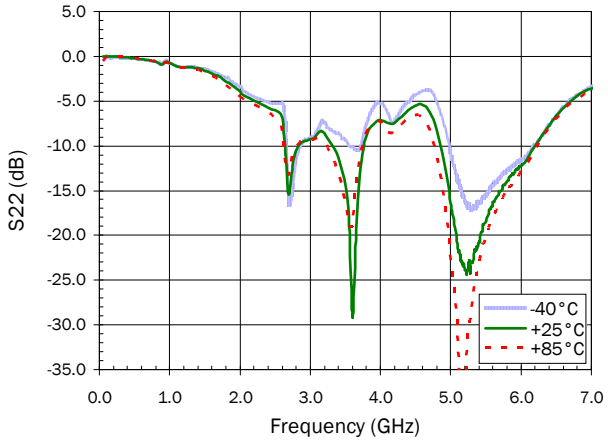
Broadband S11 - Input Return Loss



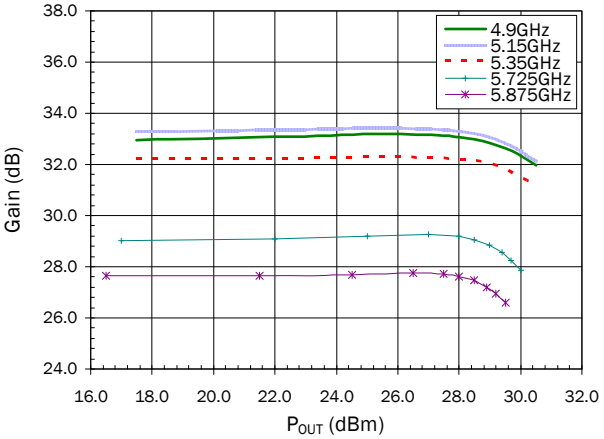
Broadband S21 - Forward Gain



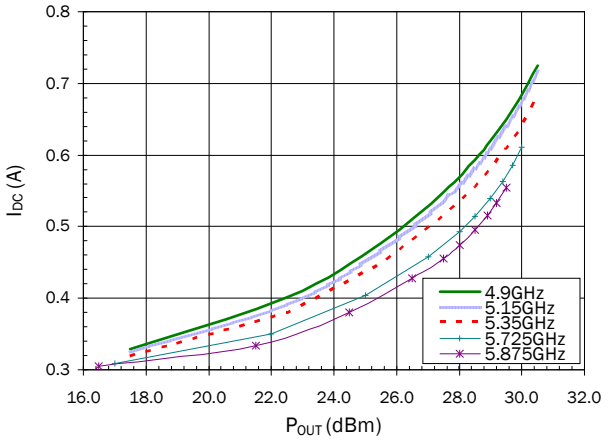
Broadband S22 - Output Return Loss



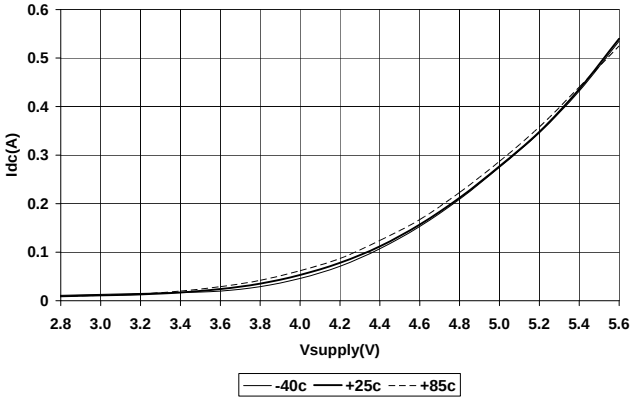
Typical Gain versus P_{OUT}, T=+25°C



DC Supply Current versus P_{OUT}, T=+25°C



Icq (DC bias point) vs Vsupply (V+ and Vpc)



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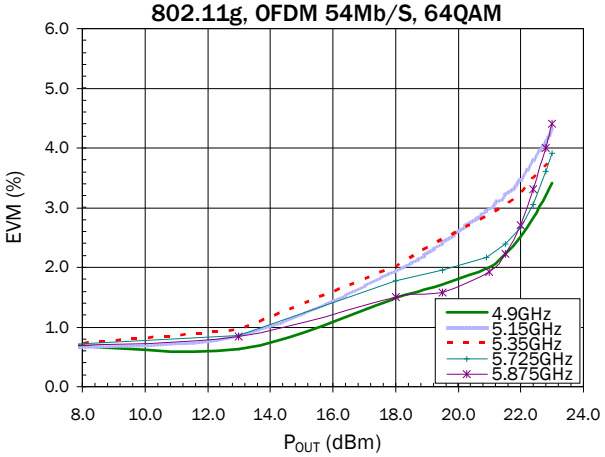
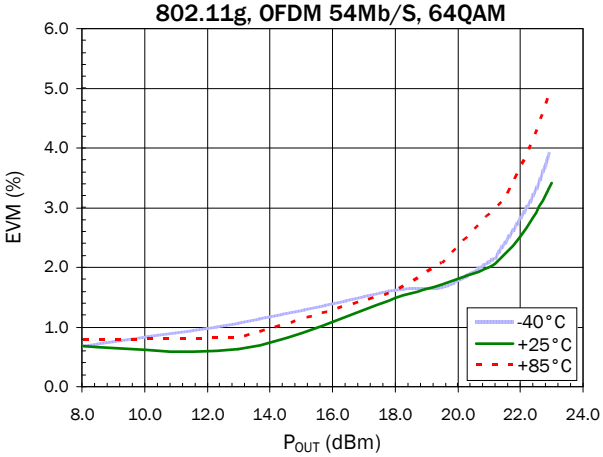
4.9GHz to 5.9GHz Evaluation Board Data (V_{BIAS}=5.0V, I_Q=270mA)
802.11a EVM, OFDM, 54Mb/s, 64QAM

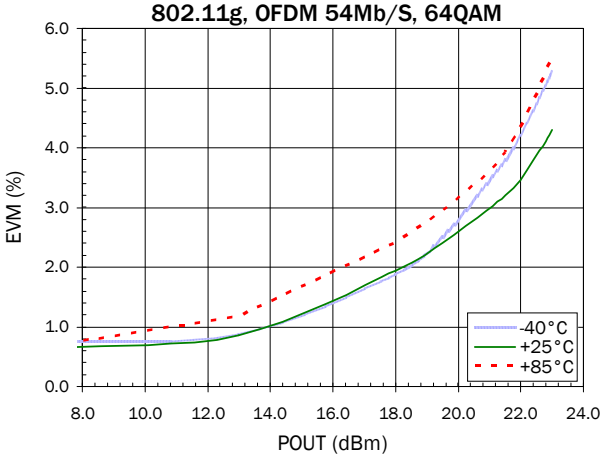
EVM versus P_{OUT}, +25°C
802.11g, OFDM 54Mb/S, 64QAM



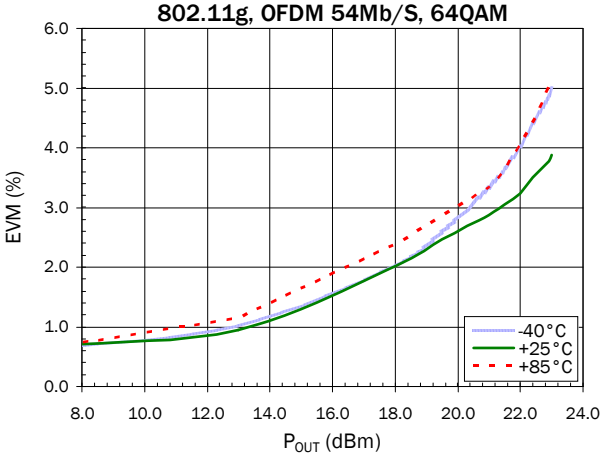
EVM versus P_{OUT}, F=4.9GHz
802.11g, OFDM 54Mb/S, 64QAM



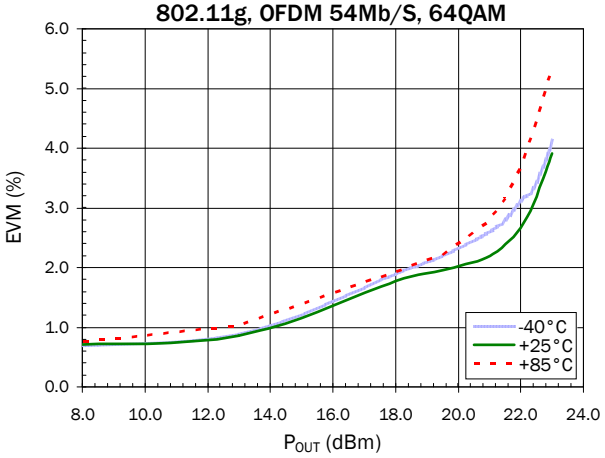
EVM versus P_{OUT}, F=5.15GHz
802.11g, OFDM 54Mb/S, 64QAM



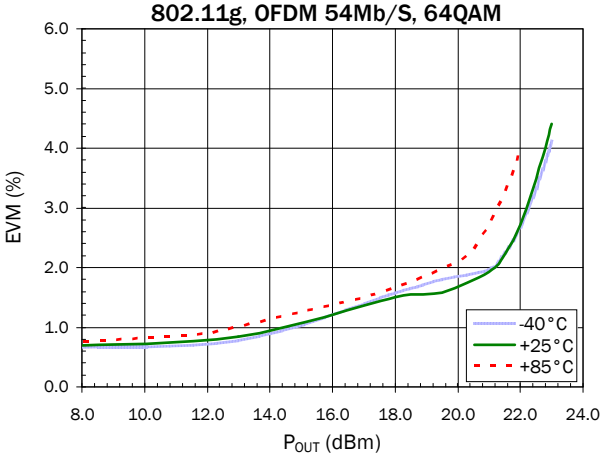
EVM versus P_{OUT}, F=5.35GHz
802.11g, OFDM 54Mb/S, 64QAM



EVM versus P_{OUT}, F=5.725GHz
802.11g, OFDM 54Mb/S, 64QAM

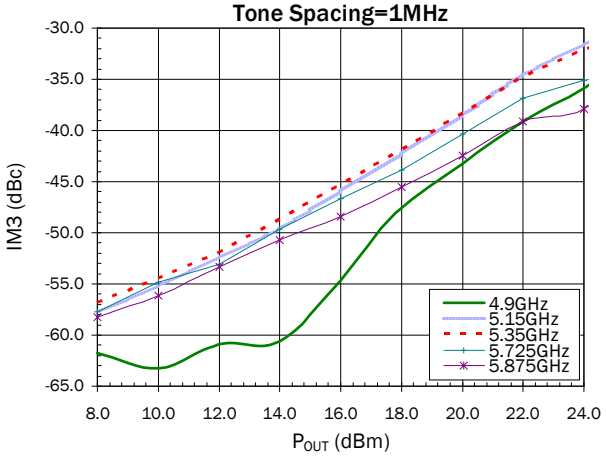


EVM versus P_{OUT}, F=5.875GHz
802.11g, OFDM 54Mb/S, 64QAM

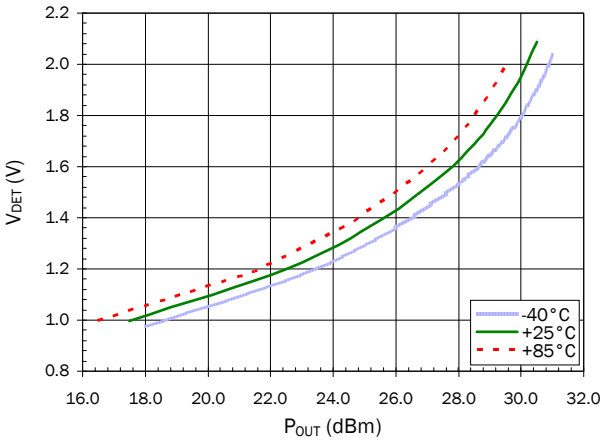


4.9GHz to 5.9GHz Evaluation Board Data (V_{BIAS}=5.0V, I_Q=270mA)

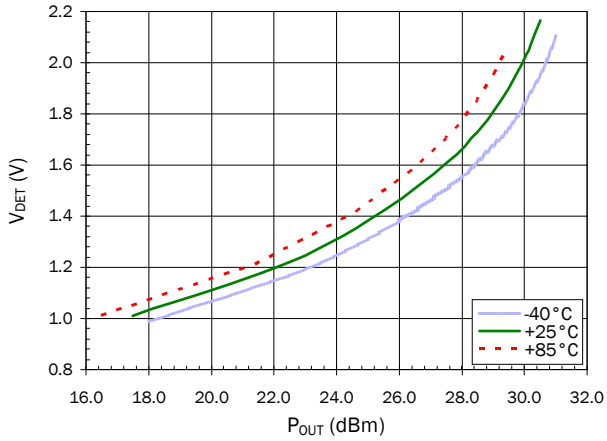
IM3 versus P_{OUT} (2 Tone Avg.), T=25°C
Tone Spacing=1MHz



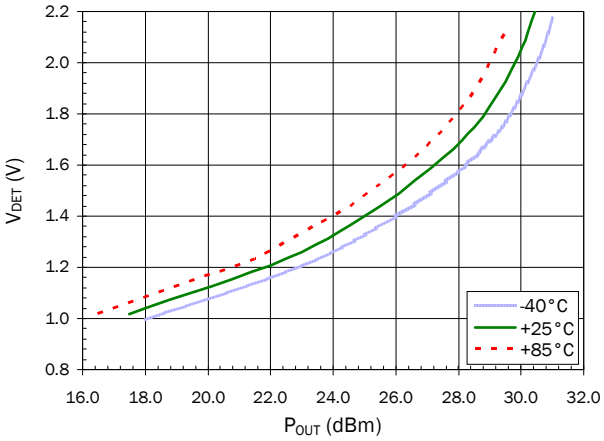
RF Power Detector (V_{DET}) versus P_{OUT}, F=4.9GHz



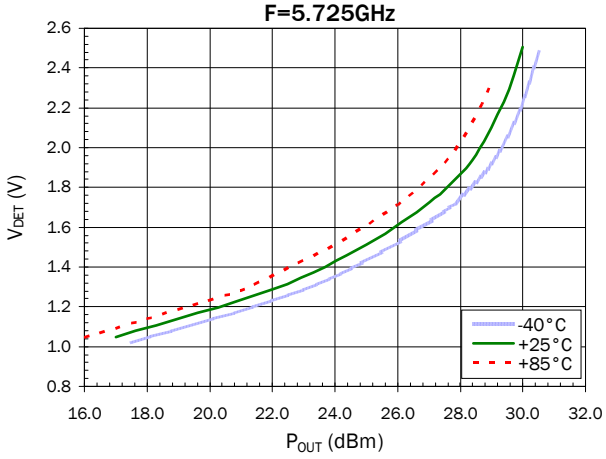
RF Power Detector (V_{DET}) versus P_{OUT}, F=5.15GHz



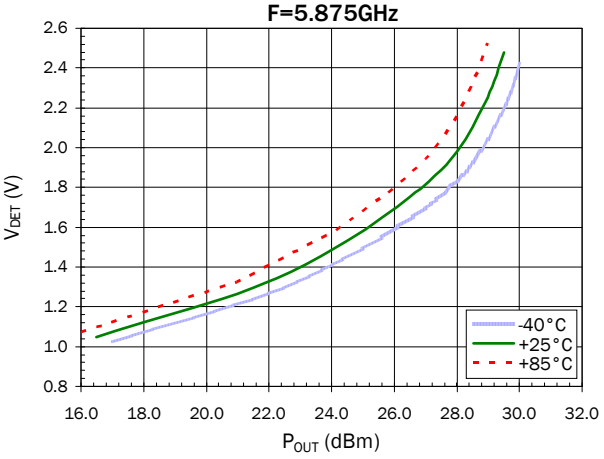
RF Power Detector (V_{DET}) versus P_{OUT}, F=5.35GHz



RF Power Detector (V_{DET}) versus P_{OUT},
F=5.725GHz



RF Power Detector (V_{DET}) versus P_{OUT},
F=5.875GHz



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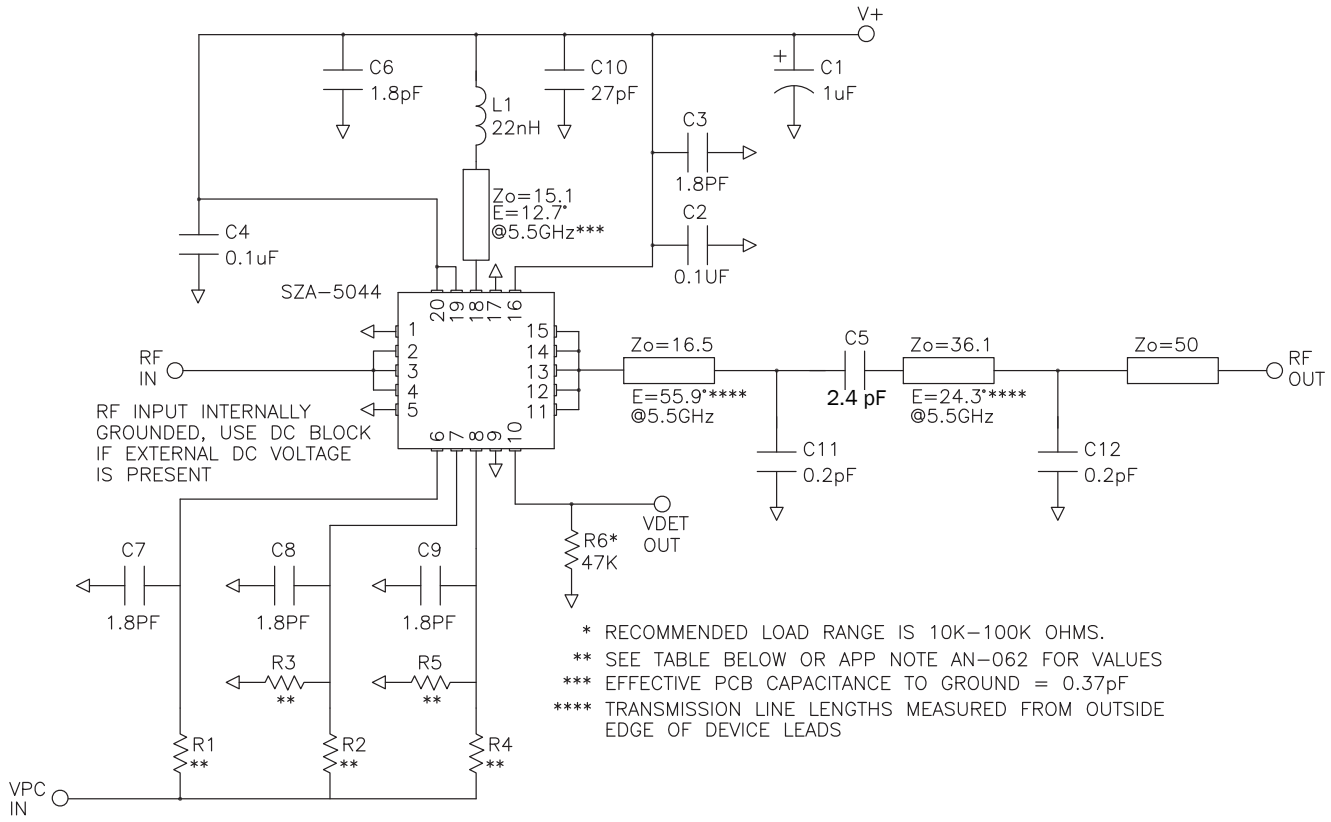
Evaluation Board Schematic for V+=V_{CC}=5.0V

(4.9GHz to 5.9GHz)



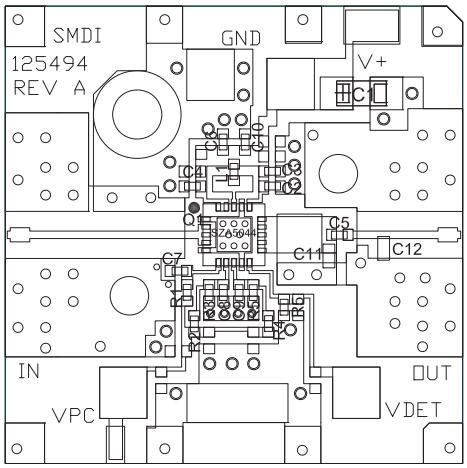
Notes: Pins 1, 3, 5, 9, 11, 15, and 17 are unwired (N/C) inside the package. Refer to page 2 for detailed pin descriptions. Some of these pins are wired to adjacent pins or grounded as shown in the application circuit. This is to maintain consistence with the evaluation board layout shown below. It is recommended to use this layout and wiring to achieve the specified performance.

To prevent potential damage, do not apply voltage to the V_{PC} pin that is +1V greater than voltage applied to pin 20 (V_{BIAS}/V_{CC}) unless V_{PC} supply current capability is less than 10mA.

Evaluation Board Layout for $V+=V_{CC}=5.0V$

(4.9GHz to 5.9GHz)

Board material GETEK, 10mil thick, Dk=3.9, 2oz. copper finish



PCB notes: Do not use less than recommended ground via holes.

RF Layers thicker than.020 inches (0.5mm) not recommended.

DESG	Description
Q1	SZA-5044
R1, 2, 3, 4, 5, 6	1%, 0402
C1	IuF 15V TANTALUM CAP
C2, 4	0.1uF CAP, 0402
C3, 6, 7, 8, 9	1.8pF Cap, 0402
C5	2.4pF Cap, 0402
C10	27pF Cap, 0402
L1	22nH IND, 0402
C11, 12	0.2pF Cap, 0603

Resistor values for $V_{PC}=2.9V$ to 5V ($V_{CC}=5V$, $I_Q=270mA$)

VPC(V)	R1	R2	R4	R3	R5
2.9	0	698	10	OUT	OUT
3.0	174	1.1K	281	OUT	OUT
3.1	348	1.37K	499	OUT	OUT
3.2	511	1.78K	750	OUT	OUt
3.3	698	2.15K	1.00K	OUT	OUT
5.0	3.6K	2.2K	2.4K	7.5K	7.5K

Note: See app note for V_{CC} and V_{PC} combinations

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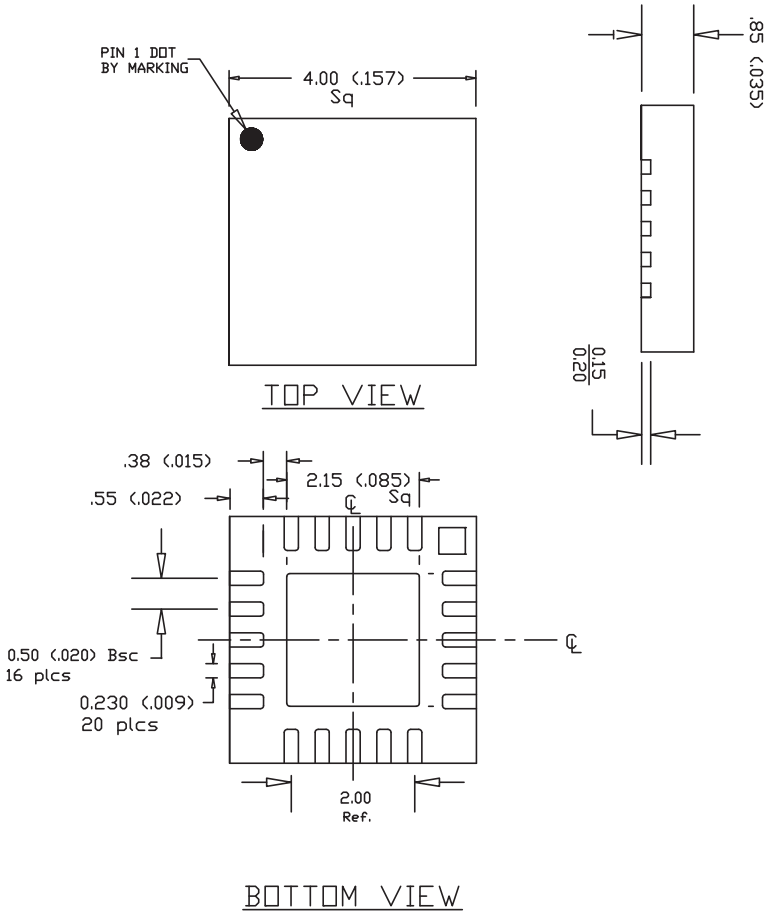
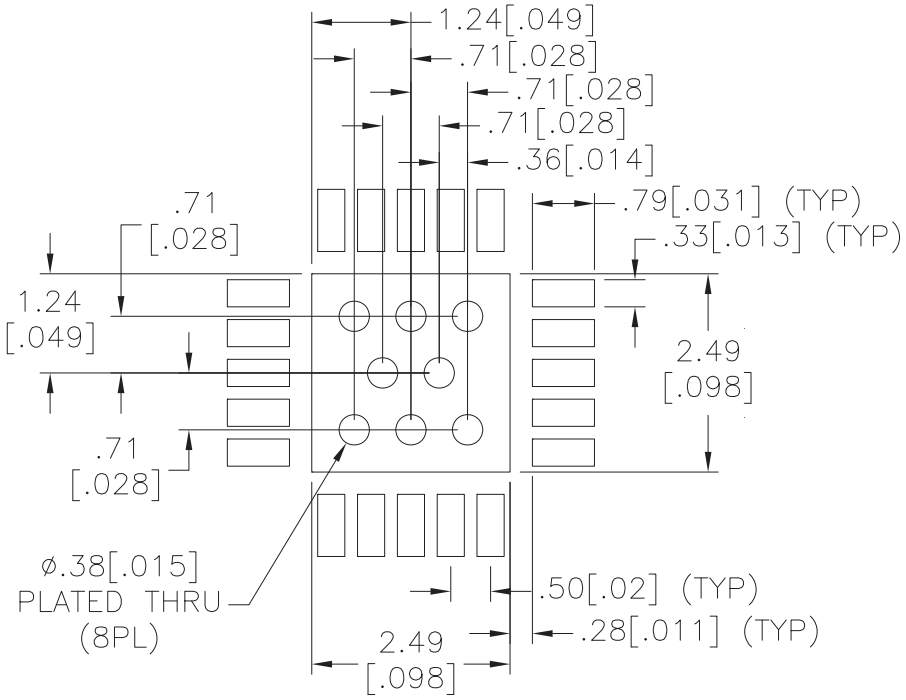
Package Drawing

Dimensions in millimeters (inches)



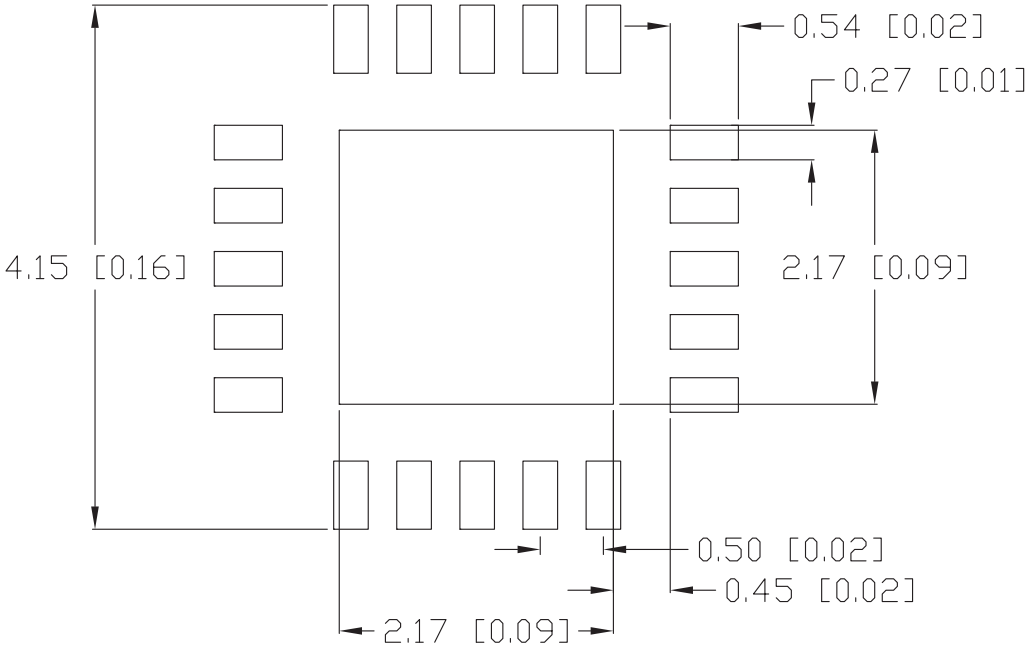
Recommended Land Pattern

Dimensions in millimeters (inches)



Recommended PCB Soldermask (SMBOC) for Land Pattern

Dimensions in millimeters (inches)



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Part Symbolization

The part will be symbolized with an "SZA-5044" for Sn/Pb plating or "SZA-5044Z" for RoHS green compliant product. Marking designator will be on the top surface of the package.

Ordering Information

Part Number	Description	Reel Size	Devices/Reel
SZA5044(Z)	Lead Free, RoHS Compliant	13"	3000
SZA5044(Z)-EVB1	4.9GHz to 5.9GHz Evaluation Board	N/A	N/A

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