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QorIQ T4 Processor Family

QorIQ T4240, T4160 and T4080 Advanced Multicore Processors

Multi-threaded SoCs deliver high performance per watt

Overview

The QorIQ T4 family is the flagship of the QorIQ T series. Advanced 28 nm process technology, integration, new higher speed IO, clustered memory subsystems, hardware acceleration and power management give the T4 family a very high performance profile in an embedded power envelope. The T4240 advanced multicore processor features 12 physical and 24 virtual high performance cores scaling up to 1.8 GHz.The T4 family is joined by the T4160 (16 virtual cores) and T4080 (eight virtual cores) processors, and the family has a 3x performance scaling factor within a pin compatible package. The T4 family features sophisticated support for hardware and software virtualization solutions.

Target Markets and Applications

The T4 family is ideal for combined control and data plane processing. A wide variety of applications can benefit from the processing, I/O integration and power management offered by this processor. Like other QorIQ devices, the T4 family of processors' high level of integration offers significant space, weight and power benefits compared to multiple discrete devices.

- Service provider networking: RNC, metro networking, gateway, core/edge router, EPC, CRAN, ATCA and AMC solutions
- Enterprise equipment: Router, switch services, UTM
- Data centers: NFV, SDN, ADC, WOC, UTM, proxy, server appliance, PCI Express® (PCIe) offload
- Storage controllers: FCoE bridging, iSCSI controller, SAN controller
- Aeronautics, defense and government: Radar imaging, ruggedized network appliance, cockpit display
- Industrial computing: Single-board computers, test equipment

Advanced Cores

The T4 family of processors are based on the new Power Architecture® e6500 core. The e6500 uses a 64-bit seven-stage pipeline for low latency response to unpredictable code execution paths, boosting single-threaded performance. The e6500 also offers higher aggregate instructions per clock at lower power with an innovative "fused core" approach to threading. The e6500 core's fully resourced dual threads provide 1.7 times the performance of a single thread.

Features of Distinction

	T4080	T4160	T4240
Cores (Dual Threaded)	4	8	12
L2 Cache	2 MB	4 MB	6 MB
CoreNet Platform Cache	1 MB	1 MB	1.5 MB
DDR Controllers	2	2	3
SerDes Lanes	24	24	36
Max 10 Gbps Ethernet	2	2	4
Max 1 Gbps Ethernet	13	13	16
PCIe Controllers	3	3	4

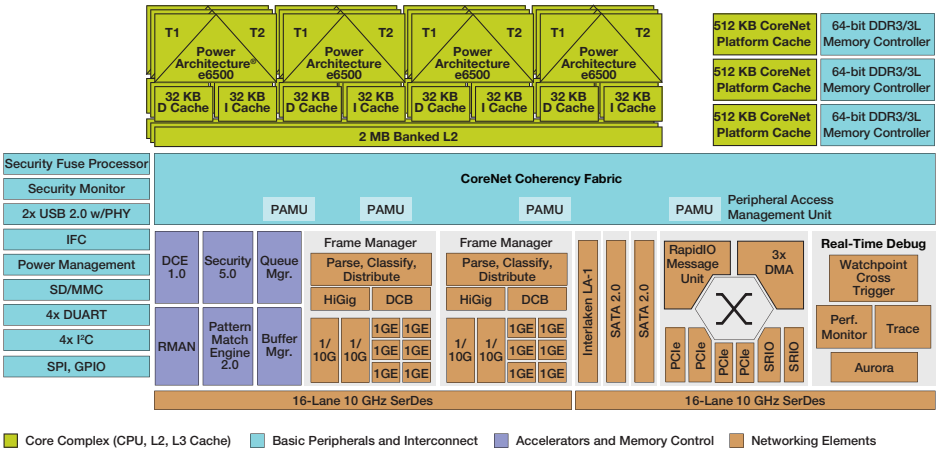
The e6500 cores are clustered in banks of four cores sharing a 2 MB L2 cache, allowing efficient sharing of code and data within a multicore cluster. Each e6500 core implements the Freescale AltiVec technology SIMD engine, dramatically boosting the performance of heavy math algorithms with DSP-like performance. The e6500 core features include:

- Up to 1.8 GHz dual threaded operation
- 7 DMIPS/MHz per core
- Advanced power saving modes, including state retention power gating

Virtualization

The T4 family of processors include support for hardware-assisted virtualization. The e6500 core offers an extra core privilege level (hypervisor) and hardware offload of logical to real address translation. In addition, the T4 family of processors include platform-level enhancements supporting I/O virtualization with DMA memory protection through IOMMUs and configurable "storage profiles" that provide isolation of I/O buffers between guest environments. Virtualization software for the T4 family includes kernel virtualization machine (KVM), Linux® containers, Freescale hypervisor and commercial virtualization software from Enea®, Greenhills Software®, Mentor Graphics® and Wind River.

QorIQ T4240 Communications Processor



T4240 Features List

Dual-threaded e6500 cores built on Power Architecture® technology	• Arranged in clusters of four e6500s sharing a 2 MB L2 cache • 12 dual threaded cores on T4240, 8 on T4160, and 4 on T4080 • Up to 1.8 GHz with 64-bit ISA support (Power Architecture v2.06-compliant) • AltiVec technology SIMD engine • User, supervisor and hypervisor instruction levels
CoreNet platform cache	• 1.5 MB configured as triple 512 KB blocks (1 MB on T4160 and T4080 processors)
Hierarchical interconnect fabric	• CoreNet fabric supporting coherent and non-coherent transactions with prioritization and bandwidth allocation amongst CoreNet endpoints • 1.6 Tb/s coherent read bandwidth • QMAN fabric supporting packet-level queue management and quality of service scheduling
64-bit DDR3/3L SDRAM memory controllers	• Up to 1866 MT/s • Three controllers on T4240 processor (two on T4160 and T4080 processors) • ECC and interleaving support
DPAA incorporates acceleration for the following functions	• Packet parsing, classification and distribution (FMAN 1.1) • Queue management for scheduling, packet sequencing and congestion management (QMAN 1.1) • Hardware buffer management for buffer allocation and de-allocation (BMAN 1.1) • Cryptography acceleration (SEC 5.0) at up to 40 Gb/s • RegEx pattern matching acceleration (PME 2.0) at up to 10 Gb/s • Decompression/compression acceleration (DCE 1.0) at up to 20 Gb/s • DPAA chip-to-chip interconnect via RapidIO message manager (RMAN 1.0)
SerDes	• 32 lanes total at up to 10 GHz (24 lanes on T4160 and T4080 processors) • Supports SGMII, QSGMII, HiGig, XAUI, XFI, 10Gbase-KR, PCIe rev 1.1/2.0/3.0, Interlaken-LA, sRIO
Ethernet interfaces	• Up to four 10 GE Ethernet MACs (two on T4160 and T4080 processors) • Up to 16 1 GE Ethernet MACs (13 on T4160 and T4080 processors) • Maximum configuration of 4 x 10 GE + 12 x 1 GE (2x 10 GE + 10x 1GE on T4160 and T4080 processors)
High-speed peripheral interfaces	• Four PCI Express 2.0/3.0 controllers (three on T4160 and T4080 processors) • Endpoint SR-IOV with 2 PFs (Physical Functions) and 128 VFs (Virtual Functions) • Two serial RapidIO 2.0 controllers/ports running at up to 5 GHz with Type 11 messaging and Type 9 data streaming support • Interlaken look-aside interface for serial TCAM connection
Additional peripheral interfaces	• Two serial ATA (SATA 2.0) controllers • Two High-Speed USB 2.0 controllers with integrated PHY • Enhanced secure digital host controller (SD/MMC/eMMC) • Enhanced serial peripheral interface • Four I^2C controllers • Four UARTs • Integrated flash controller supporting NAND and NOR flash
DMA	• Three eight-channel DMA controllers
Support for hardware virtualization and partitioning enforcement	• Extra privilege level for hypervisor support • Logical to real address translation • Virtual core aware MMU/TLB • vMPIC (virtualized interrupt controller)/virtual core capable PPC cores • vDMA (user-level DMA engine) • PAMUv2 (I/O MMU supporting paging) • DPAA (Ethernet MAC virtualization, accelerator virtualization)
QorIQ trust architecture 2.0	• Secure boot, secure debug, tamper detection, volatile key storage, alternate image and key revocation

DPAA Hardware Accelerators

Frame manager (FMAN)	50 Gb/s classify, parse and distribute
Buffer manager (BMAN)	64 buffer pools
Queue manager (QMAN)	Up to 2^{24} queues
RapidIO manager (RMAN)	Seamless mapping to DPAA
Security (SEC)	40 Gb/s: 3 DES, AES; 20 Gb/s: Kasumi/F8
Pattern matching engine (PME)	10 Gb/s
Data compression engine (DCE)	20 Gb/s aggregate

Data Path Acceleration Architecture (DPAA)

The T4 family of processors enhance the QorIQ DPAA, an innovative multicore infrastructure for scheduling work to cores (physical and virtual), hardware accelerators and network interfaces. The FMAN, a primary element of the DPAA, parses headers from incoming packets and classifies and selects data buffers with optional policing and congestion management. The FMAN passes its work to the QMAN, which assigns it to cores or accelerators with a multilevel scheduling hierarchy. The T4240 processor's implementation of the DPAA offers accelerators for cryptography, enhanced regular expression pattern matching and compression/decompression.

System Peripherals and Networking

For networking, there are dual FMANs with an aggregate of up to 16 any-speed MAC controllers that connect to PHYs, switches and backplanes over RGMII, SGMII, QSGMII, HiGig2, XAUI, XFI and 10Gbase-KR. The FMAN also supports new quality of service features through egress traffic shaping and priority flow control for data center bridging in converged data center networking applications. High-speed system expansion is supported through four PCI Express controllers that support varieties of lane lengths for PCIe specification 3.0, including endpoint SR-IOV with 128 virtual functions. Other peripheral interfaces include SRIO, Interlaken-LA, SATA, SD/MMC, I^2C, UART, SPI, a NOR/NAND controller, GPIO and a 1866 MT/s DDR3L controller.

Software and Tool Support

- Enea®: Real-time operating system support and virtualization software
- Green Hills®: Comprehensive portfolio of software and hardware development tools, trace tools, RTOS and virtualization software
- Mentor Graphics®: Commercial-grade Linux® solution and Vista simulation model which allows for a TLM2 simulation environment, software development and power estimation. Mentor Embedded Performance Library is a High Performance Computing (HPC) library of advanced math and signal processing functions for AltiVec technology.
- Wind River: Development tools, RTOS, Linux and virtualization software

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For more information visit freescale.com/QorIQ

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