TelCom Semiconductor, Inc.

TC14433
TC14433A

3-1/2 DIGIT A/D CONVERTERS

FEATURES

- Accuracy .....±0.05% of Reading ±1 Count
- Two Voltage Ranges .....1.999V and 199.9 mV
- Up to 25 Conversions Per Second
- Z_{IN} > 1000M Ohms
- Single Positive Voltage Reference
- Auto-Polarity and Auto-Zero
- Overrange and Underrange Signals Available
- Operates in Auto-Ranging Circuits
- Uses On-Chip System Clock or External Clock
- Wide Supply Range ..... e.g., ±4.5V to ±8V
- Package Available ..... 24-Pin DIP
  24-Pin CerDIP, 28-Pin SOIC and 28-Pin PLCC

APPLICATIONS

- Portable Instruments
- Digital Voltmeters
- Digital Panel Meters
- Digital Scales
- Digital Thermometers
- Remote A/D Sensing Systems
- MPU Systems
- See Application Notes 19 and 21

GENERAL DESCRIPTION

The TC14433 is a low power, high-performance, monolithic CMOS 3-1/2 digit A/D converter. The TC14433 combines both analog and digital circuits on a single IC, thus minimizing the number of external components. This dual-slope A/D converter provides automatic polarity and zero correction with the addition of two external resistors and two capacitors. The full-scale voltage range of this ratiometric IC extends from 199.9 millivolts to 1.999 volts. The TC14433 can operate over a wide range of power supply voltages, including batteries and standard 5-volt supplies.

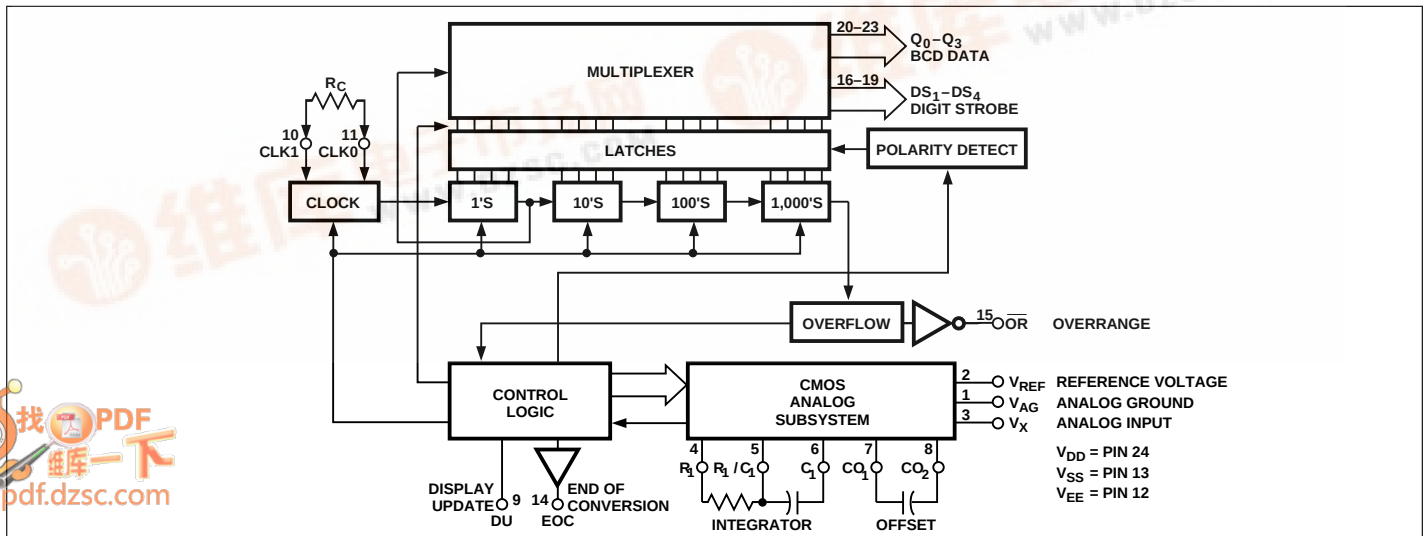
The TC14433 will interface with the TC7211A LCD display driver.

The TC14433A features improved performance over the industry standard TC14433. Rollover, which is the measurement of identical positive and negative signals, is guaranteed to have the same reading within one count for the TC14433A. Power consumption of the TC14433A is typically 4 mW, approximately one-half that of the industry standard TC14433.

ORDERING INFORMATION

Part No.	Package	Temp.Range
TC14433AEJG	24-Pin CerDIP	– 40°C to +85°C
TC14433AELI	28-Pin PLCC	– 40°C to +85°C
TC14433AEPG	24-Pin Plastic DIP	– 40°C to +85°C
TC14433COG	24-Pin SOIC	0°C to +70°C
TC14433EJG	24-Pin CerDIP	– 40°C to +85°C
TC14433ELI	28-Pin PLCC	– 40°C to +85°C
TC14433EPG	24-Pin Plastic DIP	– 40°C to +85°C

FUNCTIONAL BLOCK DIAGRAM



TC14433
TC14433A

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage ($V_{DD} - V_{EE}$) ..... – 0.5V to +18V
Voltage on Any Pin,
Reference to V_{EE} ..... – 0.5V to (V_{DD} + 0.5)
DC Current, Any Pin ..... ±10mA
Operating Temperature Range ..... – 40°C to +85°C
Power Dissipation ($T_A \leq 70°C$)
Plastic PLCC 1.0W
Plastic DIP 940mW
SOIC 940mW
CerDIP 1.45W
Storage Temperature Range ..... – 65°C to +160°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

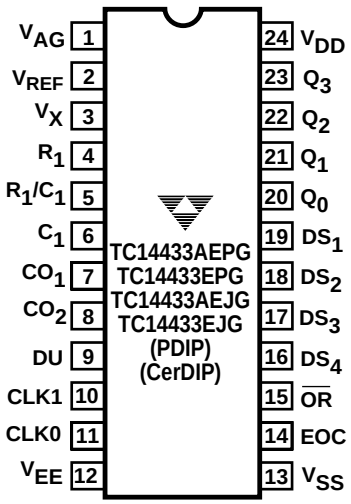
ELECTRICAL CHARACTERISTICS:

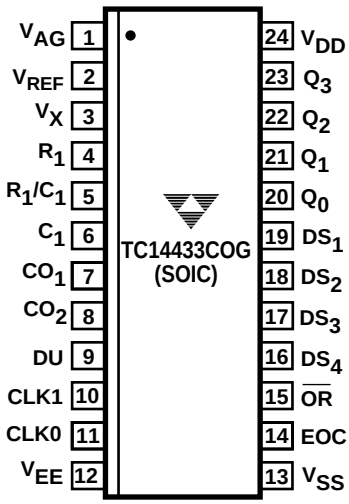
V_{DD} = +5V, V_{EE} = – 5V, C_1 = 0.1µF (mylar), C_O = 0.1µF, R_C = 300kΩ, R_1 = 470kΩ @ V_{REF} = 2V, R_1 = 27kΩ @ V_{REF} = 200mV, unless otherwise specified.

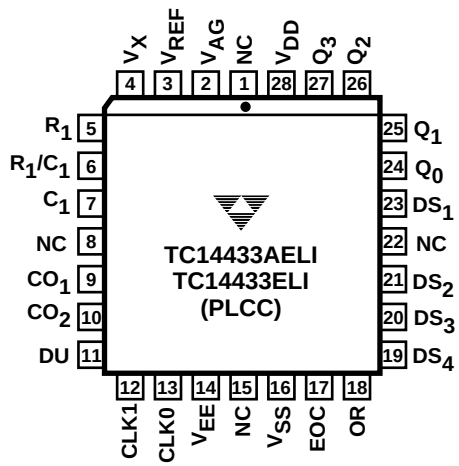
			T_A = +25°C			– 40°C < T_A < +85°C			
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Analog Input									
SYE	Rollover Error (Positive and Negative Full Scale Symmetry	200mV Full Scale V_{IN} $-V_{IN} = +V_{IN}$	–1	—	+1	—	—	—	Counts
NL	Linearity Output Reading (Note 1)	V_{REF} = 2V V_{REF} = 200mV	– 0.05 – 1 count	+0.05 —	+0.05 +1 count	— —	— —	— —	%rdg
SOR	Stability Output Reading (Note 2)	V_X = 1.99V, V_{REF} = 2V V_X = 199mV, V_{REF} = 200mV	— —	— —	2 3	— —	— —	— —	LSD
ZOR	Zero Output Reading	V_X = 0V, V_{REF} = 2V	—	0	0	—	—	—	LSD
I_{IN}	Bias Current: Analog Input Reference Input Analog Ground		 — — —	 ±20 ±20 ±20	 ±100 ±100 ±500	 — — —	 — — —	 — — —	pA
CMRR	Common-Mode Rejection	V_X = 1.4V, V_{REF} = 2V, f_{OC} = 32kHz	—	65	—	—	—	—	dB
Digital									
V_{OL}	Output Voltage Pins 14 to 23 (Note 3)	V_{SS} = 0V, "0" Level V_{SS} = – 5V, "0" Level	— —	0 – 5	0.05 –4.95	— —	— —	0.05 – 4.95	V
V_{OH}	Output Voltage Pins 14 to 23 (Note 3)	V_{SS} = 0V, "1" Level V_{SS} = – 5V, "1" Level	4.95 4.95	5 5	— —	4.95 4.95	— —	— —	V
I_{OH}	Output Current Pins 14 to 23	V_{SS} = 0V, V_{OH} = 4.6V Source V_{SS} = – 5V, V_{OH} = 5V Source	– 0.2 – 0.5	– 0.36 – 0.9	— —	– 0.14 – 0.35	— —	— —	mA
I_{OL}	Output Current Pins 14 to 23	V_{SS} = 0V, V_{OL} = 0.4V Sink V_{SS} = – 5V, V_{OL} = – 4.5V Sink	0.51 1.3	0.88 2.25	— —	0.36 0.9	— —	— —	mA
f_{CLK}	Clock Frequency	R_C = 300kΩ	—	66	—	—	—	—	kHz
I_{DU}	Input Current – DU		—	±0.00001	±0.3	—	—	±1	µA
Power									
I_Q	Quiescent Current	V_{DD} to V_{EE}, I_{SS} = 0, 14433A: V_{DD} = 5, V_{EE} = – 5 V_{DD} = 8, V_{EE} = –8 V_{DD} to V_{EE}, I_{SS} = 0, 14433: V_{DD} = 5, V_{EE} = – 5 V_{DD} = 8, V_{EE} = –8	 — — — —	 0.4 1.4 0.9 1.8	 2 4 2 4	 — — — —	 — — — —	 3.7 7.4 3.7 7.4	mA
PSRR	Supply Rejection	V_{DD} to V_{EE}, I_{SS} = 0, V_{REF} = 2V V_{DD} = 5, V_{EE} = – 5	—	0.5	—	—	—	—	mV/V

NOTES: 1. Accuracy — The accuracy of the meter at full-scale is the accuracy of the setting of the reference voltage. Zero is recalculated during each conversion cycle. The meaningful specification is linearity. In other words, the deviation from correct reading for all inputs other than positive full-scale and zero is defined as the linearity specification.
2. The LSD stability for 200mV scale is defined as the range that the LSD will occupy 95% of the time.
3. Pin numbers refer to 24-pin DIP.

PIN CONFIGURATIONS







TC14433
TC14433A

PIN DESCRIPTIONS

Pin No. 24-Pin PDIP/CerDip	Pin No. 24-Pin SOIC	Pin No. 28-Pin PLCC	Symbol	Description
1	1	2	V_{AG}	This is the analog ground; it has a high input impedance — This pin determines the reference level for the unknown input voltage (V_X) and the reference voltage (V_{REF}).
2	2	3	V_{REF}	Reference voltage — Full-scale output is equal to the voltage applied to V_{REF}. Therefore, full-scale voltage of 1.999V requires 2V reference and 199.9 mV full-scale requires a 200 mV reference. V_{REF} functions as system reset also. When switched to V_{EE}, the system is reset to the beginning of the conversion cycle.
3	3	4	V_X	The unknown input voltage (V_X) is measured as a ratio of the reference voltage (V_{REF}) in a ratiometric A/D conversion.
4	4	5	R_1	These pins are for external components used for the integration function in the dual slope conversion. Typical values are 0.1 µF (mylar) capacitor for C_1.
5	5	6	R_1/C_1	R_1 = 470 kW (resistor) for 2V full-scale.
6	6	7	C_1	R_1 = 27 kW (resistor) for 200 mV full-scale. Clock frequency of 66 kHz gives 250 msec conversion time. See equation below for calculation of integrator component values.
7	7	9	CO_1	These pins are used for connecting the offset correction capacitor. The recommended value is 0.1 µF.
8	8	10	CO_2	
9	9	11	DU	Display update input pin — When DU is connected to the EOC output every conversion is displayed. New data will be strobed into the output latches during the conversion cycle if a positive edge is received on DU prior to the ramp-down cycle. When this pin is driven from an external source, the voltage should be referenced to V_{SS}.
10	10	12	CLK_1	Clock input pins — The TC14433 has its own oscillator system clock. Connecting a single resistor between CLK_1 and CLK_0 sets the clock frequency.
11	11	13	CLK_0	A crystal or OC circuit may be inserted in lieu of a resistor for improved CLK_1, the clock input, can be driven from an external clock source, which need only have standard CMOS output drive. This pin is referenced to V_{EE} for external clock inputs. A 300 kW resistor yields a clock frequency of about 66 kHz. (See typical characteristic curves; see Figure 9 for alternate circuits.)
12	12	14	V_{EE}	Negative power current — Connection pin for the most negative supply. Please note the current for the output drive circuit is returned through V_{SS}. Typical supply current is 0.8 mA.
13	13	16	V_{SS}	Negative power supply for output circuitry — This pin sets the low voltage level for the output pins (BCD, Digit Selects, EOC, OR). When connected to analog ground, the output voltage is from analog ground to V_{DD}. If connected to V_{EE}, the output swing is from V_{EE} to V_{DD}. The recommended operating range for V_{SS} is between the V_{DD} –3 volts and V_{EE}.
14	14	17	EOC	End of conversion output generates a pulse at the end of each conversion cycle. This generated pulse width is equal to one-half the period of the system clock.
15	15	18	OR	Overrange pin — Normally this pin is set high. When V_X exceeds V_{REF} the OR pin is low.

PIN DESCRIPTIONS (Cont.)

Pin No. 24-Pin PDIP/CerDip	Pin No. 24-Pin SOIC	Pin No. 28-Pin PLCC	Symbol	Description
16	16	19	DS_4	Digit select pins — The digit select output goes high when the respective digit is selected. The MSD (1/2 digit) turns on immediately after an EOC pulse.
17	17	20	DS_3	The remaining digits turn on in sequence from MSD to LSD.
18	18	21	DS_2	To ensure that the BCD data has settled, an inter-digit blanking time of two clock periods is included.
19	19	23	DS_1	Clock frequency divided by 80 equals multiplex rate. For example, a system clock of 60 kHz gives a multiplex rate of 0.8 kHz.
20	20	24	Q_0	See Figure 12 for digit select timing diagram.
21	21	25	Q_1	BCD data output pins — Multiplexed BCD outputs contain three full digits of information during digit select DS_2, DS_3, DS_4.
22	22	26	Q_2	During DS_1, the 1/2 digit, overrange, underrange and polarity information is available.
23	23	28	Q_3	Refer to truth table.
24	24	28	V_{DD}	Positive power supply — This is the most positive power supply pin.
		8,15, 22	NC	Not Used.

CIRCUIT DESCRIPTION

The TC14433 CMOS IC becomes a modified dual-slope A/D with a minimum of external components. This IC has the customary CMOS digital logic circuitry, as well as CMOS analog circuitry. It provides the user with digital functions (such as counters, latches, multiplexers) and analog functions (such as operational amplifiers and comparators) on a single chip.

Features of this system include auto-zero, high input impedances and auto-polarity. Low power consumption and a wide range of power supply voltages are also advantages of this CMOS device. The system's auto-zero function compensates for the offset voltage of the internal amplifiers and comparators. In this "ratiometric system," the output reading is the ratio of the unknown voltage to the reference voltage, where a ratio of 1 is equal to the maximum count of 1999. It takes approximately 16,000 clock periods to complete one conversion cycle. Each conversion cycle may be divided into 6 segments. Figure 7 shows the conversion cycle in 6 segments for both positive and negative inputs.

Segment 1 — The offset capacitor (C_O), which compensates for the input offset voltages of the buffer and integrator amplifiers, is charged during this period. However, the integrator capacitor is shorted. This segment requires 4000 clock periods.

Segment 2 — During this segment, the integrator output decreases to the comparator threshold voltage. At this time, a number of counts equivalent to the input offset voltage of the comparator is stored in the offset latches for later use in the auto-zero process. The time for this segment is variable and less than 800 clock periods.

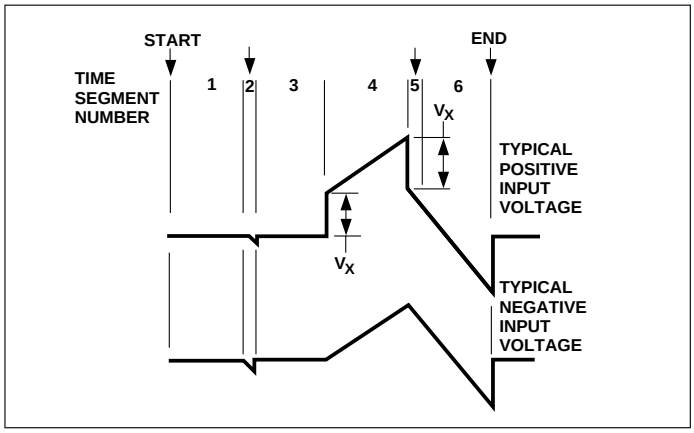


Figure 7. Integrator Waveforms at Pin 6

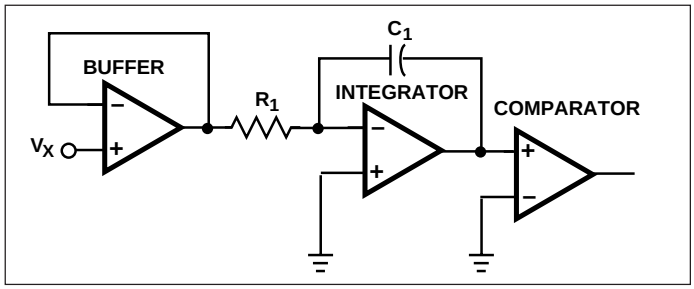


Figure 8. Equivalent Circuit Diagrams of the Analog

TC14433
TC14433A

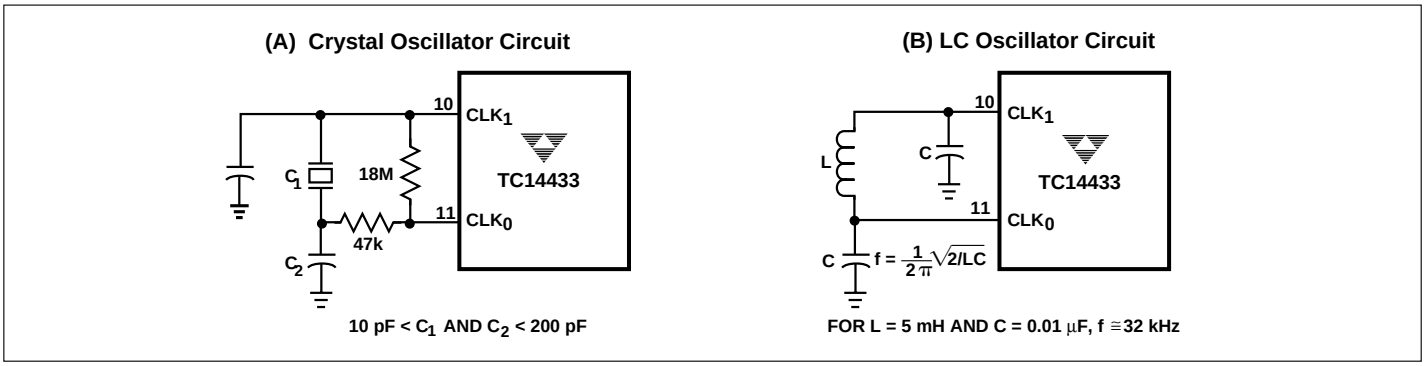


Figure 9. Alternate Oscillator Circuits

Segment 3 — This segment of the conversion cycle is the same as Segment 1.

Segment 4 — Segment 4 is an up-going ramp cycle with the unknown input voltage (V_X) as the input to the integrator. Figure 8 shows the equivalent configuration of the analog section of the TC14433. The actual configuration of the analog section is dependent upon the polarity of the input voltage during the previous conversion cycle.

Segment 5 — This segment is a down-going ramp period with the reference voltage as the input to the integrator. Segment 5 of the conversion cycle has a time equal to the number of counts stored in the offset storage latches during Segment 2. As a result, the system zeros automatically.

Segment 6 — This is an extension of Segment 5. The time period for this portion is 4000 clock periods. The results of the A/D conversion cycle are determined in this portion of the conversion cycle.

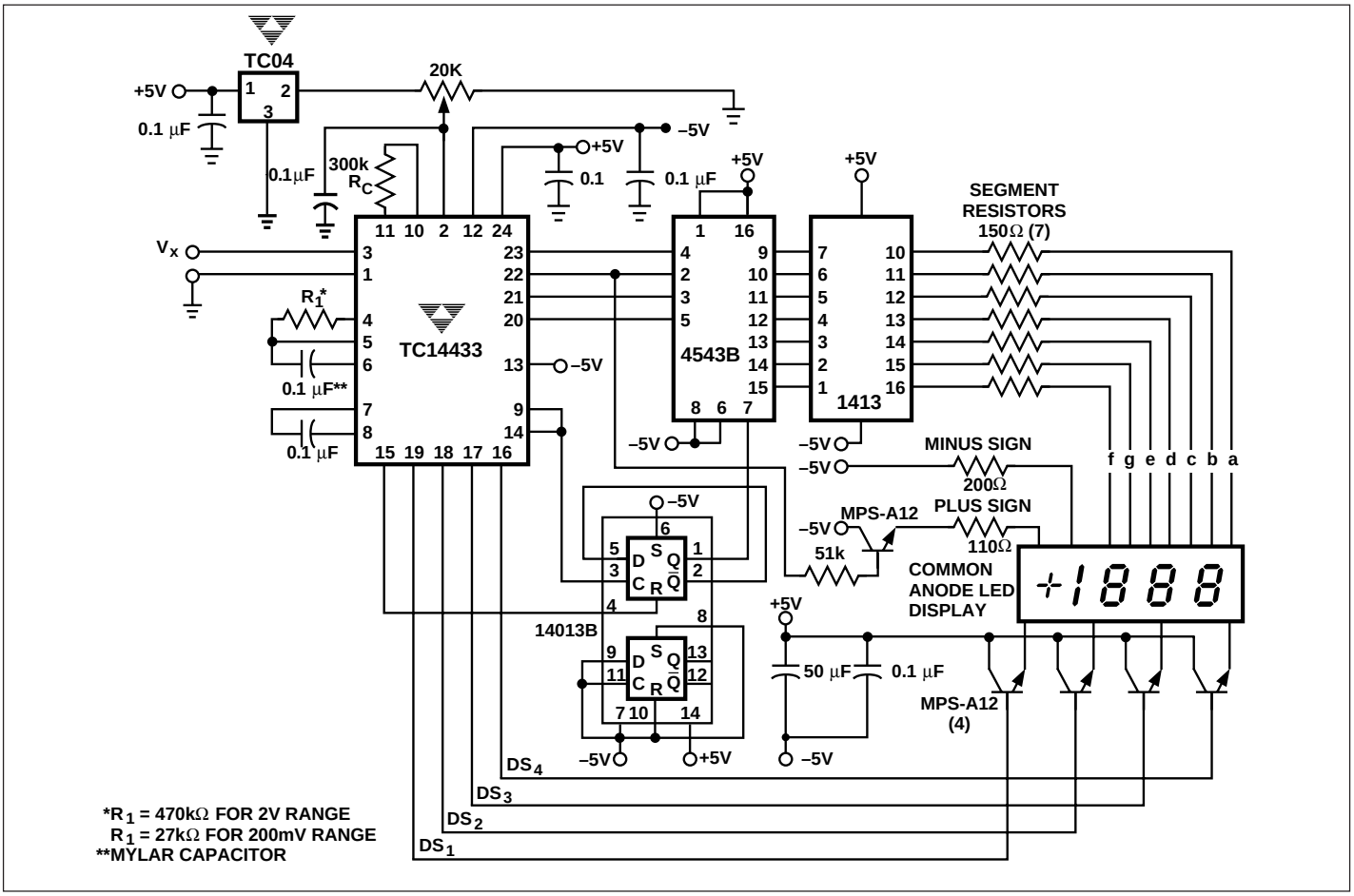


Figure 10. 3-1/2 Digit Voltmeter Common Anode Displays, Flashing Overrange

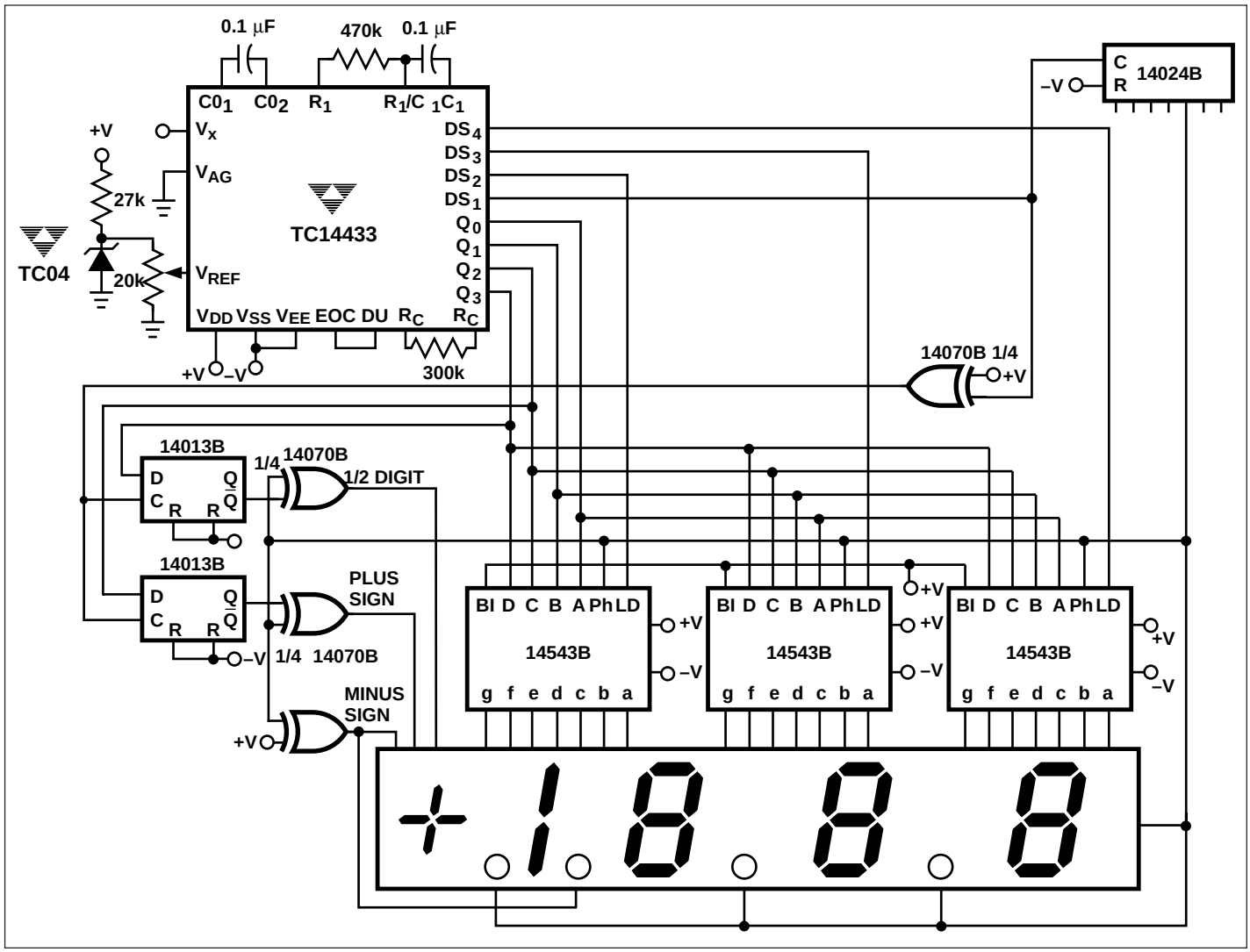


Figure 11. 3-1/2 Digit Voltmeter with LCD Display

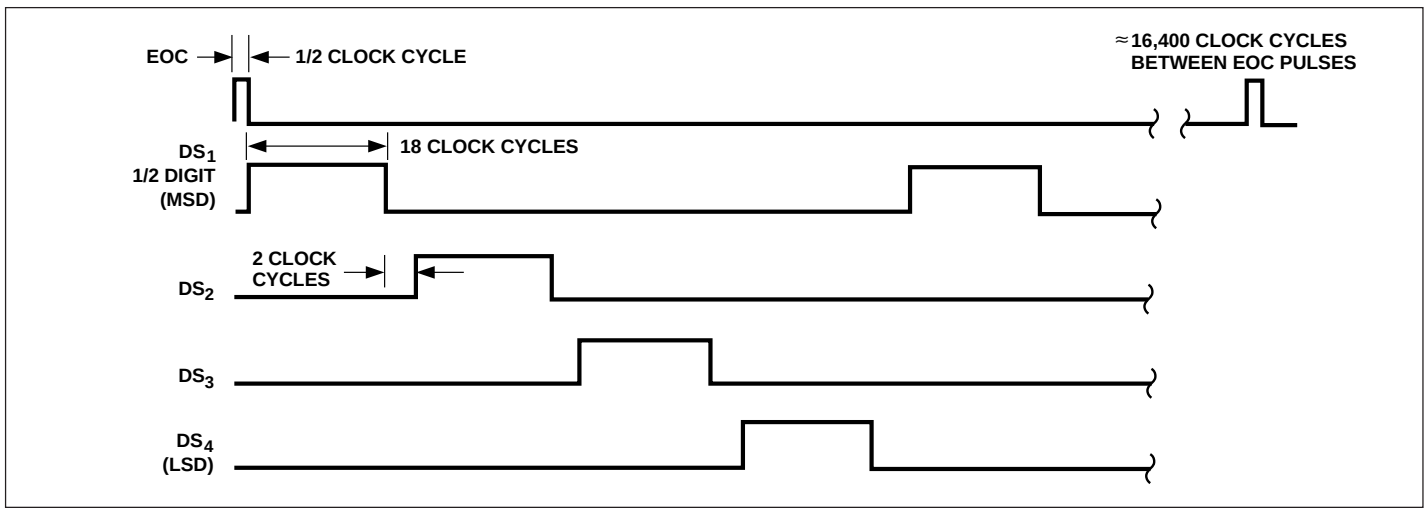


Figure 12. Digit Select Timing Diagram

TC14433
TC14433A

APPLICATIONS INFORMATION

Figure 10 is an example of a 3-1/2 digit voltmeter using the TC14433 with common-anode displays. This system requires a 2.5V reference. Full-scale may be adjusted to 1.999V or 199.9 mV. Input overrange is indicated by flashing a display. This display uses LEDs with common anode digit lines. Power supply for this system is shown as a dual ±5V supply; however, the TC14433 will operate over a wide voltage range (see recommended operating conditions, page 2).

The circuit in Figure 11 shows a 3-1/2 digit LCD voltmeter. The 14024B provides the low frequency square wave signal drive to the LCD backplane. Dual power supplies are shown here; however, one supply may be used when V_{SS} is connected to V_{EE}. In this case, V_{AG} must be at least 2.8V above V_{EE}.

When only segments b and c of the decoder are connected to the 1/2 digit of the display, 4, 0, 7 and 3 appear as 1.

The overrange indication (Q_3 = 0 and Q_0 = 1) occurs when the count is greater than 1999; e.g., 1.999V for a reference of 2V. The underrange indication, useful for autoranging circuits, occurs when the count is less than 180; e.g., 0.180V for a reference of 2V.

CAUTION

If the most significant digit is connected to a display other than a "1" only, such as a full digit display, segments other than b and c must be disconnected. The BCD to 7-segment decoder must blank on BCD inputs 1010 to 1111.

Figure 14 is an example of a 3-1/2 digit LED voltmeter with a minimum of external components (only 11 additional components). In this circuit, the 14511B provides the segment drive and the 75492 or 1413 provides sink for digit current. Display is blanked during the overrange condition.

TRUTH TABLE

Coded Condition					BCD to 7-Segment Decoding
of MSD	Q_3	Q_2	Q_1	Q_0	
+0	1	1	1	0	Blank
–0	1	0	1	0	Blank
+0 UR	1	1	1	1	Blank
–0 UR	1	0	1	1	Blank
+1	0	1	0	0	4–1, 0–1, 7–1, 3–1: Hook up only segments b and c to MSD
–1	0	0	0	0	
+1 OR	0	1	1	1	
–0 OR	0	0	1	1	

NOTES: Q_3 — 1/2 digit, low for "1", high for "0"
Q_2 — Polarity: "1" = positive, "0" = negative
Q_0 — Out of range condition exists if Q_0 = 1. When used in conjunction with Q_3, the type of out of range condition is indicated; i.e., $Q_3 = 0 \rightarrow$ OR or $Q_3 = 1 \rightarrow$ UR.

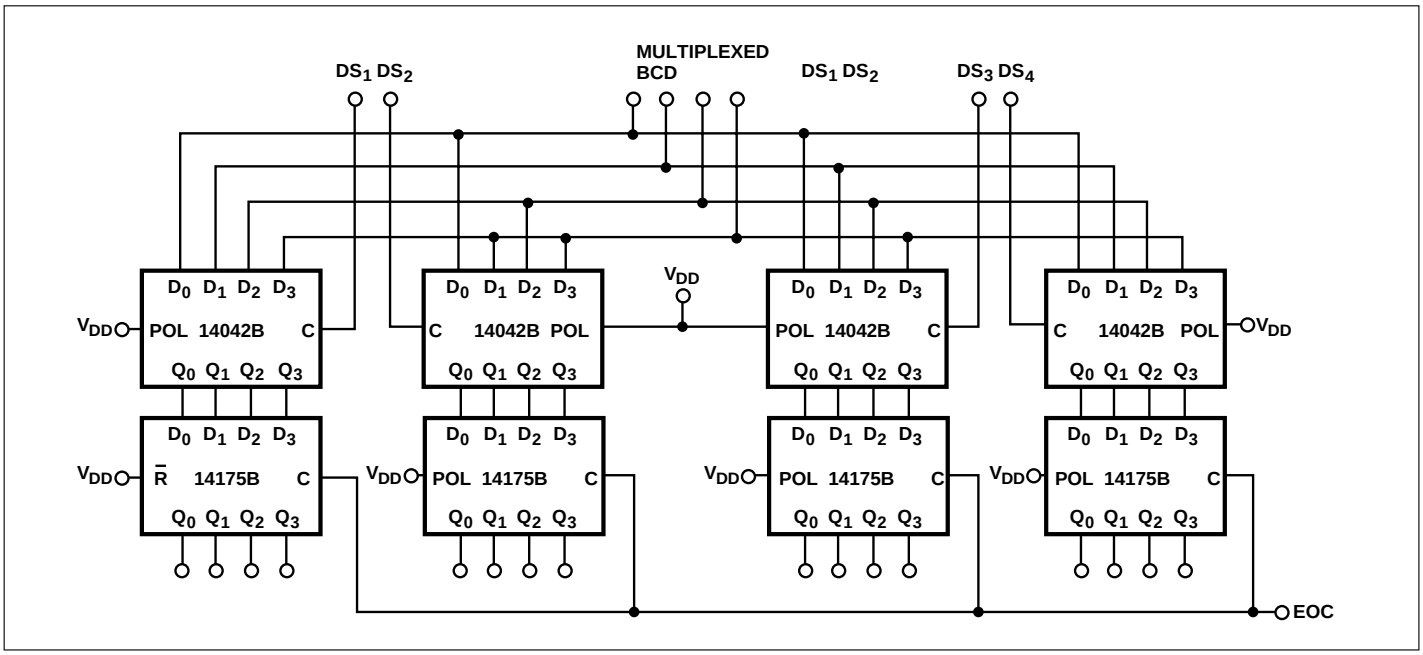


Figure 13 – Demultiplexing for TC14433 BCD Data

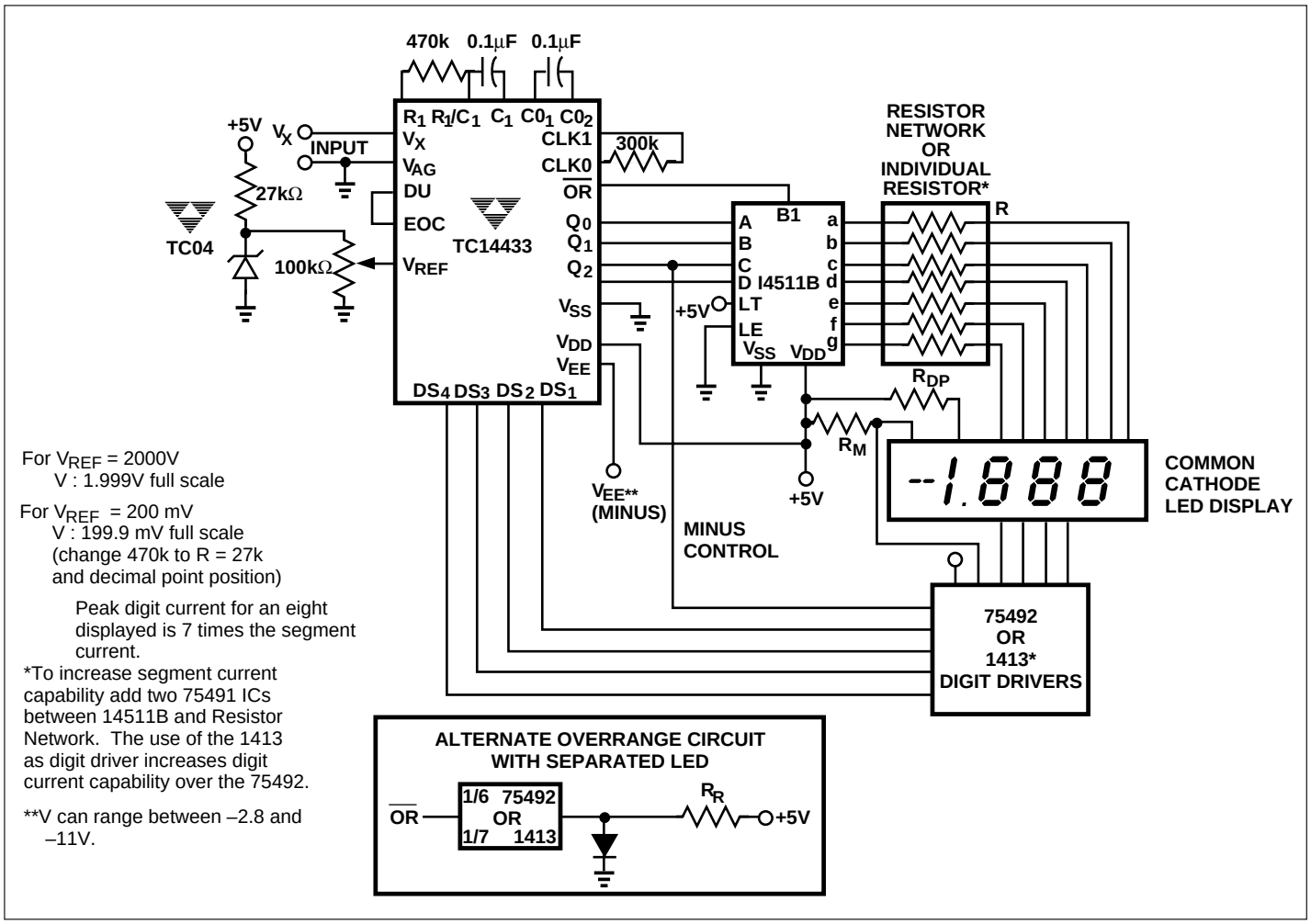
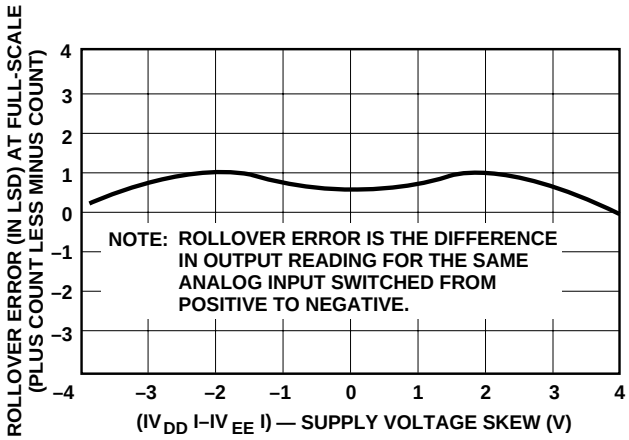
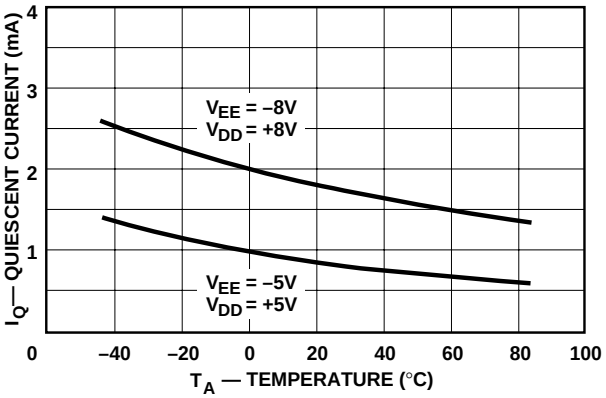


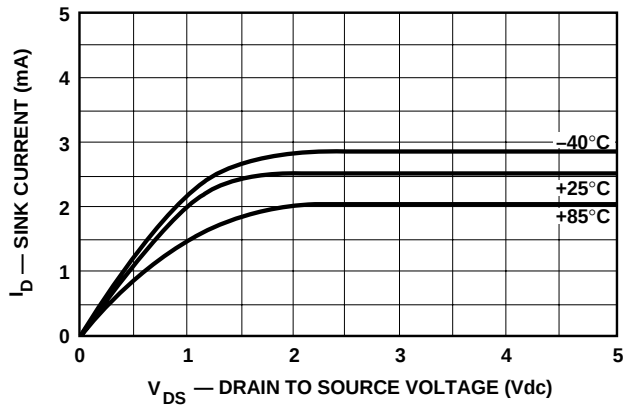
Figure 14. 3-1/2 Digit Voltmeter with Low Component Count Using Common Cathode Displays

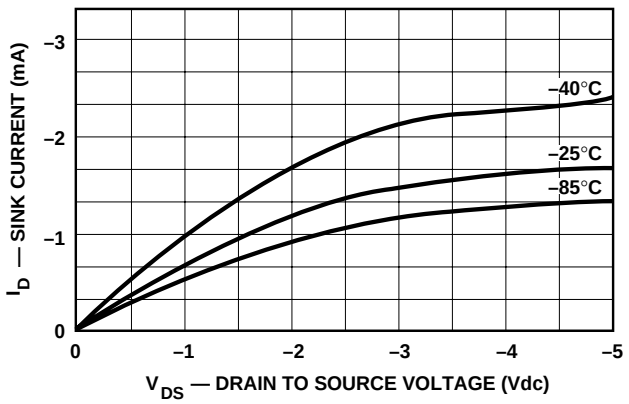
TC14433
TC14433A

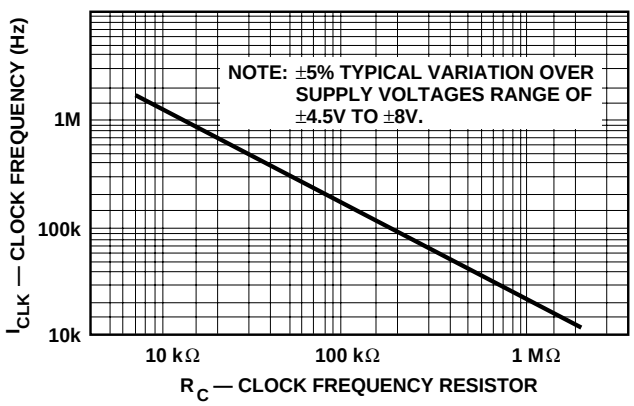
TYPICAL CHARACTERISTICS

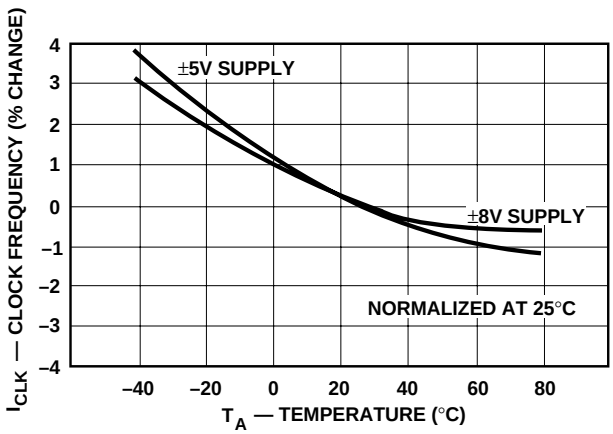












CONVERSION RATE = $\frac{\text{CLOCK FREQUENCY}}{16{,}400}$ ±1.5%
MULTIPLEX RATE = $\frac{\text{CLOCK FREQUENCY}}{80}$