

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC4W53FU

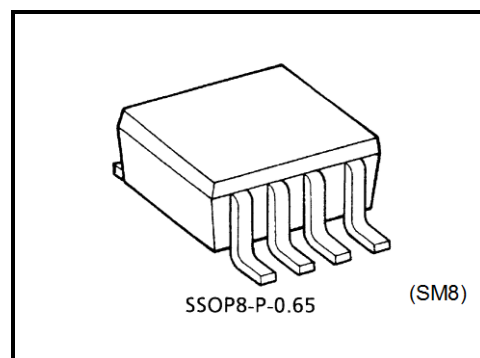
2-Channel Multiplexer, Demultiplexer

The TC4W53FU is multiplexer with capabilities of selection and mixture of analog signal and digital signal.

TC4W53FU has 2 channel configuration.

The digital signal to the control terminal turns "ON" the corresponding switch of each channel a large amplitude ($V_{DD} - V_{EE}$) can be switched by the control signal with small logical amplitude ($V_{DD} - V_{SS}$).

For example, in the case of $V_{DD} = 5\text{ V}$, $V_{SS} = 0\text{ V}$ and $V_{EE} = -5\text{ V}$, signals between -5 V and $+5\text{ V}$ can be switched from the logical circuit with a signal power supply of 5 V . As the ON-resistance of each switch is low, these can be connected to circuit with low input impedance.

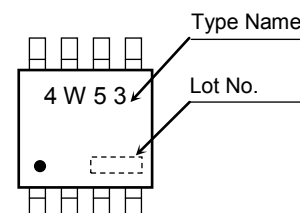


Weight
SSOP8-P-0.65: 0.02 g (typ.)

Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{DD}-V_{SS}$	-0.5 to 20	V
	$V_{DD}-V_{EE}$	-0.5 to 20	
Control input voltage	V_{CIN}	$V_{SS} - 0.5$ to $V_{DD} + 0.5$	V
Switch I/O voltage	$V_{I/O}$	$V_{EE} - 0.5$ to $V_{DD} + 0.5$	V
Control input current	I_{CIN}	± 10	mA
Potential difference across I/O during ON	V_{I-O}	-0.5 to 0.5	V
Power dissipation	P_D	300	mW
Operating temperature range	T_{opr}	-40 to 85	$^\circ\text{C}$
Storage temperature range	T_{stg}	-65 to 150	$^\circ\text{C}$
Lead temperature (10 s)	T_L	260	$^\circ\text{C}$

Marking



Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

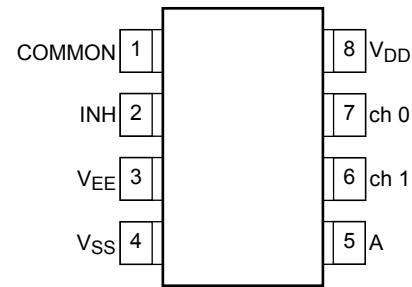
Start of commercial production
1990-05

Truth Table

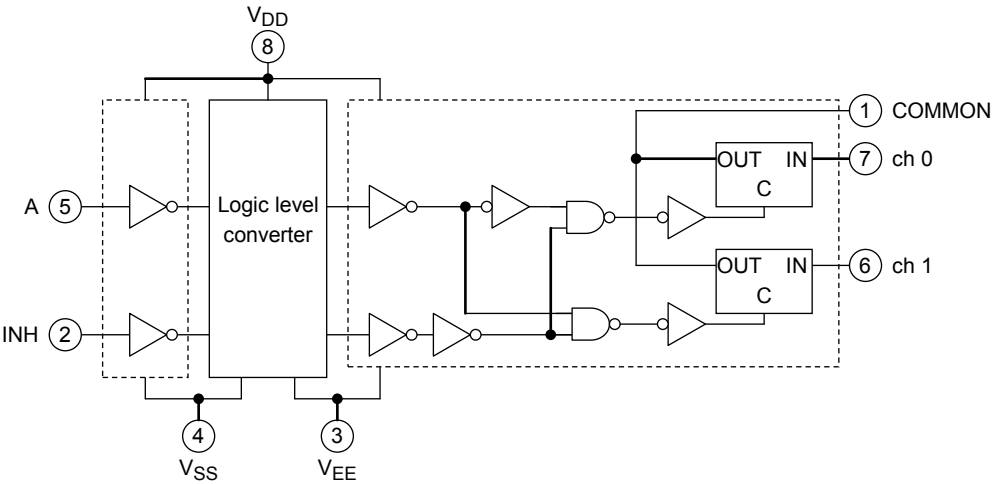
Control Input		On Channel
INH	A	
L	L	ch 0
L	H	ch 1
H	X	none

X: Don't care

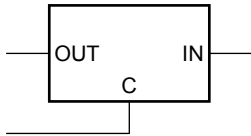
Pin Assignment (top view)



Logic Diagram



Truth Table



Control C	Impedance between IN/OUT
H	$0.5 \text{ to } 5 \times 10^2 \Omega$
L	$> 10^9 \Omega$

Operating Ranges

Characteristics	Symbol	Min.	Typ.	Max.	Unit
DC supply voltage	$V_{DD}-V_{SS}$	3	—	18	V
	$V_{DD}-V_{EE}$	3	—	18	
Control input voltage	V_{IN}	V_{SS}	—	V_{DD}	V
Switch input/output voltage	$V_{I/O}$	V_{EE}	—	V_{DD}	V

Static Electrical Characteristics

Characteristics	Symbol		Test Condition			Ta = −40°C		Ta = 25°C			Ta = 85°C		Unit
			VSS (V)	VEE (V)	VDD (V)	Min	Max	Min	Typ.	Max	Min	Max	
Control input high voltage	VIH	VIS = VDD	VEE = VSS RL = 1 kΩ ILS < 2 μA on all OFF channels		5	3.5	—	3.5	2.75	—	3.5	—	V
		10			7.0	—	7.0	5.50	—	7.0	—		
		15			11.0	—	11.0	8.25	—	11.0	—		
Control input low voltage	VIL	thru 1 kΩ			5	—	1.5	—	2.25	1.5	—	1.5	
					10	—	3.0	—	4.5	3.0	—	3.0	
					15	—	4.0	—	6.75	4.0	—	4.0	
On-state resistance	RON	0 ≤ VIS ≤ VDD RL = 10 kΩ	0	0	5	—	850	—	240	950	—	1200	Ω
			0	0	10	—	210	—	110	250	—	300	
			0	0	15	—	140	—	80	160	—	200	
ΔOn-state resistance (between any 2 switches)	ΔRON	—	0	0	5	—	—	—	10	—	—	—	Ω
			0	0	10	—	—	—	6	—	—	—	
			0	0	15	—	—	—	4	—	—	—	
Input/output leakage current	IOFF	VIN = 18 V, VOUT = 0 V VIN = 0 V, VOUT = 18 V	18			—	±100	—	±0.01	±100	—	±1000	nA
			18			—	±100	—	±0.01	±100	—	±1000	
Quiescent device current	IDD	VIN = VSS, VDD (Note)	5			—	5.0	—	0.005	5.0	—	150	μA
			10			—	10	—	0.010	10	—	300	
			15			—	20	—	0.015	20	—	600	
Input current	IIN	VIH = 18 V, VIL = 0 V	18			—	0.1	—	10 ^{−5}	0.1	—	1.0	μA
			18			—	−0.1	—	−10 ^{−5}	−0.1	—	−1.0	
Input capacitance	CIN	—	—			—	—	—	5	7.5	—	—	pF
Switch Input Capacitance	CIN	—	—			—	—	—	10	—	—	—	pF
Switch Output Capacitance	COUT		10			—	—	—	17	—	—	—	
Feed through capacitance	CIN-COUT	—	10			—	—	—	0.2	—	—	—	pF

Note : All valid input combinations.

Dynamic Electrical Characteristics (Ta = 25°C, CL = 50 pF)

Characteristics	Symbol	Test Condition				Min	Typ.	Max	Unit
			VSS (V)	VEE (V)	VDD (V)				
Phase difference between input to output (switch IN-OUT)	ϕ_{I-O}	—	0	0	5	—	15	45	ns
			0	0	10	—	8	20	
			0	0	15	—	6	15	
Propagation delay time (A-OUT)	t_{pZL} t_{pZH} t_{pLZ} t_{pHZ}	$R_L = 1\text{ k}\Omega$	0	0	5	—	170	550	ns
			0	0	10	—	90	240	
			0	0	15	—	70	160	
			0	-5	5	—	100	240	
			0	-7.5	7.5	—	80	160	
Propagation delay time (INH-OUT)	t_{pZL} t_{pZH}	$R_L = 1\text{ k}\Omega$	0	0	5	—	120	380	ns
			0	0	10	—	60	200	
			0	0	15	—	50	160	
			0	-5	5	—	80	200	
			0	-7.5	7.5	—	60	160	
	t_{pLZ} t_{pHZ}	$R_L = 1\text{ k}\Omega$	0	0	5	—	170	450	ns
			0	0	10	—	90	210	
			0	0	15	—	70	160	
			0	-5	5	—	100	210	
			0	-7.5	7.5	—	80	160	
Frequency response	f_{MAX} (I-O)	$R_L = 1\text{ k}\Omega$ (Note 1)	-5	-5	5	—	40	—	MHz
Total harmonic distortion	—	$R_L = 10\text{ k}\Omega$ $f = 1\text{ kHz}$ (Note 2)	-2.5	-2.5	2.5	—	0.15	—	%
			-5	-5	5	—	0.03	—	
			-7.5	-7.5	7.5	—	0.02	—	
Feedthrough frequency (switch off)	—	$R_L = 1\text{ k}\Omega$ (Note 3)	-5	-5	5	—	500	—	kHz
Crosstalk frequency	—	$R_L = 1\text{ k}\Omega$ (Note 4)	-5	-5	5	—	1.5	—	MHz
Crosstalk (CONTROL-OUT)	—	$R_{IN} = 1\text{ k}\Omega$ $R_{OUT} = 10\text{ k}\Omega$ $C_L = 15\text{ pF}$	0	0	5	—	200	—	mV
			0	0	10	—	400	—	
			0	0	15	—	600	—	

Note 1: Sine wave of $\pm 2.5\text{ V}_{p-p}$ shall be used for V_{IS} and the frequency of $20 \log_{10} \frac{V_{OS}}{V_{IS}} = -3\text{dB}$ shall be f_{MAX} .

Note 2: V_{IS} shall be sine wave of $\pm \left(\frac{V_{DD} - V_{EE}}{4} \right)_{p-p}$.

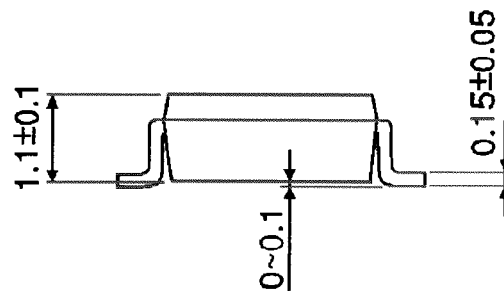
Note 3: Sine wave of $\pm 2.5\text{ V}_{p-p}$ shall be used for V_{IS} and the frequency of $20 \log_{10} \frac{V_{OS}}{V_{IS}} = -50\text{dB}$ shall be feed-through.

Note 4: Sine wave of $\pm 2.5\text{ V}_{p-p}$ shall be used for V_{IS} and the frequency of $20 \log_{10} \frac{V_{OS}}{V_{IS}} = -50\text{dB}$ shall be crosstalk.

SSOP8-P-0.65

Technical drawing of the top view of a rectangular microchip. The chip has a central square area and four rectangular pads on each side. Dimensions are given in millimeters.

- Overall width: 4.0 ± 0.1 mm
- Overall height: 2.9 ± 0.1 mm
- Central square area width: 2.8 ± 0.1 mm
- Left and right pads width: 0.65 mm
- Top and bottom pads width: $0.2^{+0.1}_{-0.05}$ mm
- Pad numbers: 1 (top left), 4 (bottom left), 5 (bottom right), 8 (top right)



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