SILICON STACKED GATE MOS INTEGRATED CIRCUIT

TC5316200AP/AF

16M BIT (1M WORD × 16 BIT / 2M WORD × 8BIT) CMOS MASK ROM

DESCRIPTION

The TC5316200AP / AF is a 16,777,216 bits read only memory organized as 1,048,576 words by 16 bits when $\overline{BYTE}$ is logical high, and is organized as 2,097,152 words by 8 bits when $\overline{BYTE}$ is logical low.

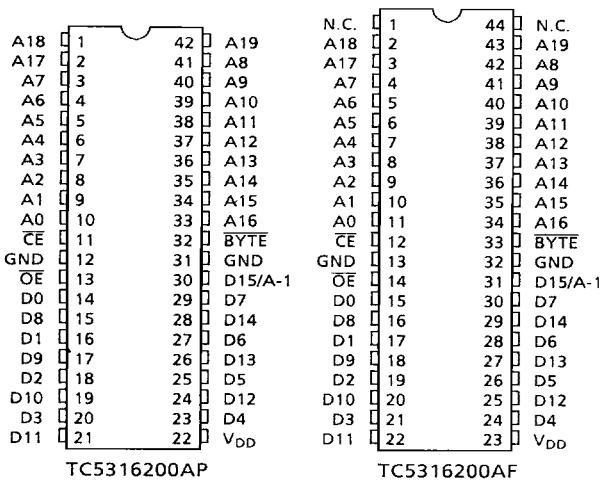
The TC5316200AP / AF is most suitable for the program memory , data memory , and character generater.

The TC5316200AP / AF is packaged in a standard 600mil 42pin DIP, or 600mil 44 pin SOP.

FEATURES

- Single 5V Power Supply
- Access Time : 150ns (Max.)
- Power Dissipation
  - Operating Current : 60mA (Max.)
  - Standby Current : 100μA (Max.)
- Fully Static Operation
- All Inputs and Outputs : TTL Compatible
- Three State Outputs
- TC5316200AP : DIP42-P-600
- TC5316200AF : SOP44-P-600

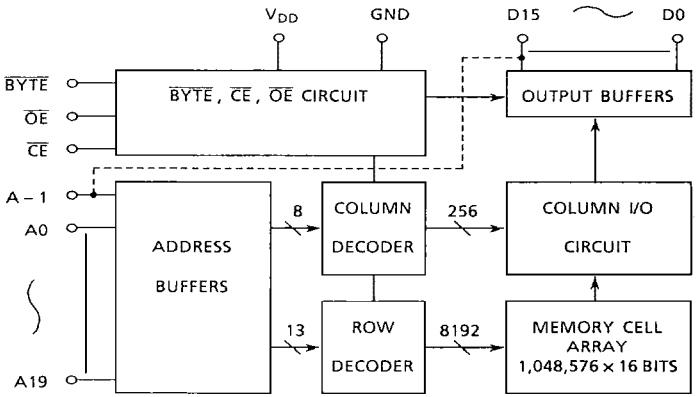
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A19	Address inputs
D0~D14	Data Outputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
D15/A-1	Data Output/Addrss Input
$\overline{BYTE}$	Word, Byte selection Input
V_{DD}	Power Supply
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MODE SELECTION

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	D0 – D7	D8 – D14	D15 / A – 1	Power
Read (16 Bit)	L	L	H	Data Out			Active
Read (8 Bit)	L	L	L	Data Out (Lower 8bit)	High Impedance	L	Active
Read (8 Bit)	L	L	L	Data Out (Upper 8bit)	High Impedance	H	Active
Output Deselect	L	H	*	High Inpedance			Active
Standby	H	*	*	High Inpedance			Standby

H : V_{IH} L : V_{IL} * : V_{IH} or V_{IL}

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	– 0.5~7.0	V
V_{IN}	Input Voltage	– 0.5~V_{DD}	V
V_{OUT}	Output Voltage	0~V_{DD}	V
P_D	Power Dissipation	1.0 / 0.6*	W
T_{STG}	Storage Temperature	– 55~150	°C
T_{OPR}	Operating Temperature	0~70	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec

* SOP

D.C. OPREATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	– 0.3	–	0.8	V

D.C. and OPERATING CHARACTERISTICS (Ta = 0~70°C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	–	± 1.0	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 0 \sim V_{DD}$	–	± 5.0	μA
I_{OH}	Output High Current	$V_{OH} = 2.4V$	– 1.0	–	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4V$	2.0	–	mA
I_{DDS1}	Standby Current	$\overline{CE} = V_{IH}$	–	2	mA
I_{DDS2}		$\overline{CE} = V_{DD} - 0.2V$	–	100	μA
I_{DDO1}	Opereating Current	$V_{IN} = V_{IH} / V_{IL}$, $t_{cycle} = 150ns$	–	70	mA
I_{DDO2}		$V_{IN} = V_{DD} - 0.2V / 0.2V$, $t_{cycle} = 150ns$	–	60	mA

CAPACITANCE f = 1MHz , Ta = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = 0V$	–	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	–	12	pF

Note : This Paramenter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (Ta = 0~70°C, V_{DD} = 5V ± 10%)

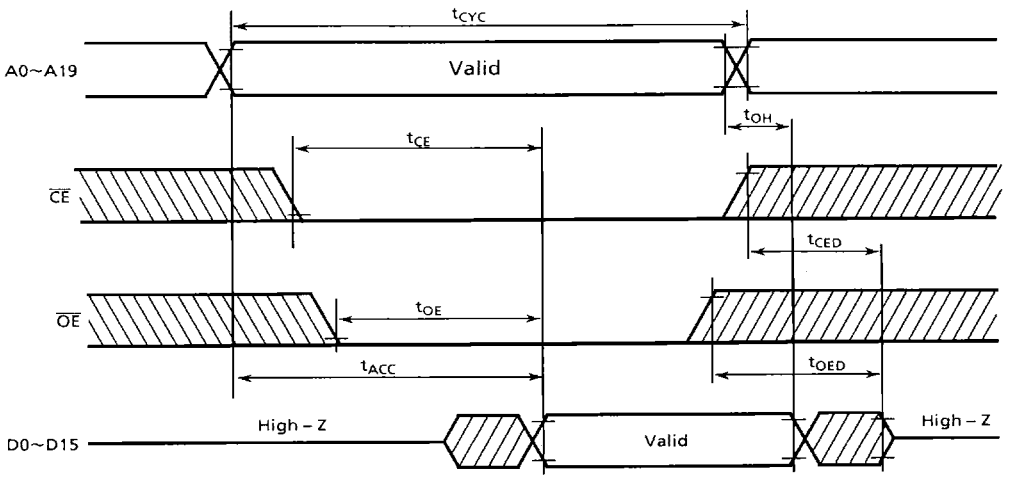
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{CYC}	Cycle Time	150	–	ns
t_{ACC}	Address Access Time	–	150	ns
t_{CE}	Chip Enable Access Time	–	150	ns
t_{BT}	$\overline{BYTE}$ Access Time	–	150	ns
t_{OE}	Output Enable Access Time	–	70	ns
t_{CED}	Output Disable Time from $\overline{CE}$	–	40	ns
t_{OED}	Output Disable Time from $\overline{OE}$	–	40	ns
t_{BTD}	Output Disable Time from $\overline{BYTE}$	–	40	ns
t_{OH}	Output Hold Time	5	–	ns

A.C. TEST CONDITIONS

Output Load		: 100pF + 1TTL
Input Levels		: 0.6V , 2.4V
Timing Measurement Reference Levels	Input	: 0.8V , 2.2V
	Output	: 0.8V , 2.0V
Input Rise and Fall Time		: 5ns

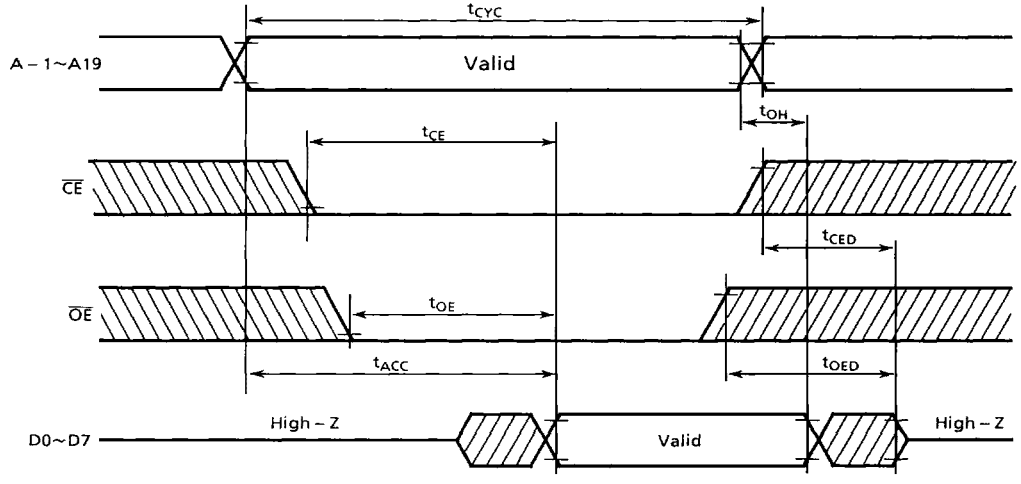
TIMING WAVEFORMS

WORD – WIDE READ MODE



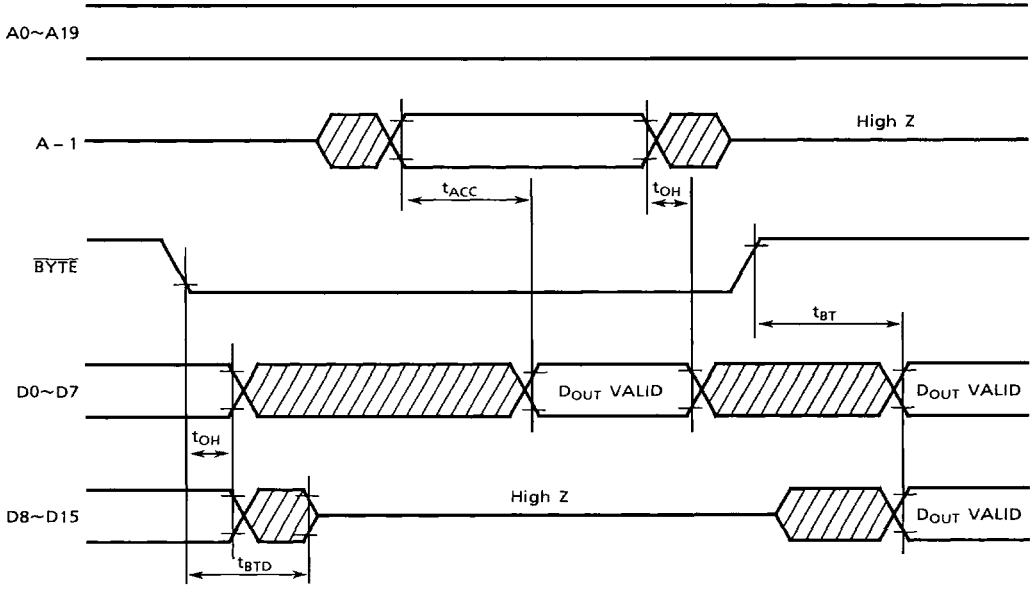
Note: $\overline{BYTE}$ = V_{IH}

BYTE – WIDE READ MODE



Note: $\overline{BYTE}$ = V_{IL}

$\overline{BYTE}$ TRANSITION



Note: $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IL}