TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74HC279AP, TC74HC279AF

Quad S-R Latch

The TC74HC279A is a high speed CMOS QUAD S-R LATCH fabricated with silicon gate $\mathrm{C}^2\mathrm{MOS}$ technology.

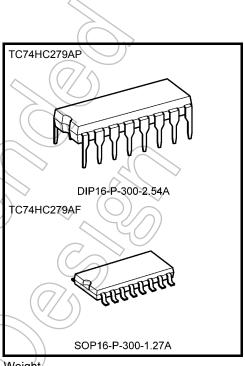
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Each latch has an independent Q output and Set and Reset inputs. \overline{S} and \overline{R} are active low. When \overline{S} input is low, the Q output goes high and when \overline{R} input is low, the Q output goes low. When both \overline{S} and \overline{R} are low, \overline{S} takes precedence resulting Q = low. When both of \overline{S} and \overline{R} are held high, Q output doesn't change.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

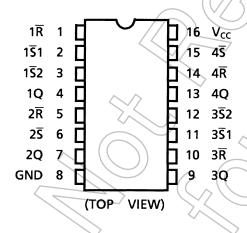
- High speed: $t_{pd} = 12 \text{ ns (typ.)}$ at $V_{CC} = 5 \text{ V}$
- Low power dissipation: $I_{CC} = 2 \mu A$ (max) at $T_a = 25$ °C
- High noise immunity: V_{NIH} = V_{NIL} = 28% V_{CC} (min)
- Symmetrical output impedance: |IOH| = IOL = 4 mA (min)
- Balanced propagation delays: $t_{pLH} \simeq t_{pHI}$
- Wide operating voltage range: V_{CC} (opr) = 2 to 6 V
- Pin and function compatible with 74LS279



Weight/

DIP16-P-300-2.54A : 1.00 g (typ.) SOP16-P-300-1.27A : 0.18 g (typ.)

Pin Assignment



IEC Logic Symbol

$ \begin{array}{c c} 1\overline{S1} & (2) & & & & \\ 1\overline{S2} & (3) & & & & \\ 1\overline{R} & (1) & & & & \\ \end{array} $	1	(<u>4)</u> 1Q
$ \begin{array}{c c} \hline 2S & (6) & S2 \\ \hline 2R & (11) & R \end{array} $	2	(7) 2Q
S1 S1 S1 S1 S1 S2 S2 S2	3	(9) 3Q
$ 4\overline{S} \xrightarrow{(15)} S4 $ $ 4\overline{R} \xrightarrow{(14)} R $	4	(13) 4Q

Truth Table

Inputs		Output
S#	R	Q
Н	Н	Qn
L	Н	Н
Н	L	L
L	L	Н

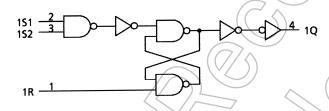
Qn: The level of Q before the indicated input condition were established.

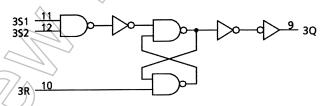
#: For latches with doubles \overline{S} input.

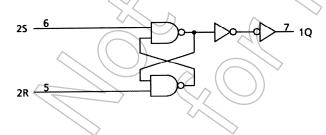
 $H = Both \ \overline{S} \ input high$

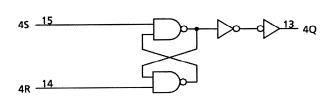
L = One of both inputs low

System Diagram









Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	–0.5 to 7	V
DC input voltage	V _{IN}	-0.5 to V _{CC} + 0.5	V
DC output voltage	V _{OUT}	-0.5 to V _{CC} + 0.5	⟨v
Input diode current	I _{IK}	±20	mA
Output diode current	lok	±20	mA
DC output current	lout	±25	mA
DC V _{CC} /ground current	Icc	±50	_ mA
Power dissipation	PD	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	T _{stg}	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of Ta = -40 to 65°C. From Ta = 65 to 85°C a derating factor of -10 mW/°C shall be applied until 300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	VCC	2 to 6	V
Input voltage	// ŷ _{IN}	0 to V _{CC}	٧
Output voltage	Vout	0 to V _{CC}	V
Operating temperature	Topr	-40 to 85	°C
		0 to 1000 (V _{CC} = 2.0 V)	
Input rise and fall time	t _r , t _f	0 to 500 (V _{CC} = 4.5 V)	ns
		0 to 400 (V _{CC} = 6.0 V)	

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		Test Condition		Ta = 25°C			Ta = -40 to 85°C	
				V _{CC} (V)	Min	Тур.	Max	Min	Max	
				2.0	1.50	_	1	1.50	_	
High-level input voltage	V _{IH}		_	4.5	3.15	_		3.15	_	V
				6.0	4.20			4.20	_	
				2.0	_	+0	0.50	_	0.50	
Low-level input voltage	V_{IL}		_	4.5	-	7/	1.35	_	1.35	V
			_	6.0	-(1	1.80	_	1.80	
				2.0	1.9	2.0	_	1.9	_	
		V _{IN} = V _{IH} or V _{IL}	$I_{OH} = -20 \mu A$	4.5	4.4	4.5	_	4.4	_	
High-level output voltage	V _{OH}			6.0	5.9	6.0		5.9	\searrow	V
			$I_{OH} = -4 \text{ mA}$	4.5	4.18	4.31	-6	4.13	> —	_
			$I_{OH} = -5.2 \text{ mA}$	6.0	5.68	5.80	(5.63) —	
				2.0	_	0.0	0.1		0.1	
			I _{OL} = 20 μA	4.5	_	0.0	0.1	~ _	0.1	
Low-level output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}		6.0	—	0.0	0.1	_	0.1	V
			I _{OL} = 4 mA	4.5	_	0.17	0.26	_	0.33	
		I _{OL} = 5.2 mA	6.0		0.18	0.26	_	0.33		
Input leakage current	I _{IN}	V _{IN} = V _{CC} or	GND	6.0	_		±0.1	_	±1.0	μА
Quiescent supply current	Icc	V _{IN} = V _{CC} or	GND	6.0		/_	2.0	_	20.0	μА

AC Characteristics (C_L = 15 pF, V_{CC} = 5 V, Ta = 25°C, input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Output transition time	t _{TLH}	<u> </u>	_	4	8	ns
Propagation delay time (S1, S2-Q)	t _{pLH}	_	_	12	22	ns
Propagation delay time	t _{pkH}	_	_	9	17	ns
Propagation delay time (R-Q)	t _{pLH}	_	_	11	20	ns

AC Characteristics (C $_{L}=50\ pF,$ input: $t_{r}=t_{f}=6\ ns)$

Characteristics	Symbol	Symbol Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit
	- ,		V _{CC} (V)	Min	Тур.	Max	Min	Max	
Output transition time	t _{TLH} t _{THL}	-	2.0 4.5 6.0		30 8 7	75 15 13		95 19 16	ns
Propagation delay time (\$\overline{S}1\$, \$\overline{S}2\$-Q)	t _{pLH} t _{pHL}	_	2.0 4.5 6.0	_ _ _ _	45 15 13	130 26 22		165 33 28	ns
Propagation delay time (\$\overline{S}\$-Q)	t _{pLH} t _{pHL}	_	2.0 4.5 6.0	- (38 12 10	100 20 17		125 25 21	ns
Propagation delay time (R -Q)	t _{pLH}	_	2.0 4.5 6.0		42 14 12	120 24 20		150 30 26	ns
Input capacitance	C _{IN}	_		<i>J</i>	5 🛇	10		10	pF
Power dissipation capacitance	C _{PD} (Note)	- (18	7	\$ <u></u>	_	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

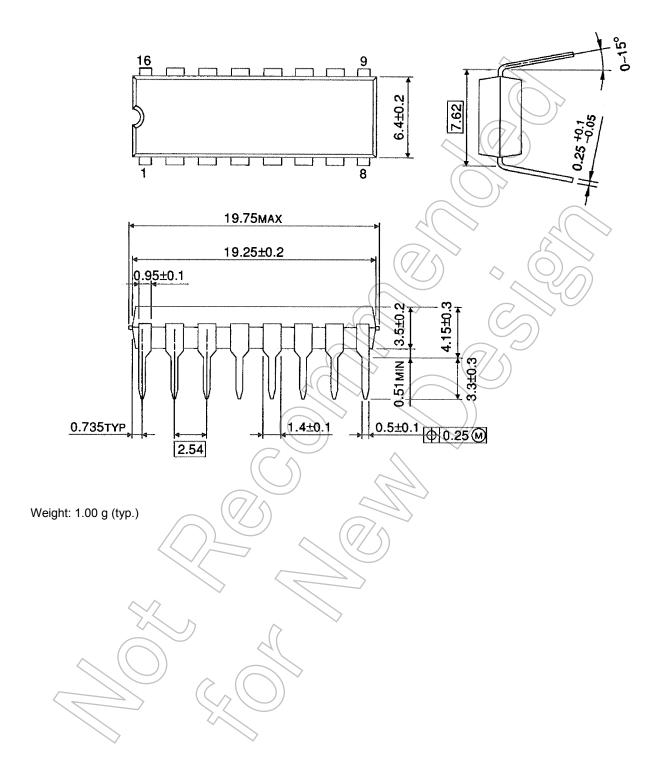
Average operating current can be obtained by the equation:

$$I_{CC}$$
 (opr) = $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per circuit)



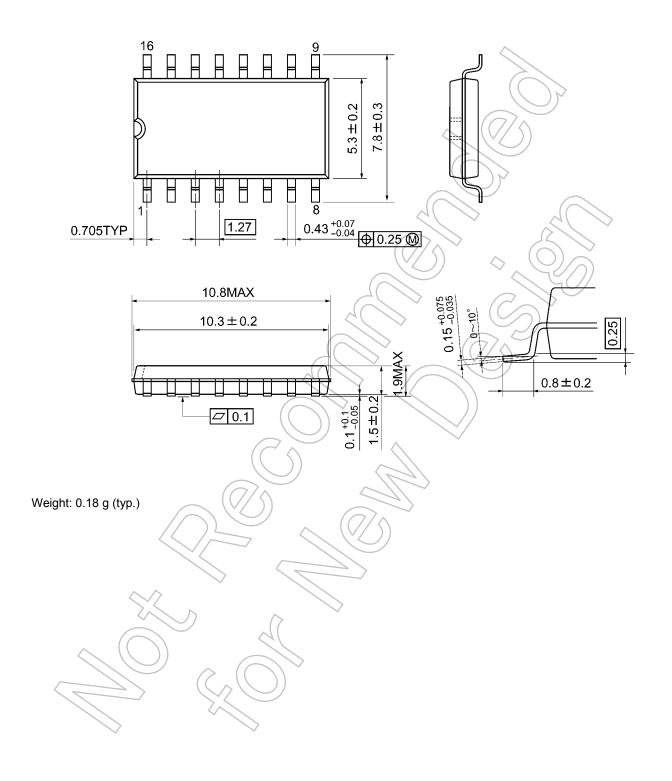
Package Dimensions

DIP16-P-300-2.54A Unit: mm



Package Dimensions

SOP16-P-300-1.27A Unit: mm



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